



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

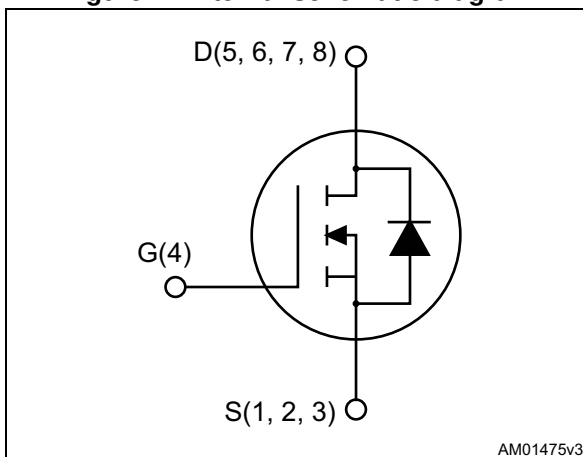


N-channel 30 V, 0.0076 Ω typ., 56 A STripFET™ H5 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet — production data



Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on) \max}$	I_D
STL56N3LLH5	30 V	0.009 Ω	56 A

- Low on-resistance $R_{DS(on)}$
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™ H5 technology. The device has been optimized to achieve very low on-state resistance, contributing to a FoM that is among the best in its class.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL56N3LLH5	56N3LH5	PowerFLAT™ 5x6	Tape and reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
2.1	Electrical characteristics (curves)	6
3	Test circuits	8
4	Package mechanical data	9
5	Packaging mechanical data	13
6	Revision history	15

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	+22 / -20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	56	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	37	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25^\circ\text{C}$	15	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 100^\circ\text{C}$	10	A
$I_{DM}^{(1)(3)}$	Drain current (pulsed)	224	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	60	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25^\circ\text{C}$	62.5	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25^\circ\text{C}$	4	W
$E_{AS}^{(4)}$	Single pulse avalanche energy	150	mJ
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. The value is rated according to R_{thj-c}
2. The value is rated according to $R_{thj-pcb}$
3. Pulse width limited by safe operating area
4. Starting $T_j = 25^\circ\text{C}$, $I_D = 56\text{ A}$, $V_{DD} = 50\text{ V}$

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{ sec}$

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0, I _D = 250 μA	30			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0, V _{DS} = 30 V,			1	μA
		V _{GS} = 0 V _{DS} = 30 V, T _C = 125 °C			10	μA
I _{GSS}	Gate body leakage current	V _{DS} = 0, V _{GS} = +22 / -20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	1		2.5	V
R _{DS(on)}	Static drain-source on- resistance	V _{GS} = 10 V, I _D = 7.5 A		0.0076	0.009	Ω
		V _{GS} = 4.5 V, I _D = 7.5 A		0.0099	0.0112	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} =25 V, f=1 MHz, V _{GS} =0	-	950		pF
C _{oss}	Output capacitance		-	193		pF
C _{rss}	Reverse transfer capacitance		-	27		pF
Q _g	Total gate charge	V _{DD} =15 V, I _D = 15 A	-	6.5	10	nC
Q _{gs}	Gate-source charge	V _{GS} =4.5 V	-	3.3		nC
Q _{gd}	Gate-drain charge	<i>Figure 14</i>	-	2.4		nC
R _g	Gate input resistance	f = 1 MHz, gate DC Bias = 0, test signal level = 20 mV, I _D = 0	-	1.7	2.5	Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}$, $I_D=7.5\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=10\text{ V}$ <i>Figure 13</i>	-	10.8	-	ns
t_r	Rise time		-	15.6	-	ns
$t_{d(off)}$	Turn-off delay time		-	14.2	-	ns
t_f	Fall time		-	6	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		56	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		224	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 15\text{ A}$, $V_{GS}=0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 15\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=25\text{ V}$, $T_j=150\text{ }^\circ\text{C}$	-	20	36	ns
Q_{rr}	Reverse recovery charge		-	10	18	nC
I_{RRM}	Reverse recovery current		-	1		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration= 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

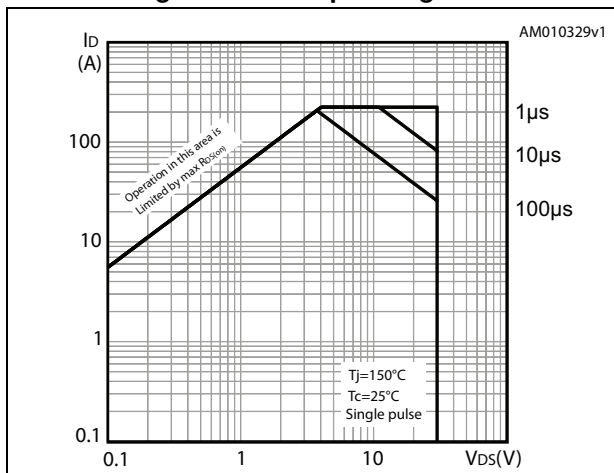


Figure 3. Thermal impedance

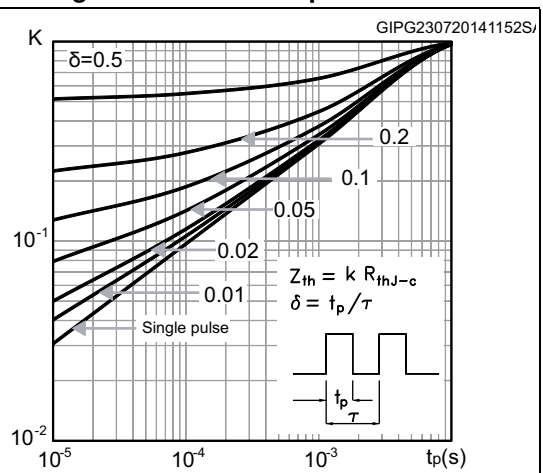


Figure 4. Output characteristics

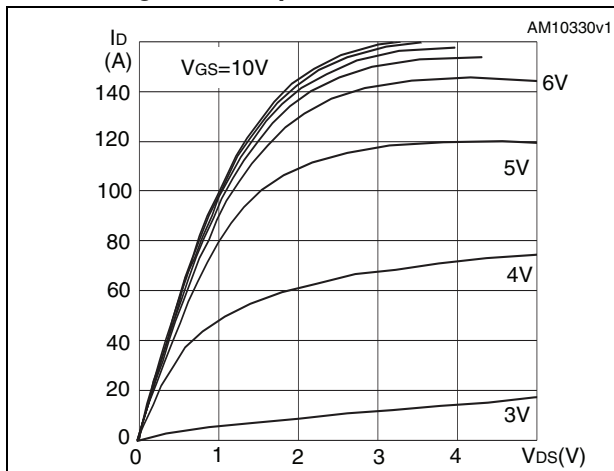


Figure 5. Transfer characteristics

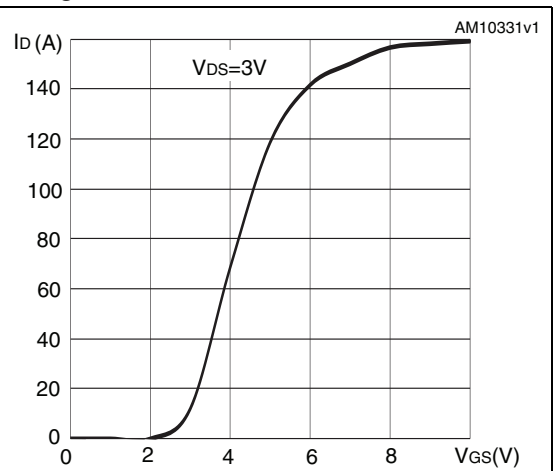


Figure 6. Normalized $V_{(BR)DSS}$ vs temperature

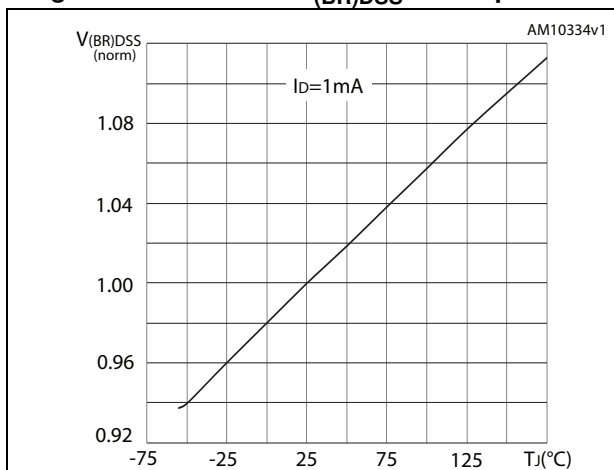


Figure 7. Static drain-source on-resistance

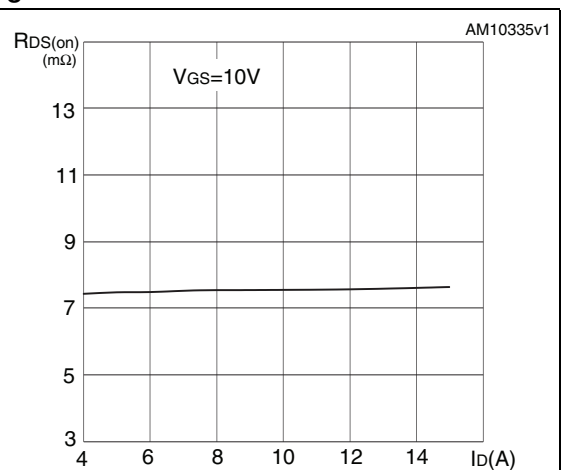


Figure 8. Gate charge vs gate-source voltage

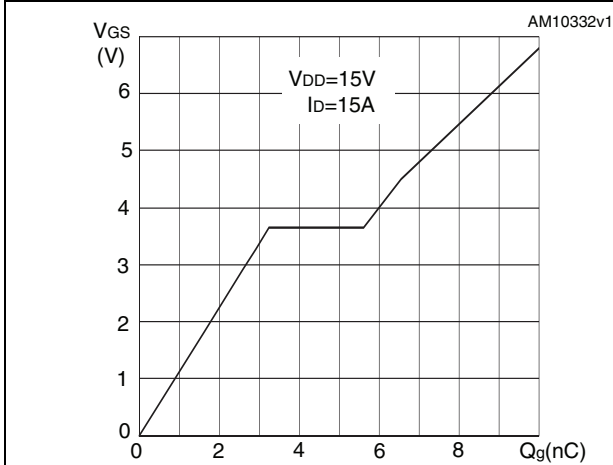


Figure 9. Capacitance variations

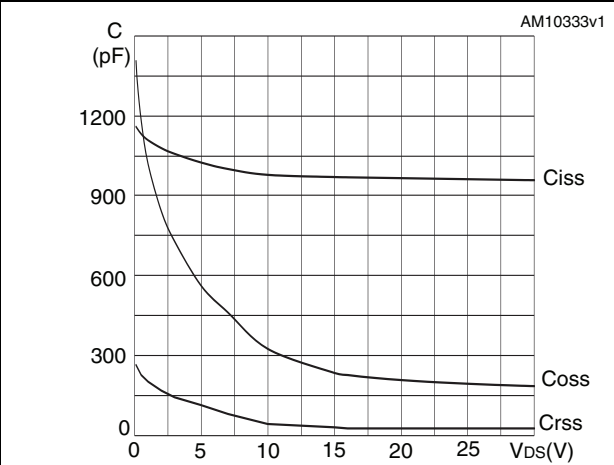


Figure 10. Normalized gate threshold voltage vs temperature

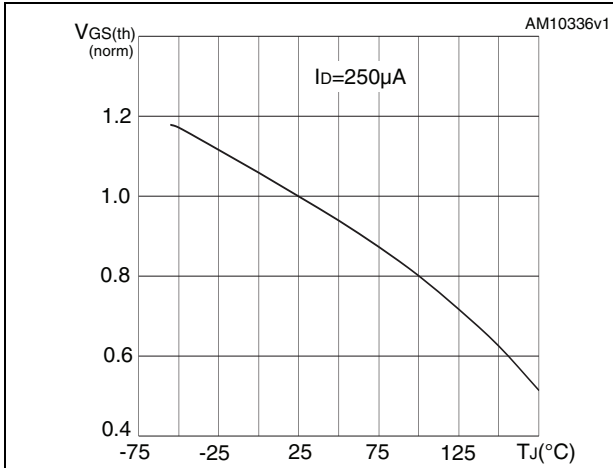


Figure 11. Normalized on-resistance vs temperature

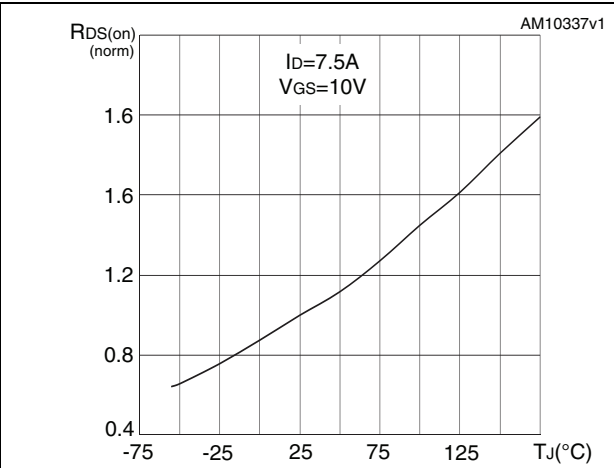
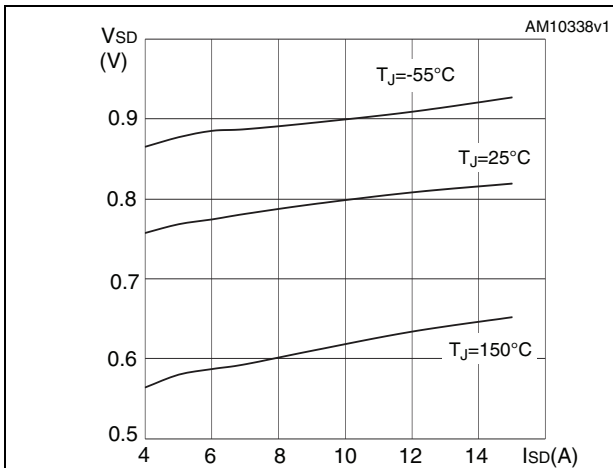


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

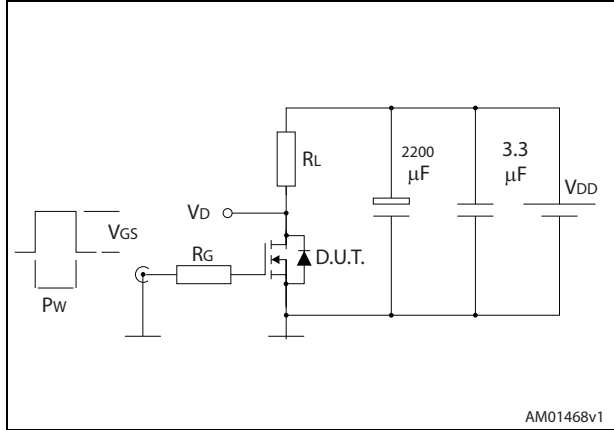


Figure 14. Gate charge test circuit

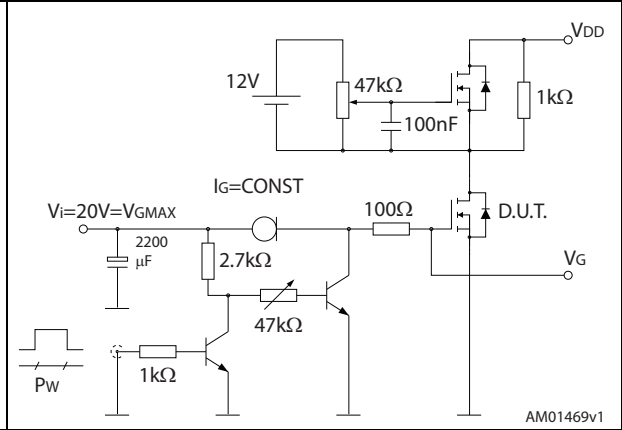


Figure 15. Test circuit for inductive load switching and diode recovery times

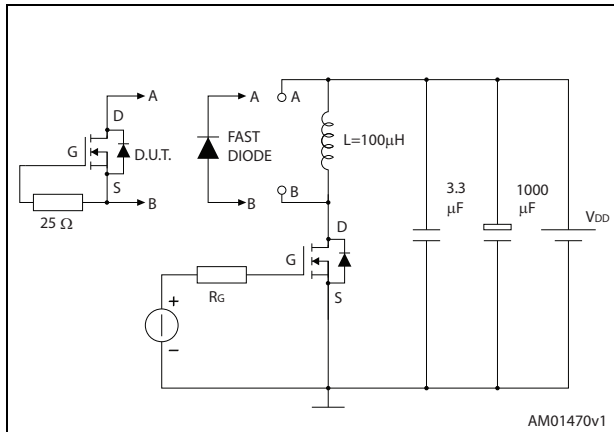


Figure 16. Unclamped inductive load test circuit

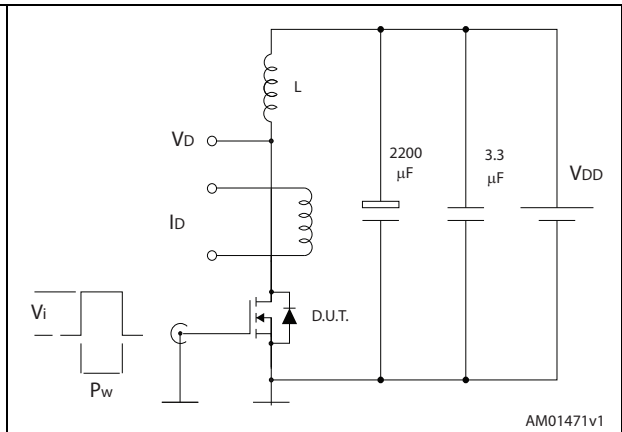


Figure 17. Unclamped inductive waveform

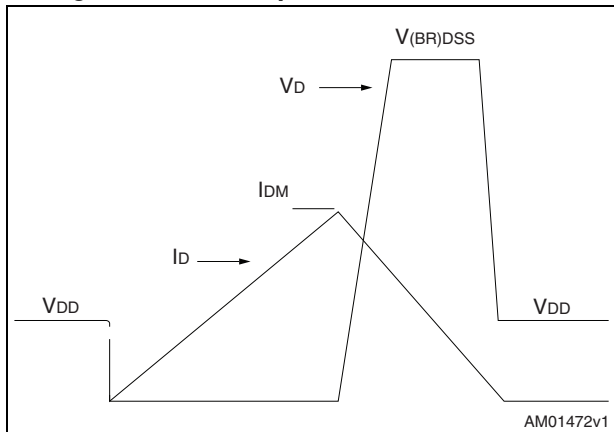
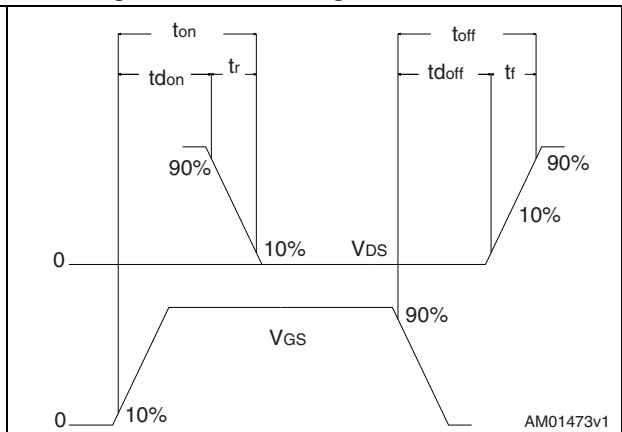


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 19. PowerFLAT™ 5x6 type S-R drawing

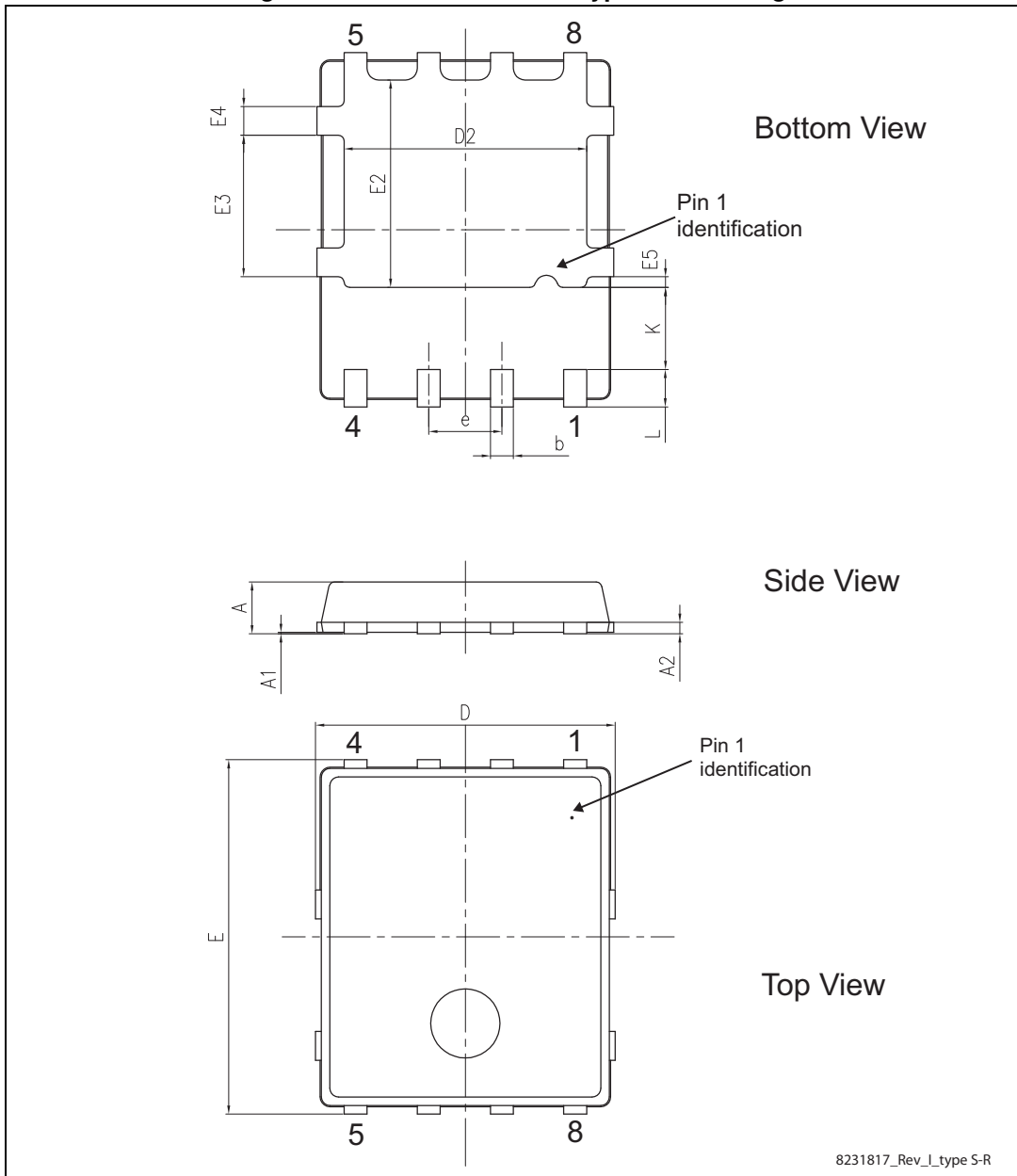
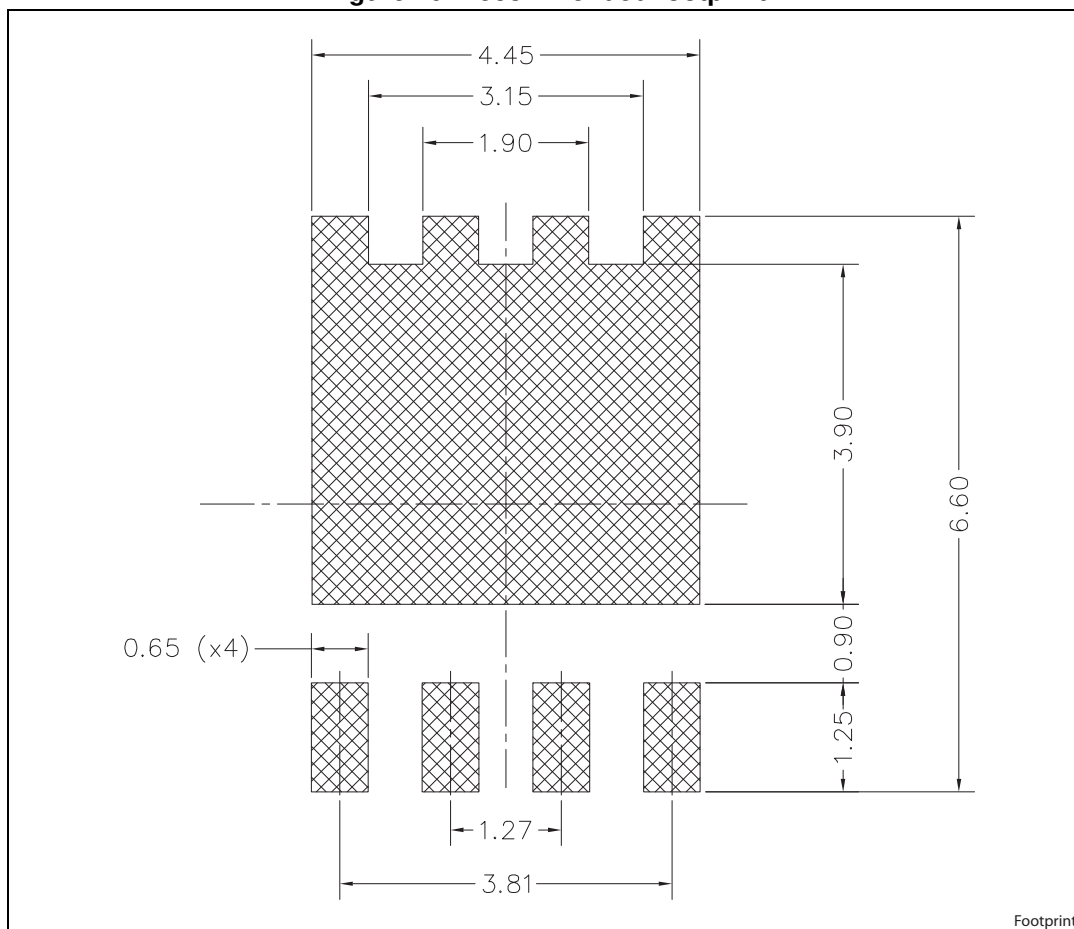


Table 8. PowerFLAT 5x6 type S-R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
D2	4.11		4.31
E	5.95	6.15	6.35
e		1.27	
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
K	1.275		1.575
L	0.60		0.80

Figure 20. Recommended footprint



Note: All dimensions are in mm

5 Packaging mechanical data

Figure 21. PowerFLAT™ 5x6 tape^(a)

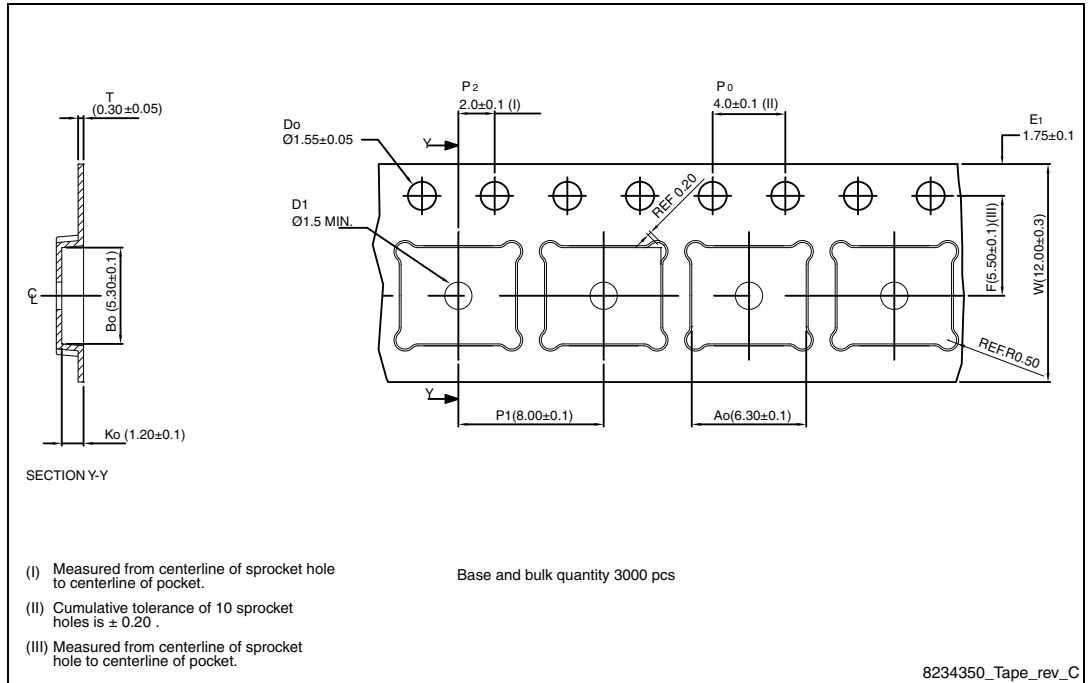
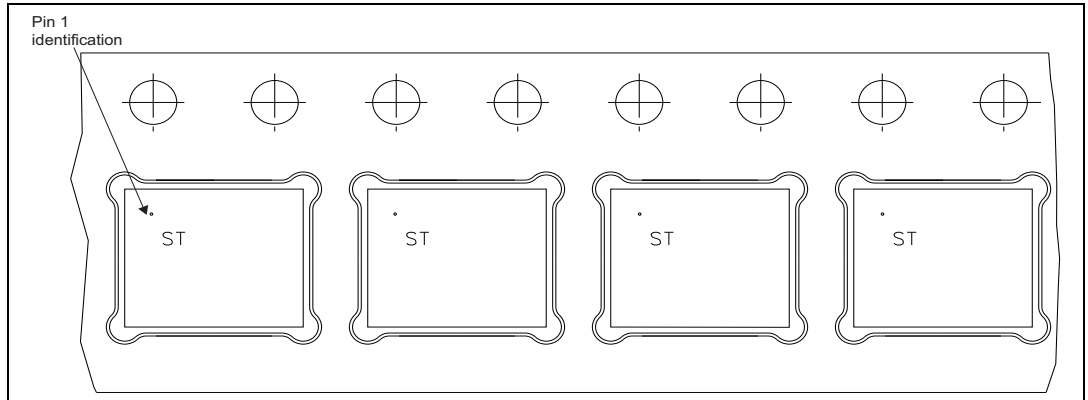
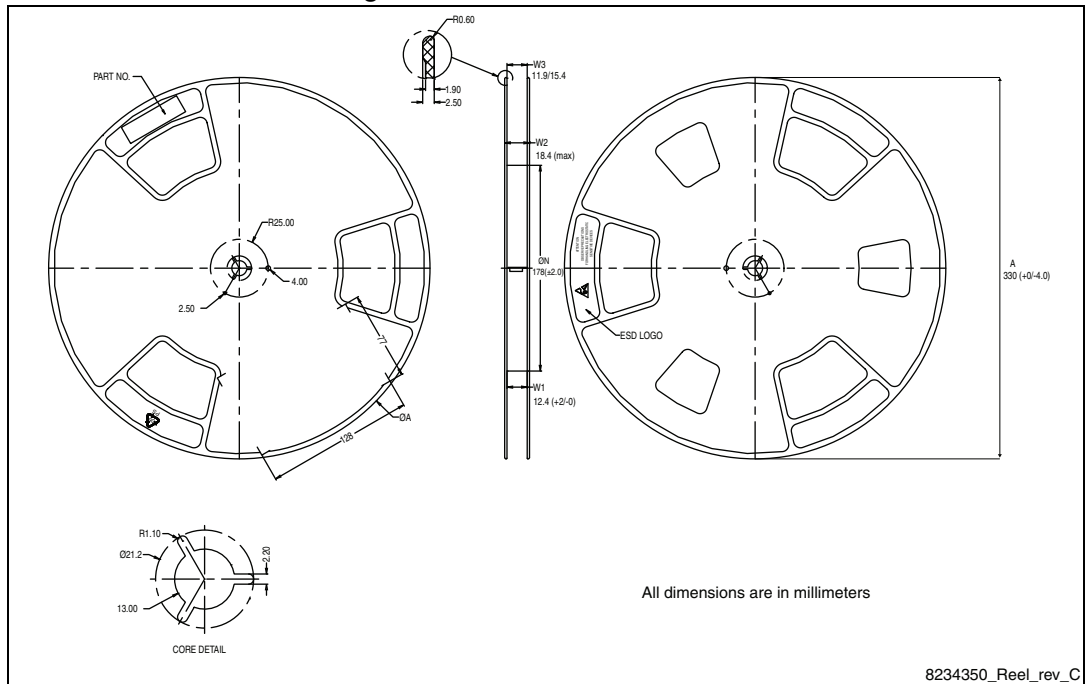


Figure 22. PowerFLAT™ 5x6 package orientation in carrier tape.



a. All dimensions are in millimeters.

Figure 23. PowerFLAT™ 5x6 reel



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
24-Jan-2011	1	First release.
01-Jul-2011	2	Document status promoted from preliminary data to datasheet.
27-Apr-2012	3	Added E_{AS} value in Table 2: Absolute maximum ratings . Updated Table 3: Thermal resistance , Table 4: On/off states , Table 5: Dynamic and Table 7: Source drain diode . Minor text changes.
13-Feb-2013	4	– Added: Section 5: Packaging mechanical data . – Updated Section 4: Package mechanical data .
25-Jul-2014	5	– Modified: title, features and description in cover page – Modified: I_{SD} and I_{SDM} max values in Table 7 – Updated: Figure 2 and 3 – Updated: Figure 13 , 14 , 15 and 16 – Updated: Section 4: Package mechanical data – Minor text changes

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2014 STMicroelectronics – All rights reserved