



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

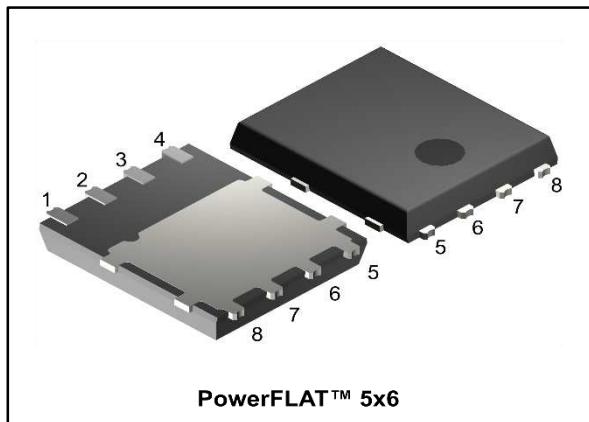
Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: [info@chipsmall.com](mailto:info@chipsmall.com) Web: [www.chipsmall.com](http://www.chipsmall.com)

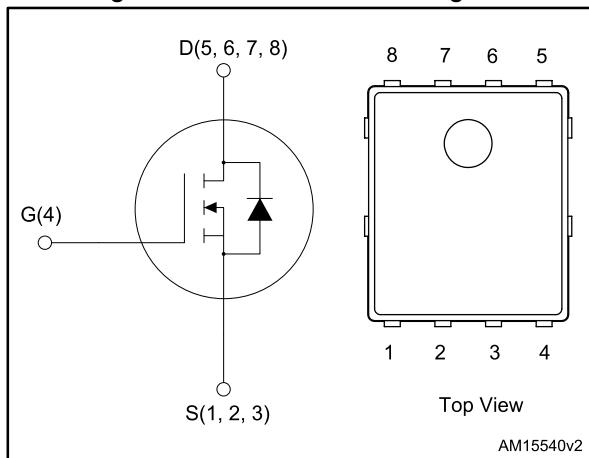
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

## Automotive-grade dual N-channel 30 V, 4.5 mΩ typ., 80 A STripFET™ H5 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data



**Figure 1: Internal schematic diagram**



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STL66N3LLH5	30 V	5.8 mΩ	80 A

- Designed for automotive applications and AEC-Q101 qualified
- Low on-resistance R<sub>DS(on)</sub>
- High avalanche ruggedness
- Low gate drive power loss
- Wettable flank package

### Applications

- Switching applications
- Automotive

### Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™ H5 technology. The device has been optimized to achieve very low on-state resistance, contributing to a FoM that is among the best in its class.

**Table 1: Device summary**

Order code	Marking	Package	Packing
STL66N3LLH5	66N3LLH5	PowerFLAT™ 5x6	Tape and reel

## Contents

<b>1</b>	<b>Electrical ratings .....</b>	<b>3</b>
<b>2</b>	<b>Electrical characteristics .....</b>	<b>4</b>
2.1	Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits .....</b>	<b>9</b>
<b>4</b>	<b>Package information .....</b>	<b>10</b>
4.1	PowerFLAT™ 5X6 package information .....	10
4.2	PowerFLAT™ 5X6 packing information .....	12
<b>5</b>	<b>Revision history .....</b>	<b>14</b>

# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	30	V
$V_{GS}$	Gate-source voltage	$\pm 22$	V
$I_D^{(1)}$	Drain current (continuous) at $T_{case} = 25^\circ C$	80	A
	Drain current (continuous) at $T_{case} = 100^\circ C$	57	
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25^\circ C$	21	A
	Drain current (continuous) at $T_{pcb} = 100^\circ C$	14.5	
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	84	A
$P_{TOT}^{(1)}$	Total dissipation at $T_{case} = 25^\circ C$	72	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25^\circ C$	4.8	
$T_J$	Operating junction temperature range	-55 to 175	$^\circ C$
$T_{stg}$	Storage temperature range		

## Notes:

(1) This value is rated according to  $R_{thj-c}$

(2) This value is rated according to  $R_{thj-pcb}$

(3) Pulse width is limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.08	$^\circ C/W$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	

## Notes:

(1) When mounted on a 1-inch<sup>2</sup> FR-4, 2 Oz copper board,  $t < 10$  s.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AV}$	Avalanche current, not repetitive	10.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25^\circ C$ , $I_D = I_{AV}$ , $V_{DD} = 24$ V)	180	mJ

## 2 Electrical characteristics

( $T_{case} = 25^\circ C$  unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 V, I_D = 250 \mu A$	30			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0 V, V_{DS} = 30 V$			1	$\mu A$
		$V_{GS} = 0 V, V_{DS} = 30 V, T_C = 125^\circ C$			10	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0 V, V_{GS} = \pm 22 V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1		3	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10 V, I_D = 10.5 A$		4.5	5.8	$m\Omega$
		$V_{GS} = 4.5 V, I_D = 10.5 A$		6	7.5	

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V$	-	1500	-	pF
$C_{oss}$	Output capacitance		-	295	-	
$C_{rss}$	Reverse transfer capacitance		-	39	-	
$Q_g$	Total gate charge	$V_{DD} = 15 V, I_D = 21 A, V_{GS} = 4.5 V$ (see <i>Figure 14: "Test circuit for gate charge behavior"</i> )	-	12	-	nC
$Q_{gs}$	Gate-source charge		-	4	-	
$Q_{gd}$	Gate-drain charge		-	4.7	-	

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15 V, I_D = 10.5 A, R_G = 4.7 \Omega, V_{GS} = 10 V$ (see <i>Figure 13: "Test circuit for resistive load switching times"</i> and )	-	9.3	-	ns
$t_r$	Rise time		-	14.5	-	
$t_{d(off)}$	Turn-off delay time		-	22.7	-	
$t_f$	Fall time		-	4.5	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		21	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		84	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0 \text{ V}$ , $I_{SD} = 19 \text{ A}$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 19 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ ,	-	25		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 25 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <i>Figure 15: "Test circuit for inductive load switching and diode recovery times"</i> )	-	17.5		nC
$I_{RRM}$	Reverse recovery current		-	1.4		A

**Notes:**

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

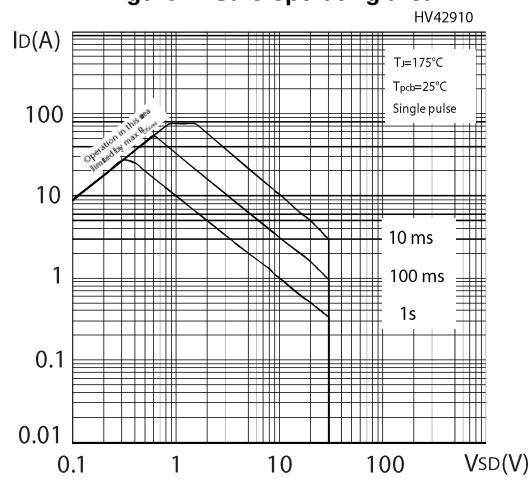


Figure 3: Thermal impedance

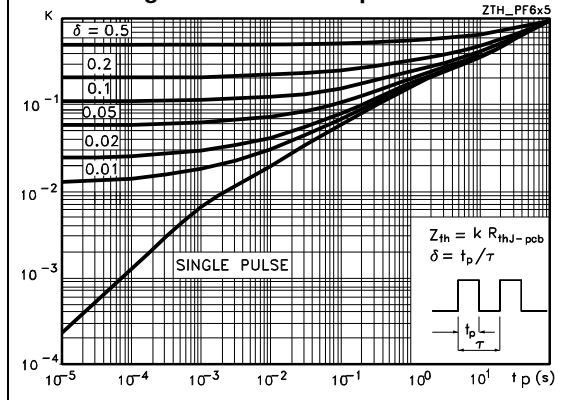


Figure 4: Output characteristics

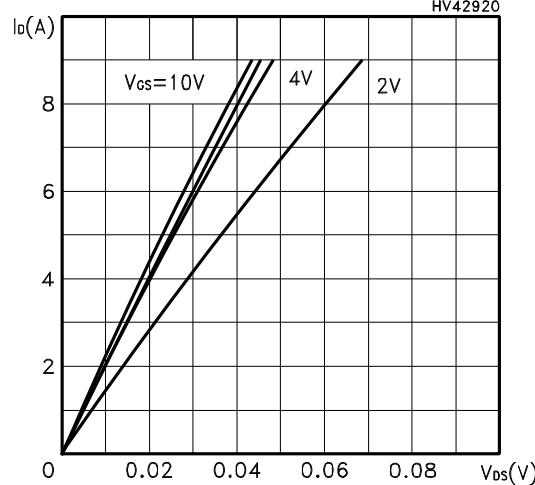
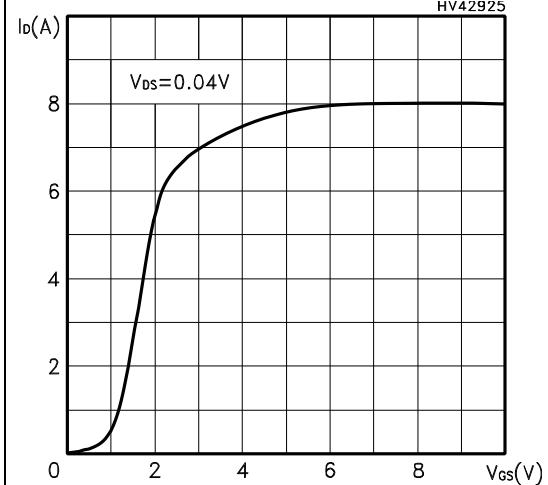
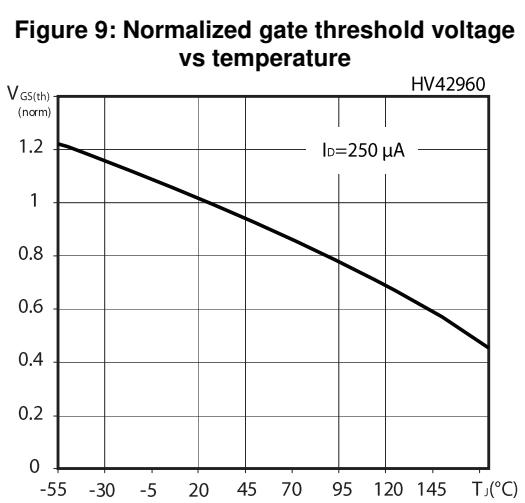
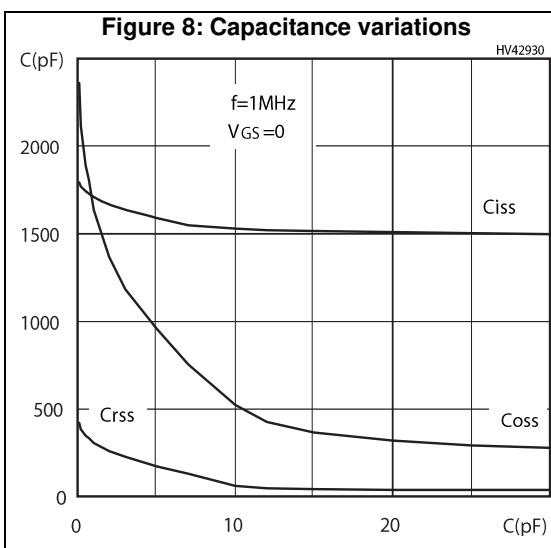
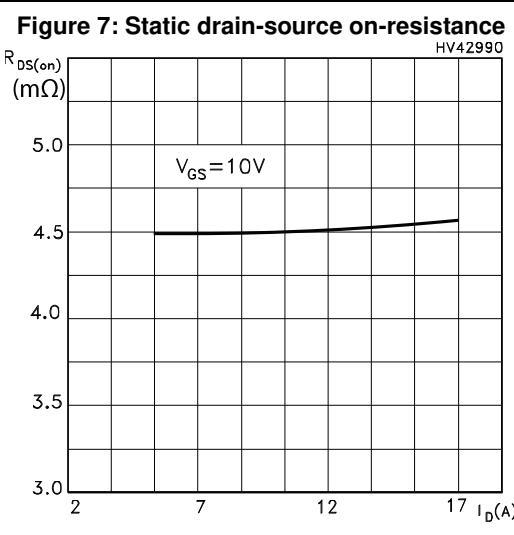
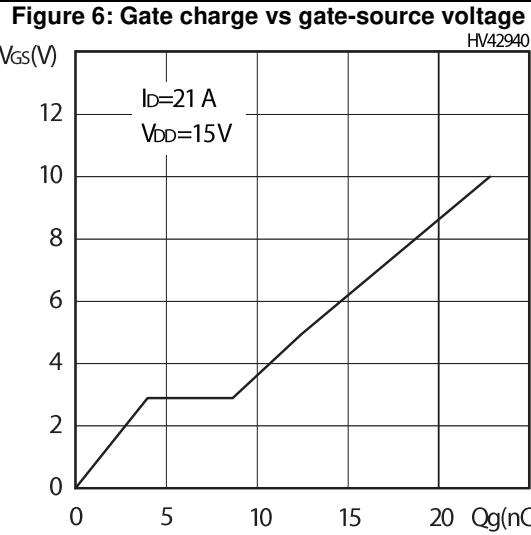
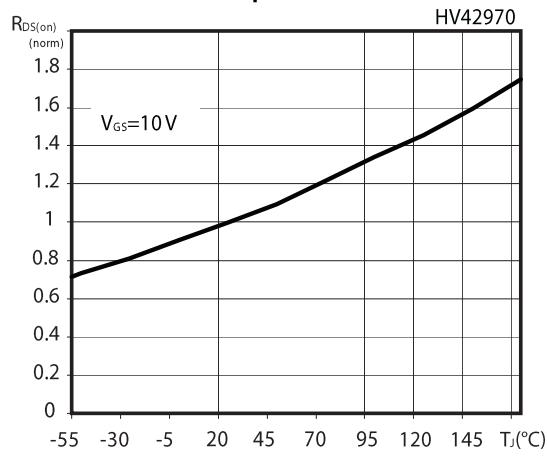
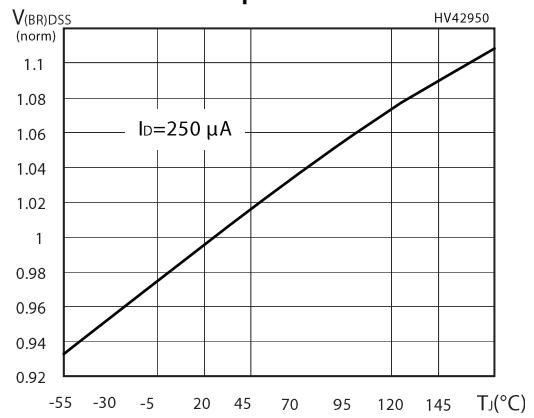
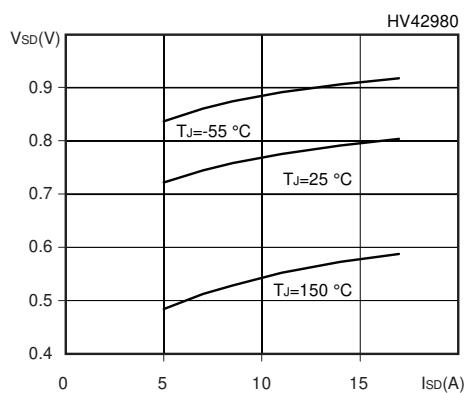


Figure 5: Transfer characteristics

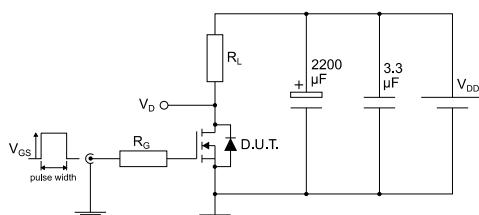




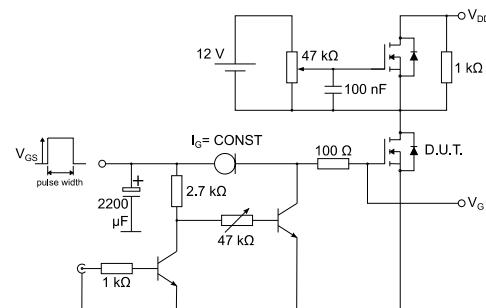
**Figure 10: Normalized on-resistance vs temperature****Figure 11: Normalized V(BR)DSS vs temperature****Figure 12: Source-drain diode forward characteristics**

### 3 Test circuits

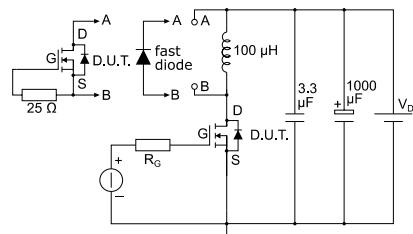
**Figure 13: Test circuit for resistive load switching times**



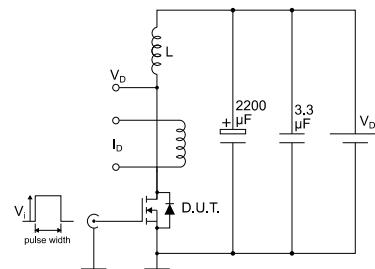
**Figure 14: Test circuit for gate charge behavior**



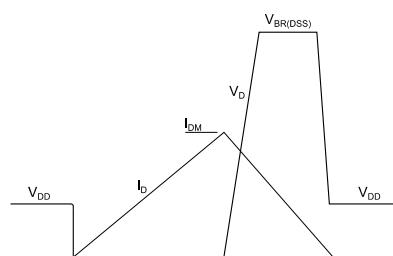
**Figure 15: Test circuit for inductive load switching and diode recovery times**



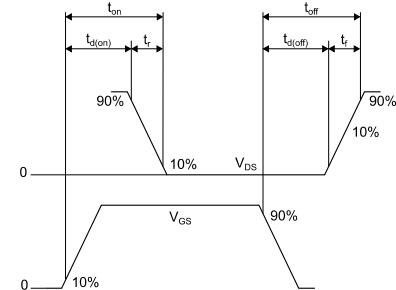
**Figure 16: Unclamped inductive load test circuit**



**Figure 17: Unclamped inductive waveform**



**Figure 18: Switching time waveform**



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 PowerFLAT™ 5X6 package information

Figure 19: PowerFLAT™ 5x6 WF type C package outline

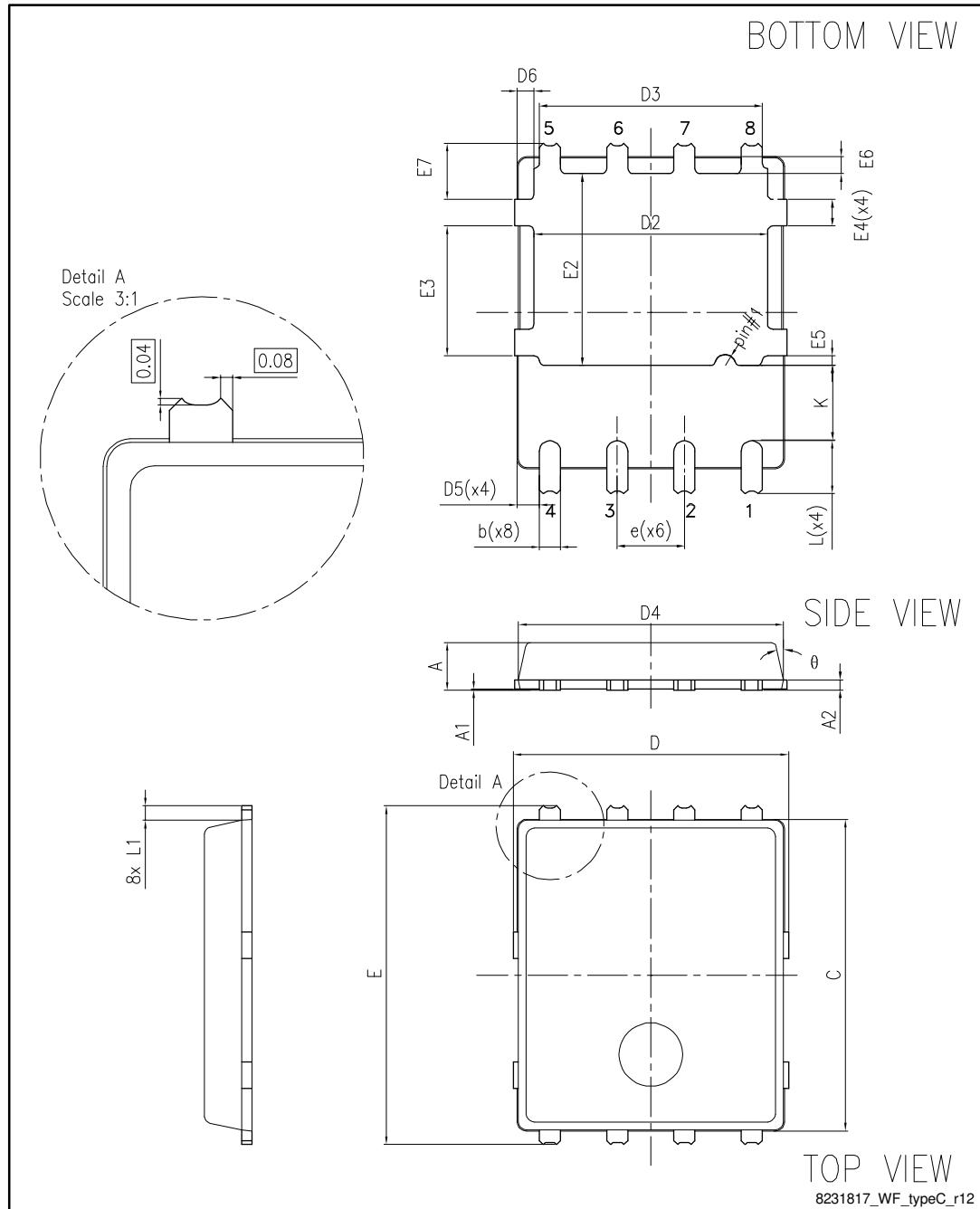
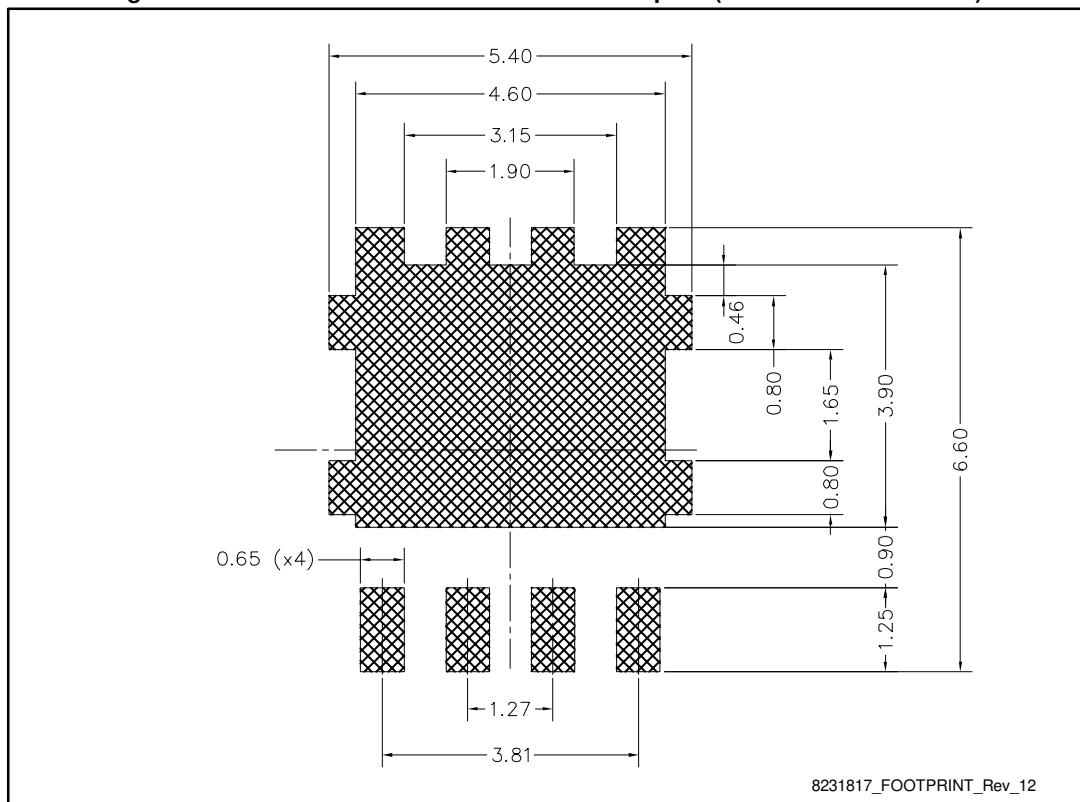


Table 9: PowerFLAT™ 5x6 WF type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.0	5.20
D5	0.25	0.4	0.55
D6	0.15	0.3	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.2	0.325	0.450
E7	0.85	1.00	1.15
K	1.05		1.35
L	0.90	1.00	1.10
L1	0.175	0.275	0.375
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



## 4.2 PowerFLAT™ 5X6 packing information

Figure 21: PowerFLAT™ 5x6 WF tape

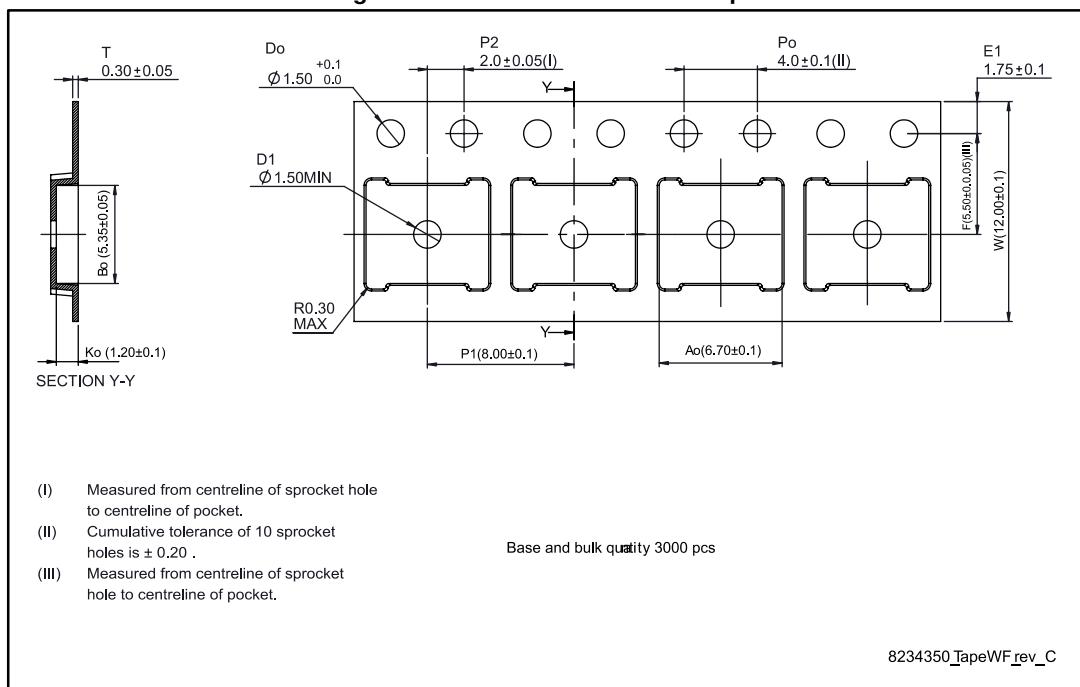


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

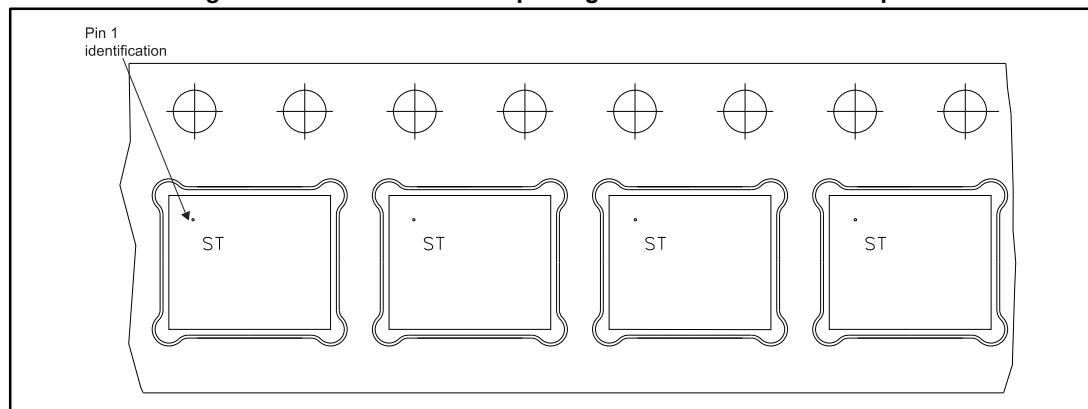
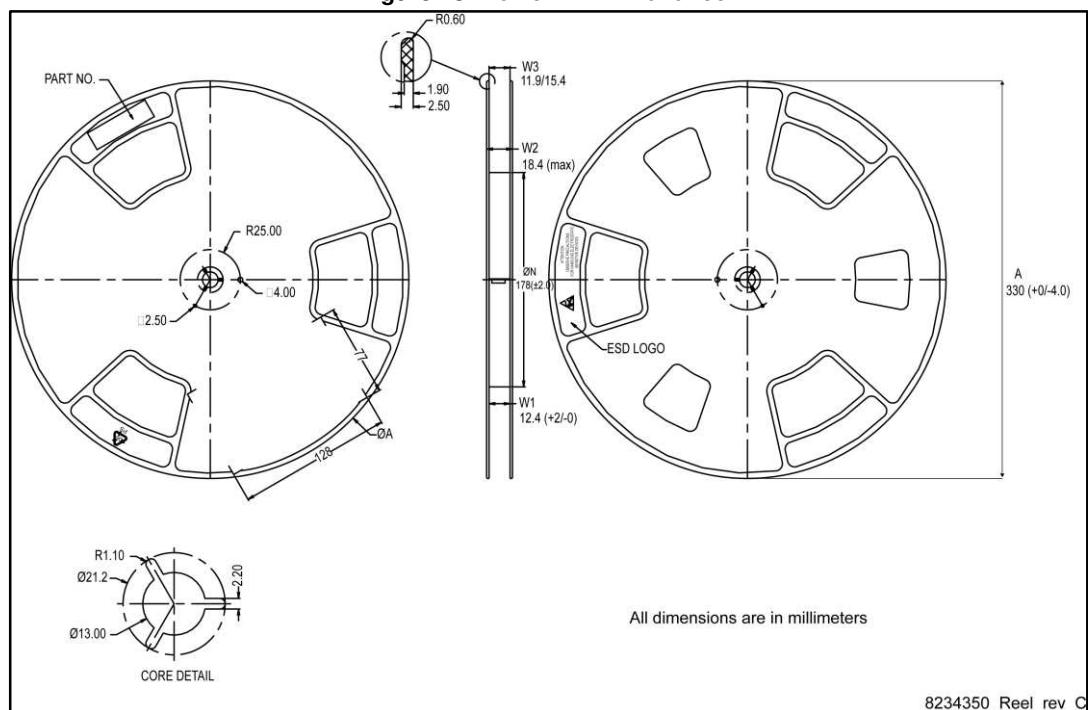


Figure 23: PowerFLAT™ 5x6 reel



## 5 Revision history

Table 10: Document revision history

Date	Revision	Changes
19-Oct-2011	1	First release.
17-dec-2014	2	Document status promoted from preliminary to production data. Updated title, features and description in cover page. Updated Chapter: Package mechanical data and Chapter: Packaging mechanical data.
22-Jan-2016	3	Updated title and features in cover page. Updated <a href="#">Section 4.1: "PowerFLAT™ 5X6 package information"</a> Minor text changes.

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved