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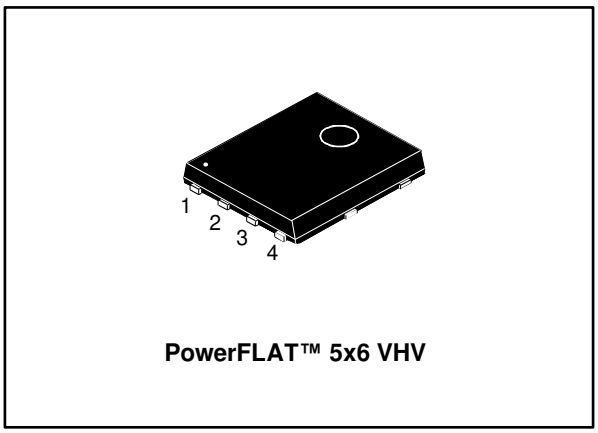
# STL7LN80K5

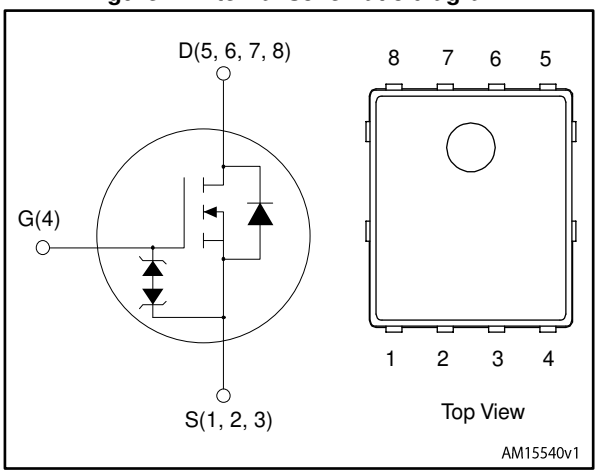
## N-channel 800 V, 0.95 Ω typ., 5 A MDmesh™ K5 Power MOSFET in a PowerFLAT™ 5x6 VHV package

Datasheet - production data




**PowerFLAT™ 5x6 VHV**

**Figure 1: Internal schematic diagram**




## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ |
|---|---|---|---|
| STL7LN80K5 | 800 V | 1.15 Ω | 5 A |

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best figure of merit (FoM)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

## Applications

- Switching applications

## Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

**Table 1: Device summary**

| Order code | Marking | Package | Packing |
|---|---|---|---|
| STL7LN80K5 | 7LN80K5 | PowerFLAT™ 5x6 VHV | Tape and reel |

# Contents

# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{GS}$ | Gate-source voltage | ± 30 | V |
| $I_D$ (1) | Drain current (continuous) at $T_C$ = 25 °C | 5 | A |
| $I_D$ (1) | Drain current (continuous) at $T_C$ = 100 °C | 3.4 | A |
| $I_D$ (2) | Drain current (pulsed) | 20 | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25 °C | 42 | W |
| dv/dt (3) | Peak diode recovery voltage slope | 4.5 | V/ns |
| dv/dt (4) | MOSFET dv/dt ruggedness | 50 | |
| $T_{stg}$ | Storage temperature range | - 55 to 150 | °C |
| $T_J$ | Operating junction temperature range | | |

**Notes:**

(1)Limited by maximum junction temperature.

(2)Pulse width limited by safe operating area

(3)$I_{SD}$ ≤ 5 A, di/dt 100 A/µs; $V_{DS}$ peak < $V_{(BR)DSS}$,$V_{DD}$= 640 V

(4)$V_{DS}$ ≤ 640 V

**Table 3: Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case | 3 | °C/W |
| $R_{thj\text{-}pcb}$ (1) | Thermal resistance junction-pcb | 59 | °C/W |

**Notes:**

(1)When mounted on 1inch² FR-4 board, 2 oz Cu.

**Table 4: Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$) | 1.5 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting Tj = 25 °C, $I_D$ = $I_{AR}$, $V_{DD}$ = 50 V) | 200 | mJ |

# 2 Electrical characteristics

$T_C$ = 25 °C unless otherwise specified

**Table 5: On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0 V, $I_D$ = 1 mA | 800 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{GS}$ = 0 V, $V_{DS}$ = 800 V | | | 1 | µA |
| | | $V_{GS}$ = 0 V, $V_{DS}$ = 800 V, $T_C$ = 125 °C | | | 50 | µA |
| $I_{GSS}$ | Gate-body leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | | | ±10 | µA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ =100 µA | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 2.5 A | | 0.95 | 1.15 | Ω |

**Table 6: Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$= 100 V, f = 1 MHz, $V_{GS}$ = 0 V | - | 270 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 22 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 0.5 | - | pF |
| $C_{o(er)}$ (1) | Equivalent capacitance energy related | $V_{DS}$ = 0 to 640 V, $V_{GS}$ = 0 V | - | 17 | - | nC |
| $C_{o(tr)}$ (2) | Equivalent capacitance time related | | - | 48 | - | nC |
| $R_G$ | Intrinsic gate resistance | f = 1 MHz, $I_D$=0 A | - | 7.5 | - | Ω |
| $Q_g$ | Total gate charge | $V_{DD}$ = 640 V, $I_D$ = 5 A, $V_{GS}$ = 10 V (see *Figure 15: "Test circuit for gate charge behavior"*) | - | 12 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 2.6 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 8.6 | - | nC |

**Notes:**

(1)Energy related is defined as a constant equivalent capacitance giving the same stored energy as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$

(2)Time related is defined as a constant equivalent capacitance giving the same stored energy as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$

**Table 7: Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 400 V, $I_D$ = 2.5 A $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see *Figure 14: "Test circuit for resistive load switching times"* and *Figure 19: "Switching time waveform"*) | - | 9.3 | - | ns |
| $t_r$ | Rise time | | - | 6.7 | - | ns |
| $t_{d(off)}$ | Turn-off-delay time | | - | 23.6 | - | ns |
| $t_f$ | Fall time | | - | 17.4 | - | ns |

**Table 8: Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 5 | A |
| $I_{SDM}$ (1) | Source-drain current (pulsed) | | - | | 20 | A |
| $V_{SD}$ (2) | Forward on voltage | $I_{SD}$= 5 A, $V_{GS}$ = 0 V | - | | 1.6 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 5 A, di/dt = 100 A/µs, $V_{DD}$ = 60 V (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*) | - | 276 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 2.13 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 15.4 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 5 A, di/dt = 100 A/µs, $V_{DD}$ = 60 V, $T_j$ = 150 °C (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*) | - | 402 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 2.79 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 13.9 | | A |

**Notes:**

(1)Pulse width is limited by safe operating area

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

**Table 9: Gate-source Zener diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)GSO}$ | Gate-source breakdown voltage | $I_{GS}$ = ±1 mA, $I_D$ = 0 A | 30 | - | | V |

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection,thus eliminating the need for additional external componentry.

## 2.2 Electrical characteristics (curves)

**Figure 2: Safe operating area**

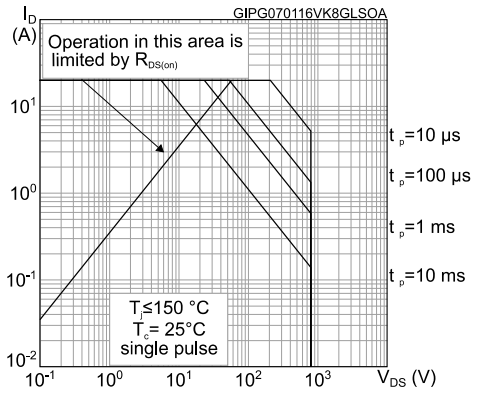



**Figure 3: Thermal impedance**

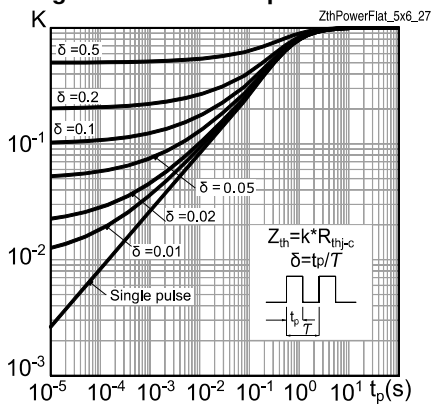



**Figure 4: Output characteristics**

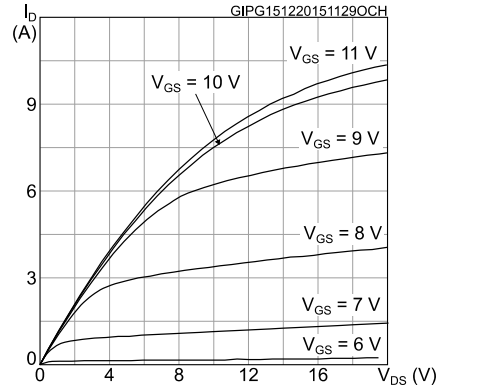



**Figure 5: Transfer characteristics**

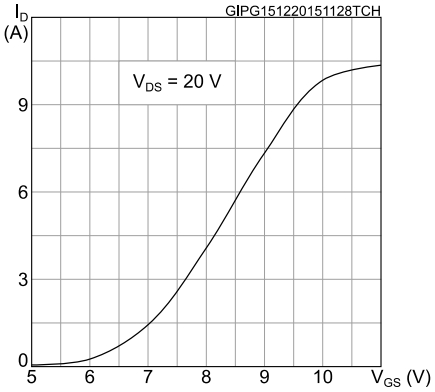



**Figure 6: Gate charge vs gate-source voltage**

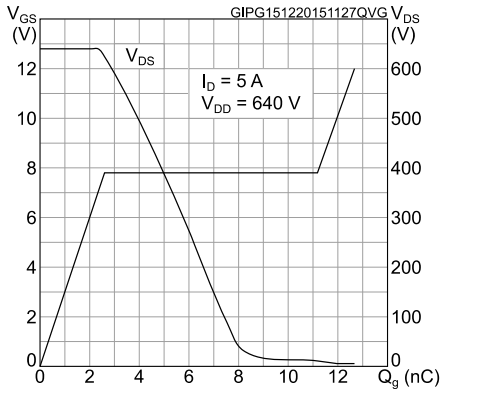



**Figure 7: Static drain-source on-resistance**

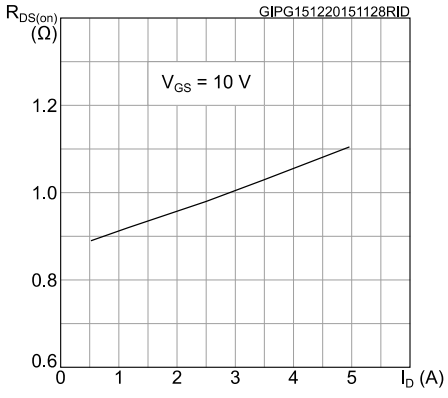


**Figure 8: Capacitance variations**

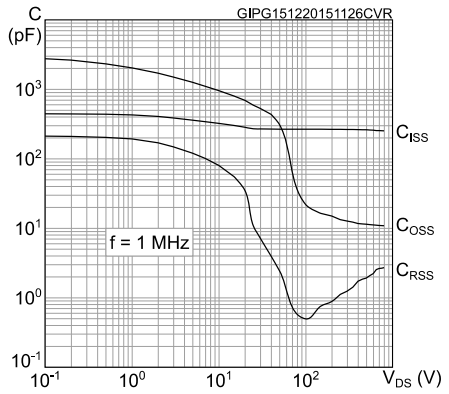



**Figure 9: Normalized gate threshold voltage vs temperature**

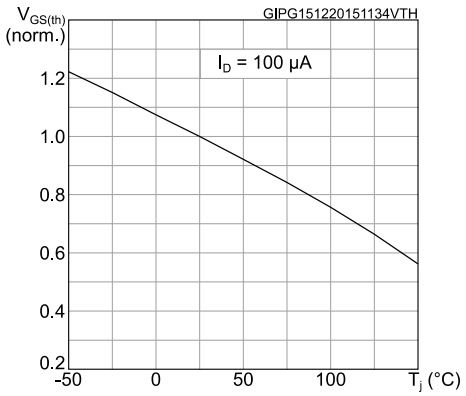



**Figure 10: Normalized $V_{(BR)DSS}$ vs temperature**

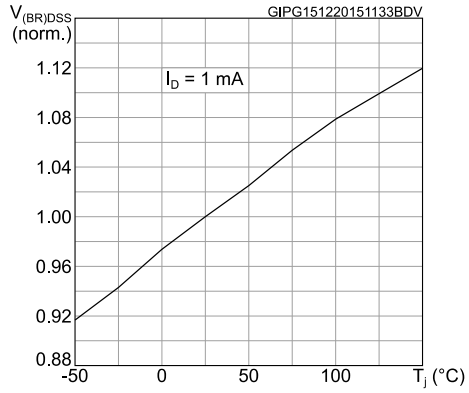



**Figure 11: Normalized on-resistance vs temperature**

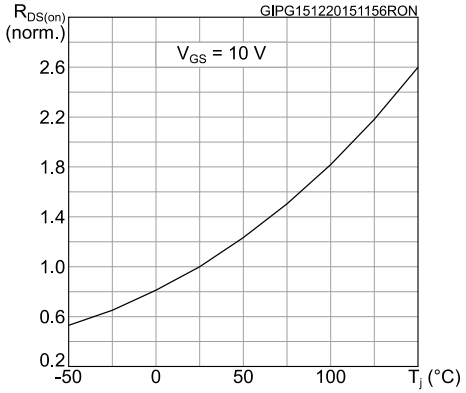



**Figure 12: Source-drain diode forward characteristics**

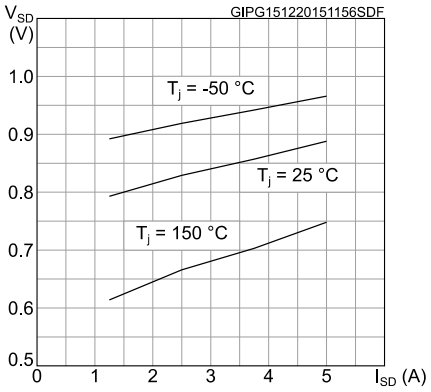
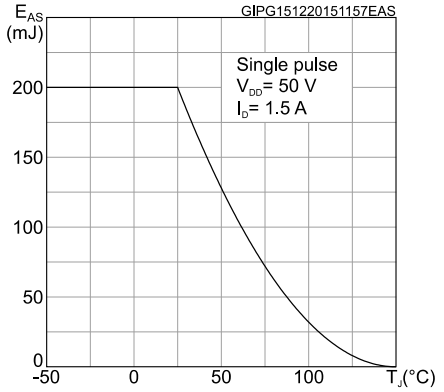



**Figure 13: Maximum avalanche energy vs starting $T_J$**



# 3 Test circuits

**Figure 14: Test circuit for resistive load switching times**

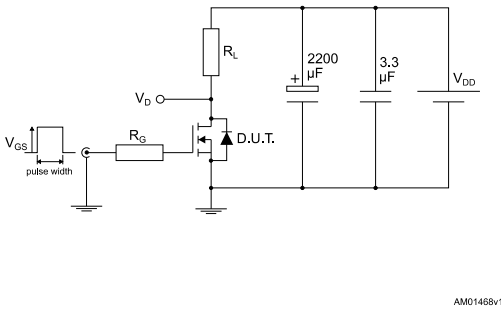



**Figure 15: Test circuit for gate charge behavior**

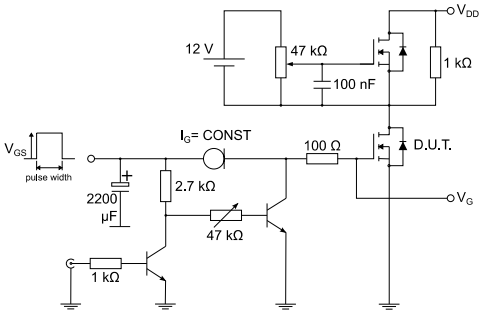



**Figure 16: Test circuit for inductive load switching and diode recovery times**

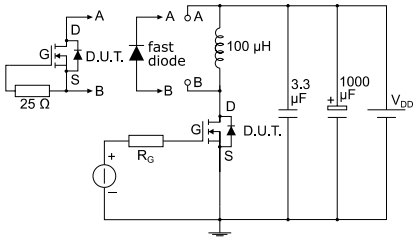



**Figure 17: Unclamped inductive load test circuit**

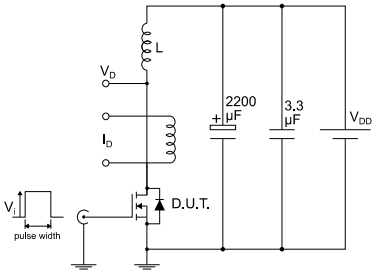



**Figure 18: Unclamped inductive waveform**

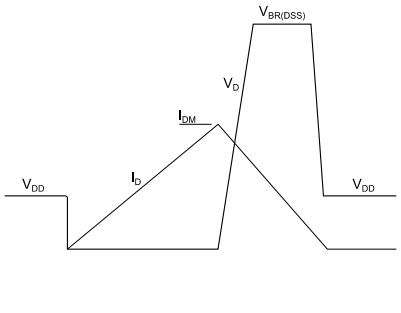
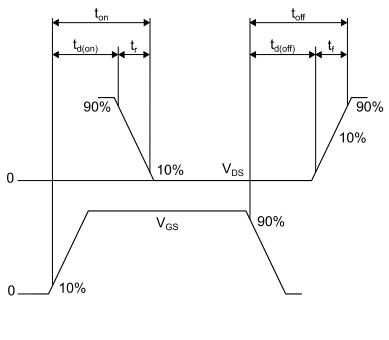



**Figure 19: Switching time waveform**



# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

## 4.1 PowerFLAT™ 5x6 VHV package information

**Figure 20: PowerFLAT™ 5x6 VHV Package outline**

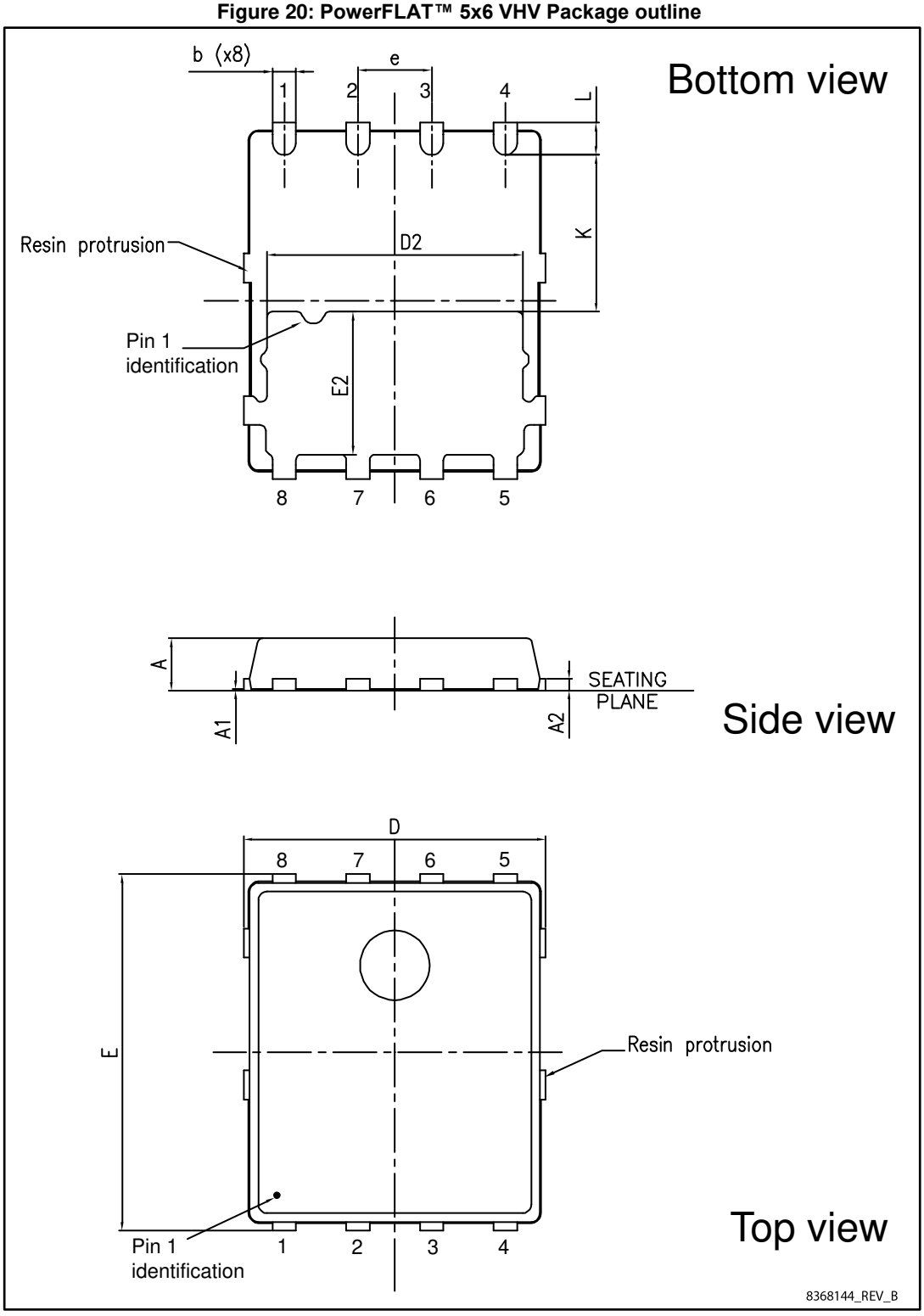
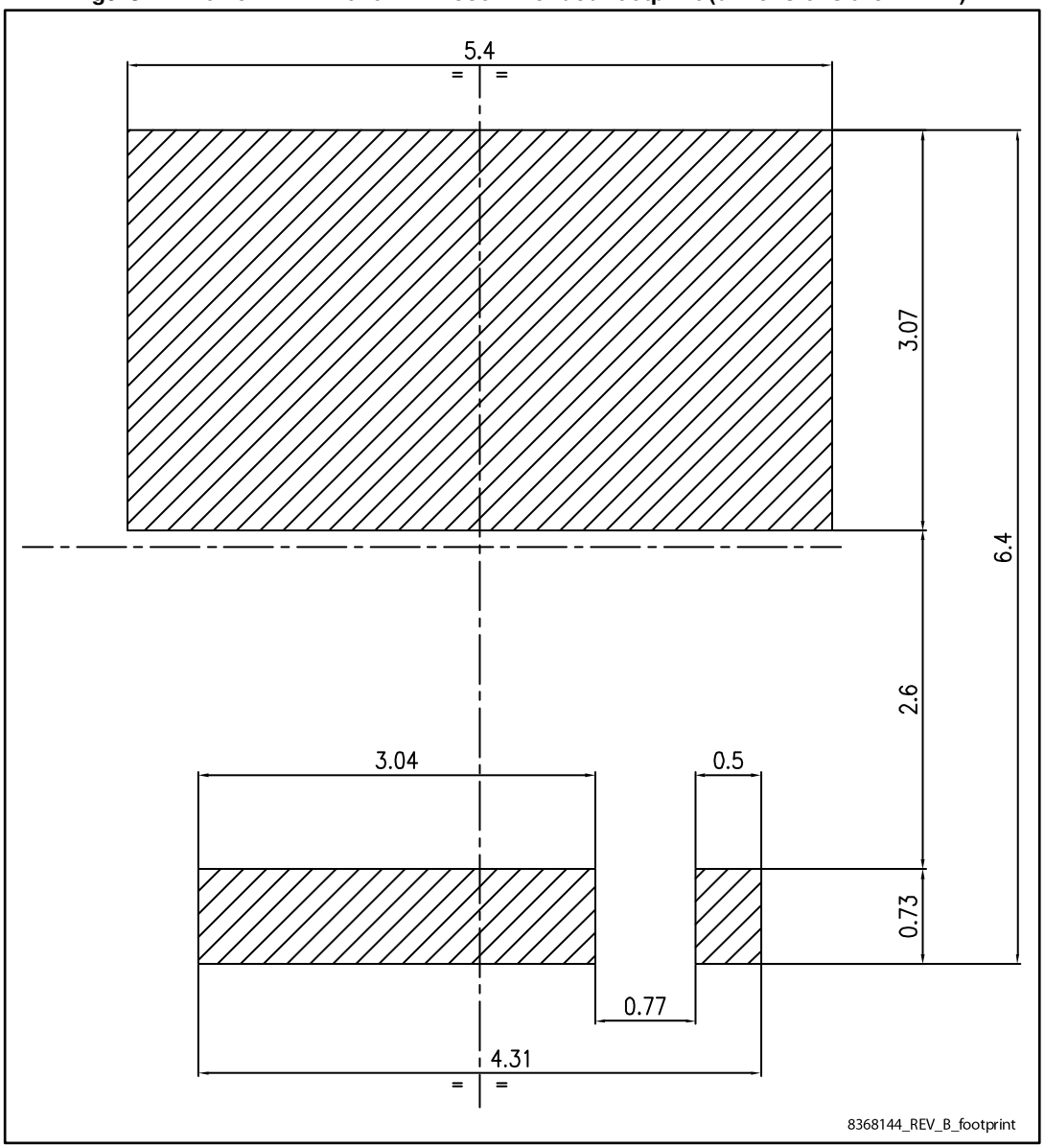


Table 10: PowerFLAT™ 5x6 VHV package mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.80 | | 1.00 |
| A1 | 0.02 | | 0.05 |
| A2 | | 0.25 | |
| b | 0.30 | | 0.50 |
| D | 5.00 | 5.20 | 5.40 |
| E | 5.95 | 6.15 | 6.35 |
| D2 | 4.30 | 4.40 | 4.50 |
| E2 | 2.40 | 2.50 | 2.60 |
| e | | 1.27 | |
| L | 0.50 | 0.55 | 0.60 |
| K | 2.60 | 2.70 | 2.80 |

Figure 21: PowerFLAT™ 5x6 VHV recommended footprint (dimensions are in mm)



## 4.2 PowerFLAT™ 5x6 packing information

**Figure 22: PowerFLAT™ 5x6 tape (dimensions are in mm)**

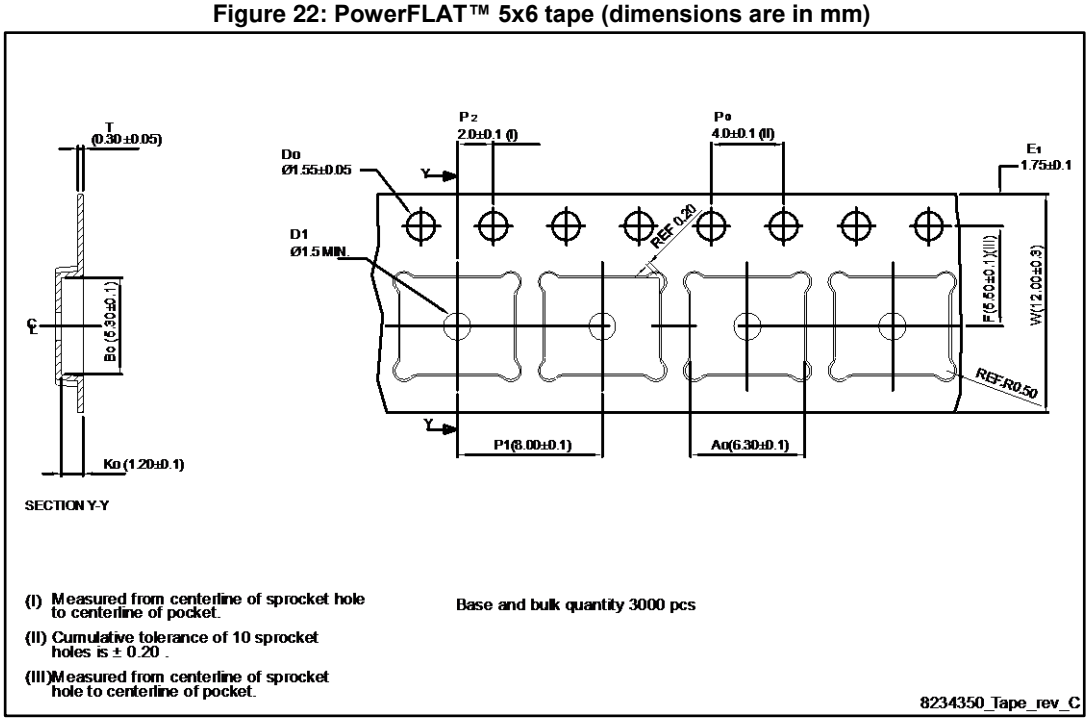



**Figure 23: PowerFLAT™ 5x6 package orientation in carrier tape**

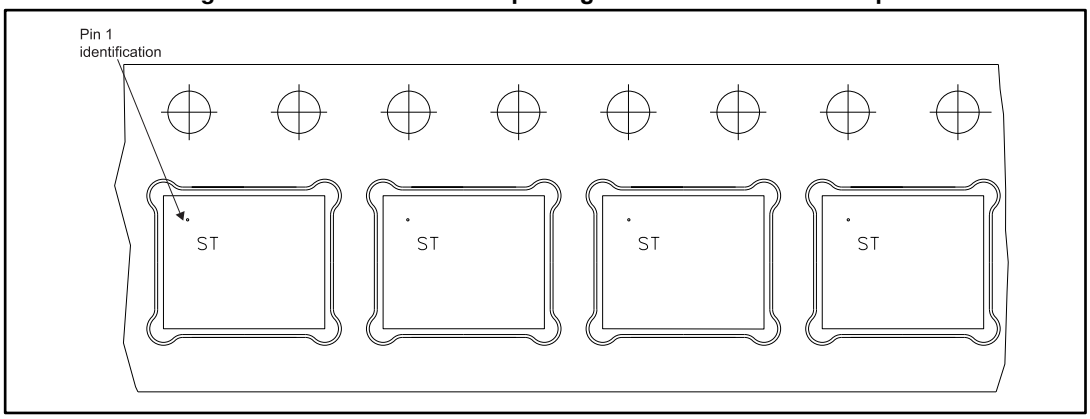
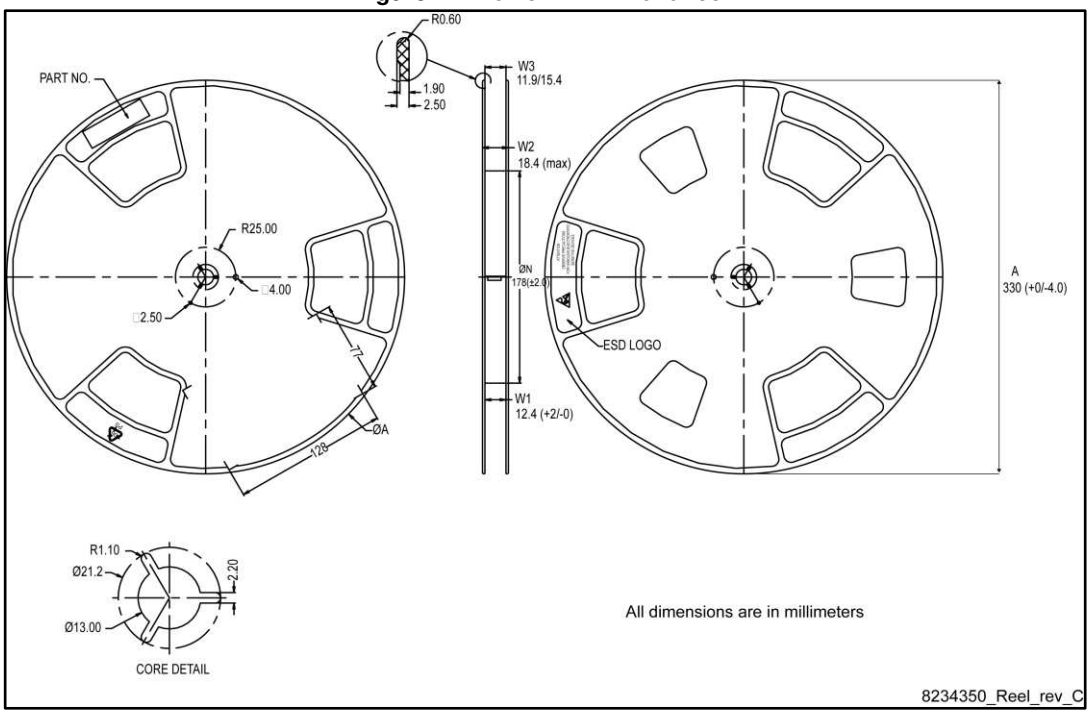


**Figure 24: PowerFLAT™ 5x6 reel**



# 5 Revision history

Table 11: Document revision history

| Date | Revision | Changes |
|---|---|---|
| 07-Jan-2016 | 1 | First release. |
| 26-Jan-2016 | 2 | Modified: *Table 2: "Absolute maximum ratings"*<br>Minor text changes |

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