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STL85N6F3

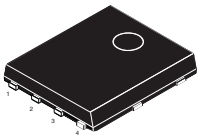
N-channel 60 V, 0.0057 Ω, 19 A PowerFLAT™ 5x6 STripFET™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STL85N6F3	60 V	< 0.0065 Ω	19 A (1)

1. The value is rated according $R_{thj\text{-}pcb}$

- Extremely low on-resistance $R_{DS(on)}$
- 100% avalanche tested



PowerFLAT™ 5x6

Applications

- Switching applications

Description

This N-channel enhancement mode Power MOSFET benefits from the latest refinement of STMicroelectronics' unique “single feature size“ strip-based process, which decreases the critical alignment steps to offer exceptional manufacturing reproducibility. The result is a transistor with extremely high packing density for low on-resistance, rugged avalanche characteristics and low gate charge.

Figure 1. Internal schematic diagram

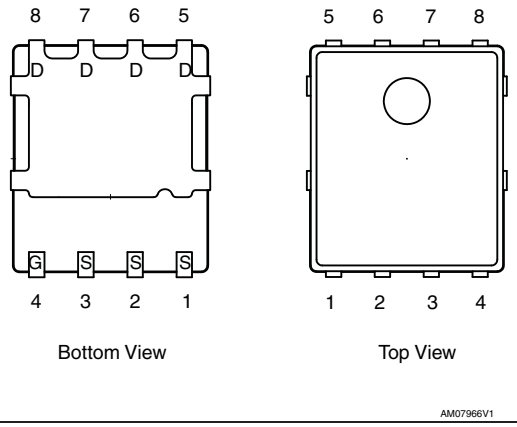


Table 1. Device summary

Order code	Marking	Package	Packaging
STL85N6F3	85N6F3	PowerFLAT™ 5x6	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	60	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25°C	19	A
I_D (1)	Drain current (continuous) at T_C = 100°C	12	A
I_{DM} (2)	Drain current (pulsed)	76	A
I_D (3)	Drain current (continuous) at T_C=25°C	85	A
I_D (3)	Drain current (continuous) at T_C = 100°C	54	A
P_{TOT} (1)	Total dissipation at T_C = 25°C	4	W
P_{TOT} (3)	Total dissipation at T_C = 25°C	80	W
	Derating factor	0.03	W/°C
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. The value is rated according $R_{thj\text{-}pcb}$
2. Pulse width limited by safe operating area
3. The value is rated according $R_{thj\text{-}c}$

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case (drain) (steady state)	1.56	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-ambient	31.3	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10sec

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	60			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating @125°C			10 100	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±200	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2			V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 8.5A		0.0057	0.0065	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	3050 659 38	-	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=30 V, I_D = 19 A V_{GS} =10 V *(see Figure 14)*	-	49.8 14.6 12	-	nC nC nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 30 V, I_D= 9.5 A,		21.8		ns
t_r	Rise time	R_G= 4.7 Ω, V_{GS} = 10 V	-	14.3	-	ns
$t_{d(off)}$	Turn-off delay time	*(see Figure 13)*		38.4		ns
t_f	Fall time			7.1		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		19	A
I_{SDM}(1)	Source-drain current (pulsed)		-		76	A
V_{SD}(2)	Forward on voltage	I_{SD} = 19 A, V_{GS}=0	-		1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 19 A,		53.6		ns
Q_{rr}	Reverse recovery charge	di/dt = 100 A/µs,	-	120.1		nC
I_{RRM}	Reverse recovery current	V_{DD}= 48 V, Tj=150°C		4.5		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

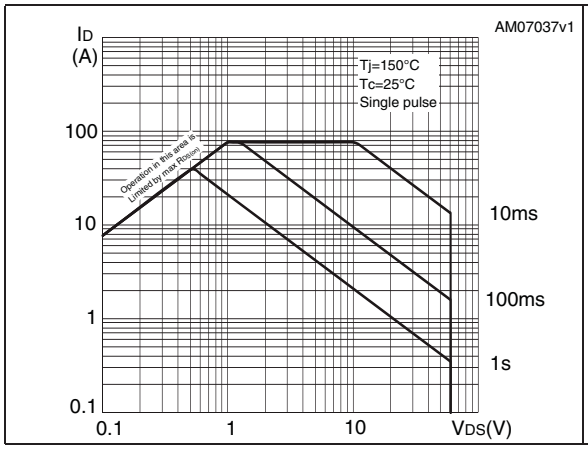


Figure 3. Thermal impedance

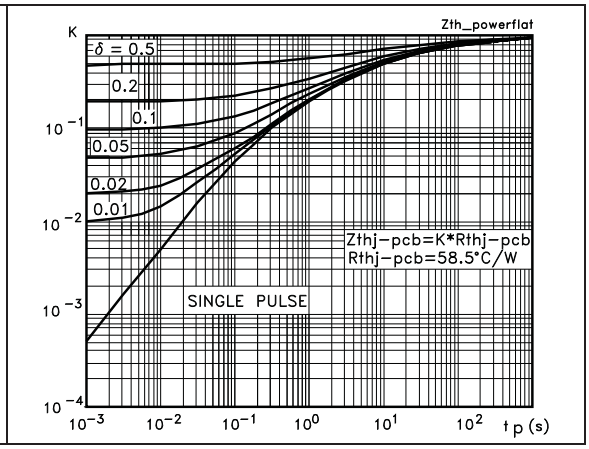


Figure 4. Output characteristics

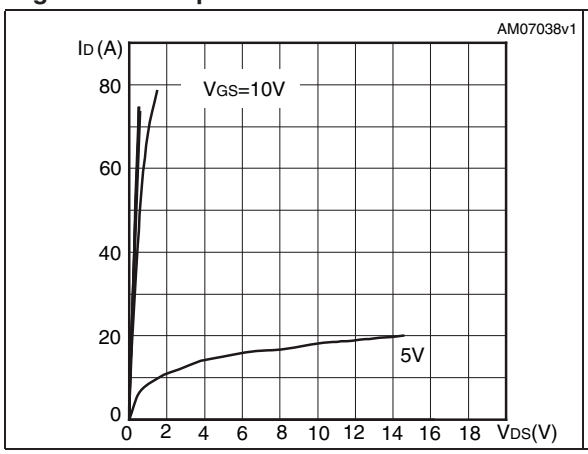


Figure 5. Transfer characteristics

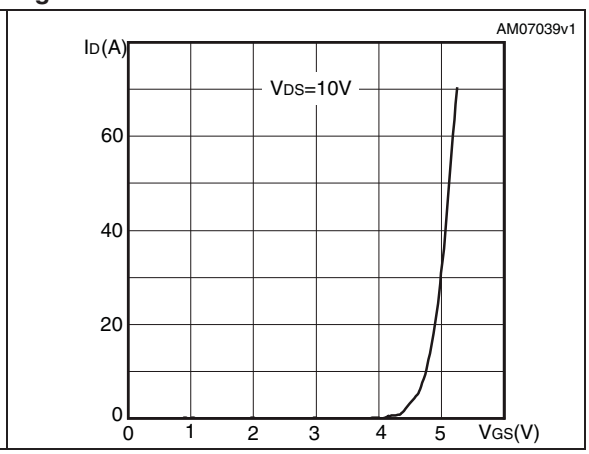


Figure 6. Normalized B_{VDSS} vs temperature

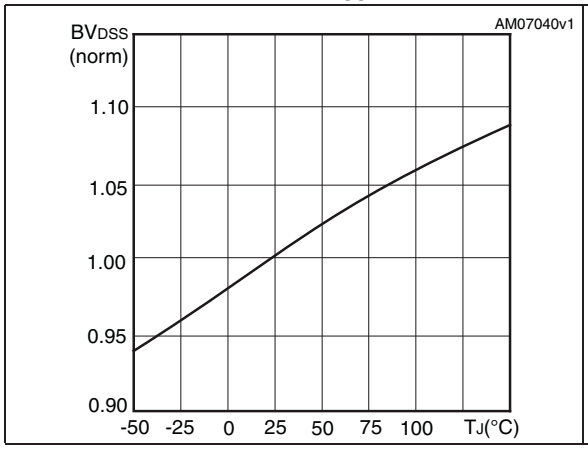


Figure 7. Static drain-source on resistance

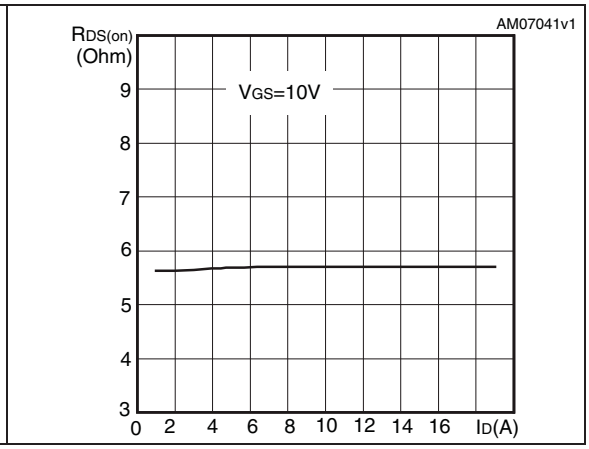


Figure 8. Gate charge vs gate-source voltage

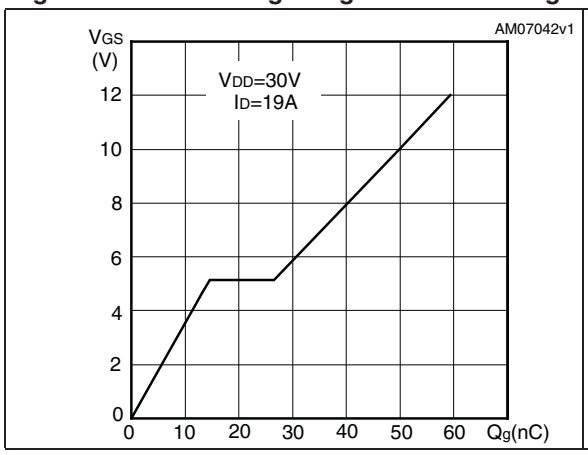


Figure 9. Capacitance variations

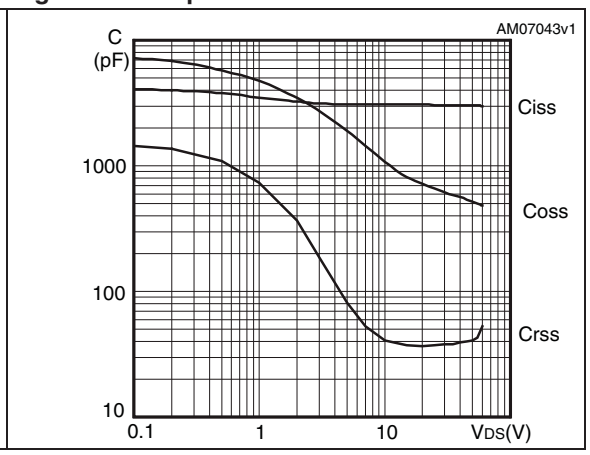


Figure 10. Normalized gate threshold voltage vs temperature

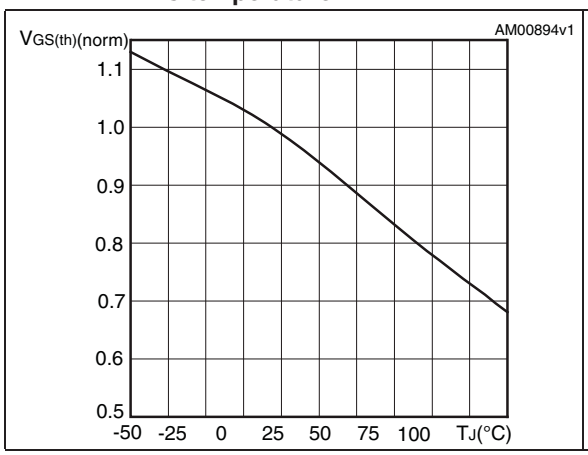


Figure 11. Normalized on resistance vs temperature

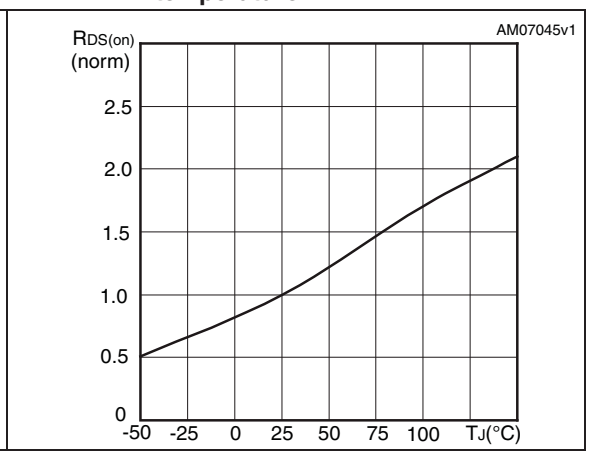
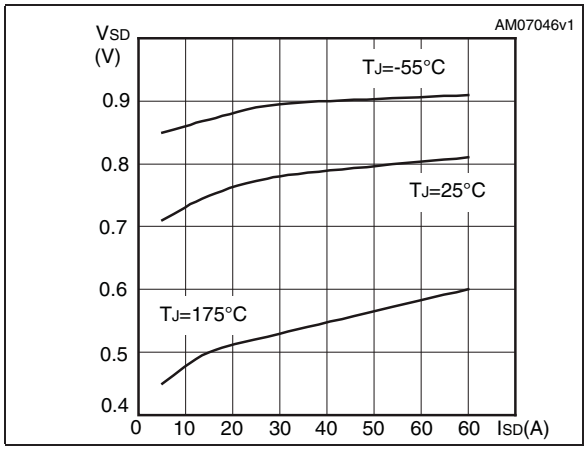


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

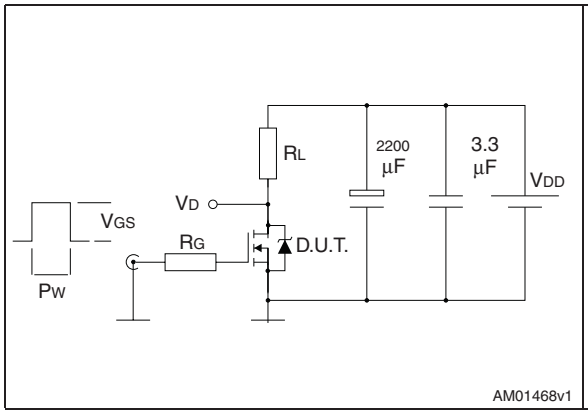


Figure 14. Gate charge test circuit

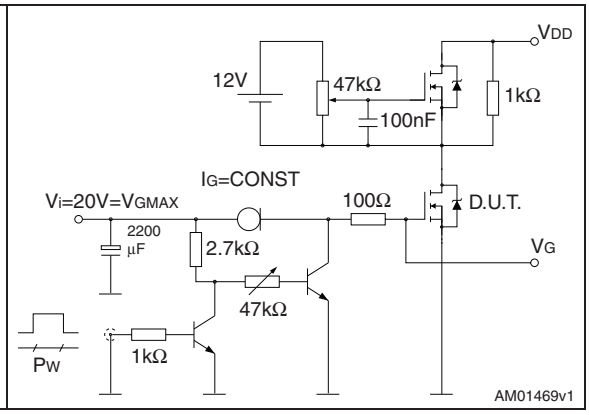


Figure 15. Test circuit for inductive load switching and diode recovery times

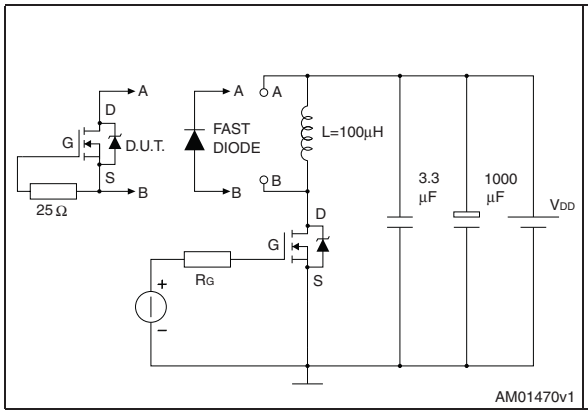


Figure 16. Unclamped inductive load test circuit

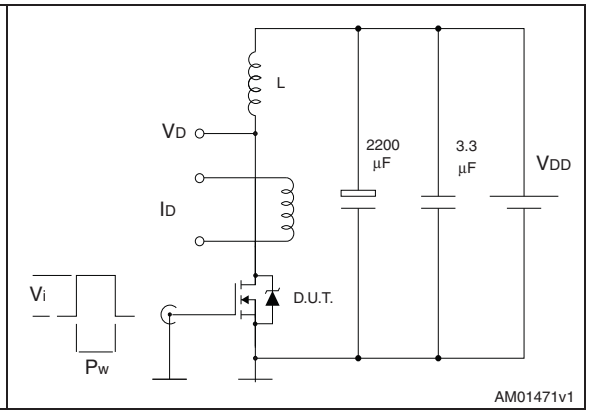


Figure 17. Unclamped inductive waveform

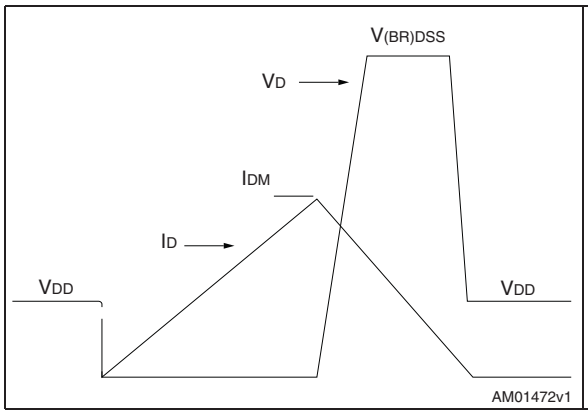
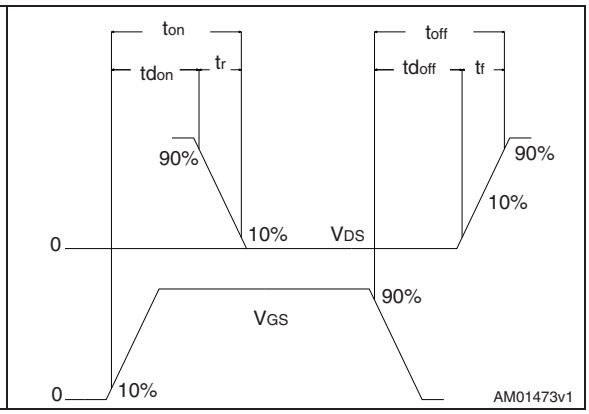


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ 5x6 type S-C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
e1		0.65	
L	0.715		1.015
K	1.05		1.35

Figure 19. PowerFLAT™ 5x6 type S-C drawing

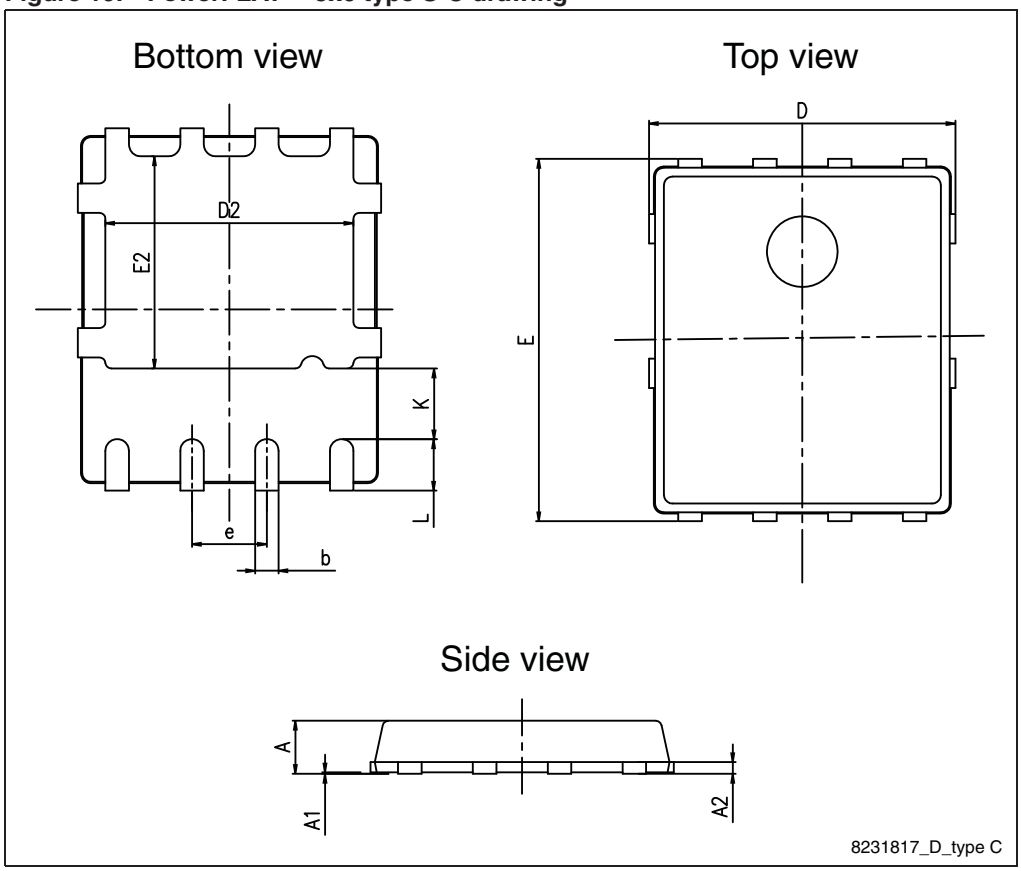


Table 9. PowerFLAT™ 5x6 type C-B mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.83	0.93
A1	0	0.02	0.05
A3		0.20	
b	0.35	0.40	0.47
D		5.00	
D1		4.75	
D2	4.15	4.20	4.25
E		6.00	
E1		5.75	
E2	3.43	3.48	3.53
E4	2.58	2.63	2.68
e		1.27	
L	0.70	0.80	0.90

Figure 20. PowerFLAT™ 5x6 type C-B drawing

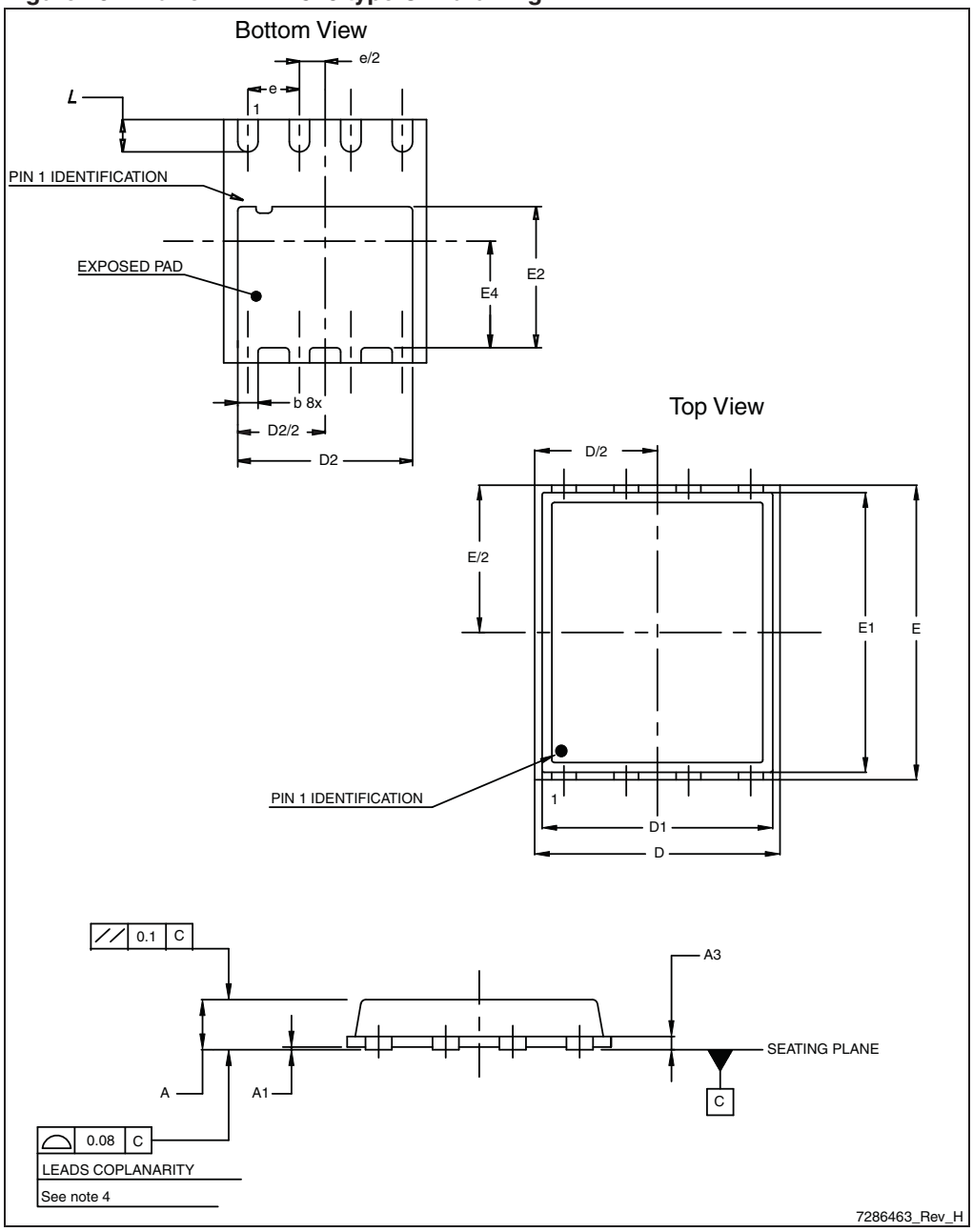
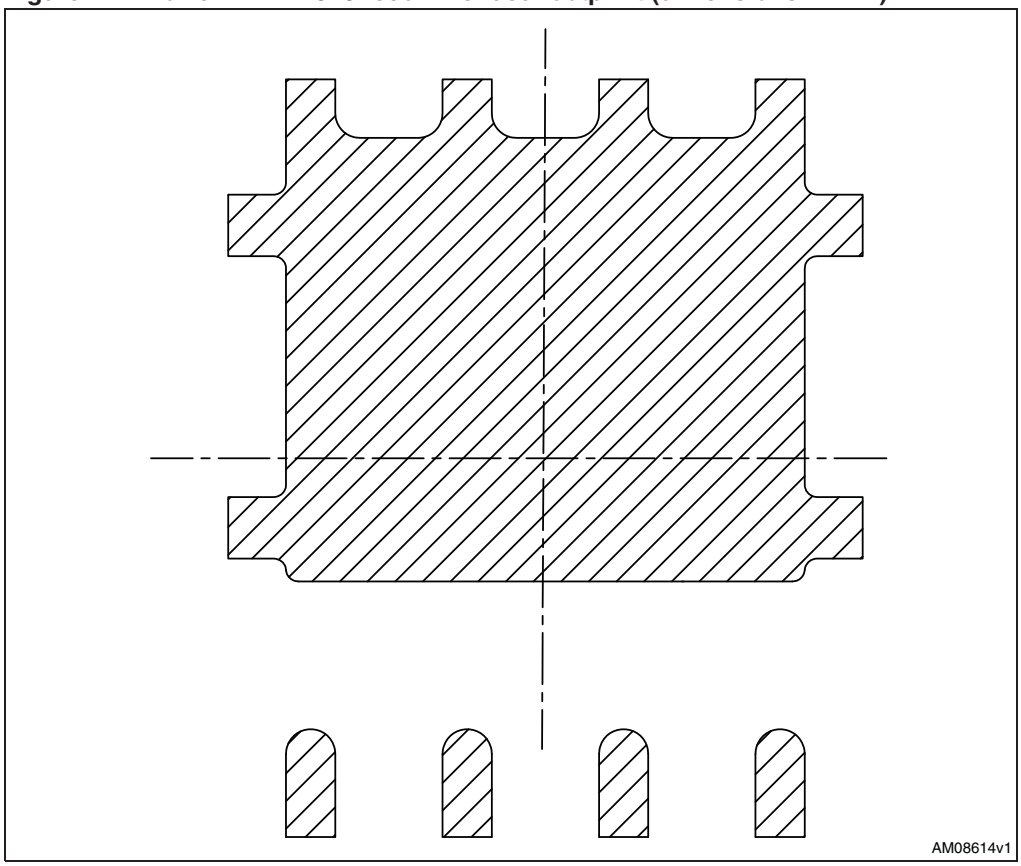


Figure 21. PowerFLAT™ 5x6 recommended footprint (dimensions in mm)



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
22-Jan-2009	1	First release.
08-Jul-2011	2	Datasheet promoted from preliminary data to datasheet.

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