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STL86N3LLH6AG

Automotive-grade N-channel 30 V, 4 mΩ typ., 80 A STripFET™ H6 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

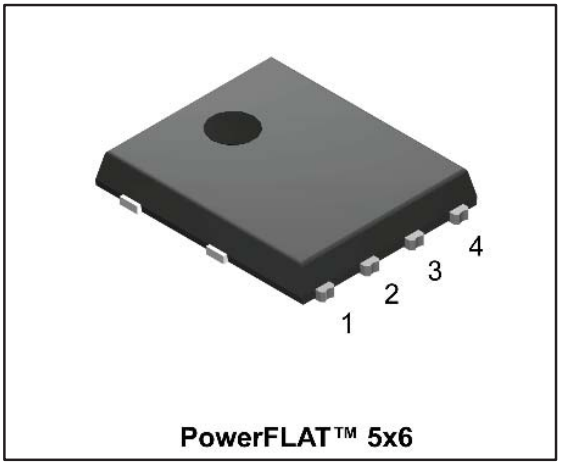
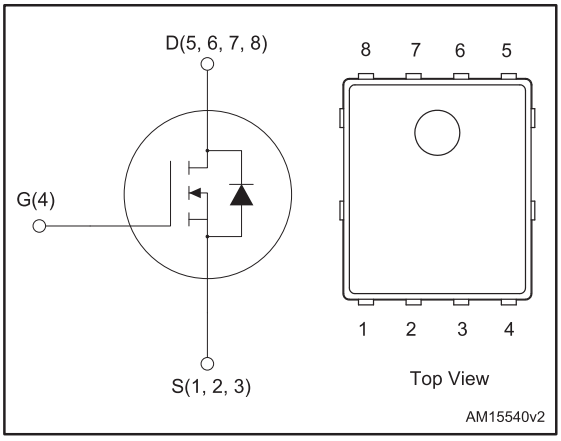


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL86N3LLH6AG	30 V	5.2 mΩ	80 A

- AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss
- Logic level
- Wettable flank package

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET™ H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STL86N3LLH6AG	86N3LLH6	PowerFLAT™ 5x6	Tape and reel

This is information on a product in full production.

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	80	A
I_D (1)	Drain current (continuous) at T_C = 70 °C	60	
I_D (1)	Drain current (continuous) at T_C = 100 °C	51	A
I_{DM} (1), (2)	Drain current (pulsed)	320	A
I_D (3)	Drain current (continuous) at T_{pcb} = 25 °C	21	A
I_D (3)	Drain current (continuous) at T_{pcb} = 70 °C	15.7	A
I_D (3)	Drain current (continuous) at T_{pcb} = 100 °C	13.1	A
I_{DM} (2), (3)	Drain current (pulsed)	84	A
P_{TOT} (1)	Total dissipation at T_C = 25 °C	60	W
P_{TOT} (3)	Total dissipation at T_{pcb} = 25 °C	4	
T_{stg}	Storage temperature range	- 55 to 150	°C
T_j	Operating junction temperature range		

Notes:

(1)The value is rated according to $R_{thj\text{-}c}$.

(2)Pulse width limited by safe operating area.

(3)The value is rated according to $R_{thj\text{-}pcb}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.08	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	31.3	

Notes:

(1)When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 s

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 1 mA	30			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 30 V			1	µA
		V_{GS} = 0, V_{DS} = 30 V, T_C = 125 °C			10	
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.7	2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 10.5 A		4	5.2	mΩ
		V_{GS} = 4.5 V, I_D = 10.5 A		6.7	7.6	mΩ

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	1350	1690	2030	pF
C_{oss}	Output capacitance		230	290	350	pF
C_{rss}	Reverse transfer capacitance		140	176	210	pF
Q_g	Total gate charge	V_{DD} = 15 V, I_D = 21 A, V_{GS} = 4.5 V (see *Figure 14: "Test circuit for gate charge bahavior"*)	-	17	-	nC
Q_{gs}	Gate-source charge		-	8	-	nC
Q_{gd}	Gate-drain charge		-	6	-	nC
R_G	Gate input resistance	f = 1 MHz, Gate DC Bias = 0, Test signal level = 20 mV open drain, ID = 0	1.25	1.7	1.2	Ω

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V, I_D = 10.5 A, R_G = 4.7 Ω, V_{GS} = 10 V See *Figure 13: "Test circuit for resistive load switching times"* and *Figure 18: "Switching time waveform"*	-	9.5	-	ns
t_r	Rise time		-	30	-	ns
$t_{d(off)}$	Turn-off delay time		-	37	-	ns
t_f	Fall time		-	12	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		21	A
I_{SDM}(1)	Source-drain current (pulsed)		-		84	A
V_{SD}(2)	Forward on voltage	I_{SD} = 21 A, V_{GS} = 0	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 10.5 A, di/dt = 100 A/µs V_{DD} = 25 V See *Figure 15: "Test circuit for inductive load switching and diode recovery times"*	-	24		ns
Q_{rr}	Reverse recovery charge		-	16.8		nC
I_{RRM}	Reverse recovery current		-	1.4		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

2.2 Electrical characteristics (curves)

Figure 2: Safe operating area

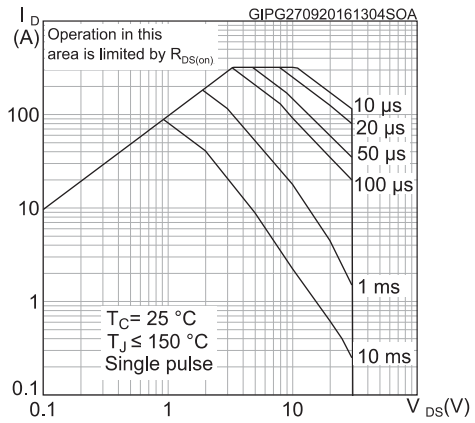


Figure 3: Thermal impedance

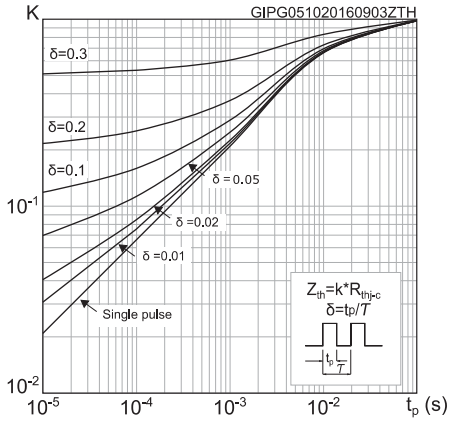


Figure 4: Output characteristics

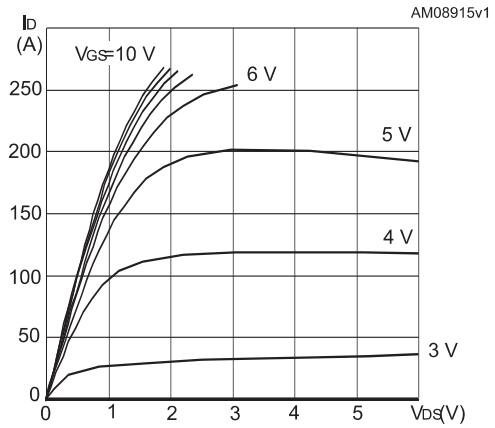


Figure 5: Transfer characteristics

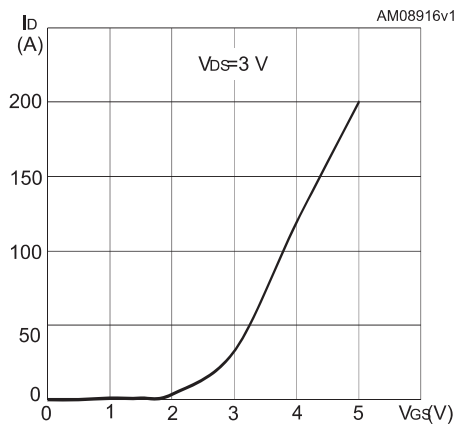


Figure 6: Normalized $V_{(BR)DSS}$ vs temperature

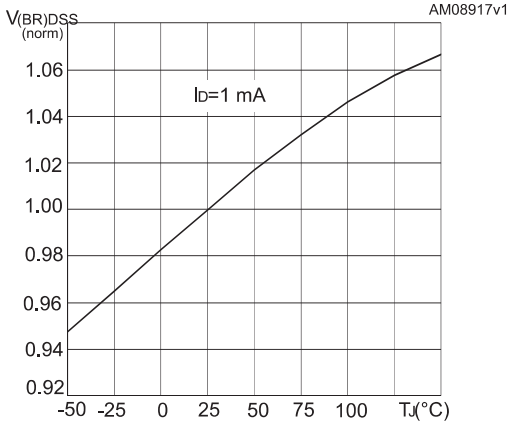


Figure 7: Static drain-source on-resistance

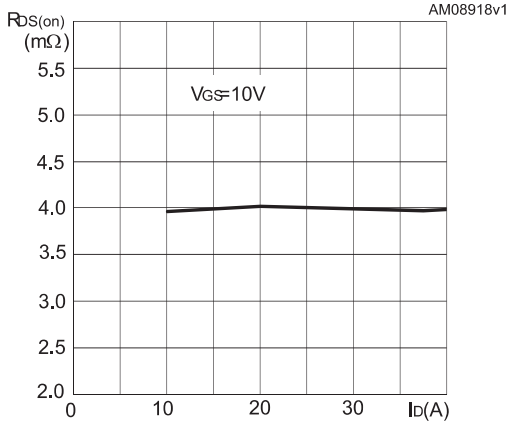


Figure 8: Gate charge vs gate-source voltage

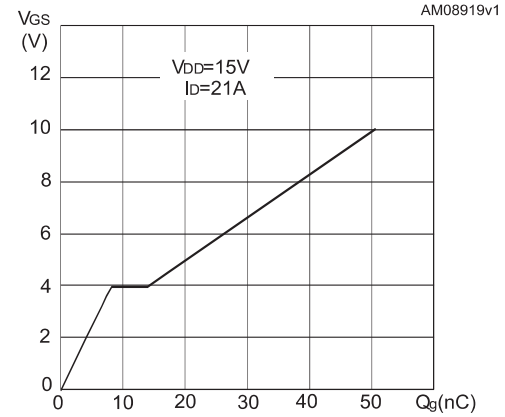


Figure 9: Capacitance variations

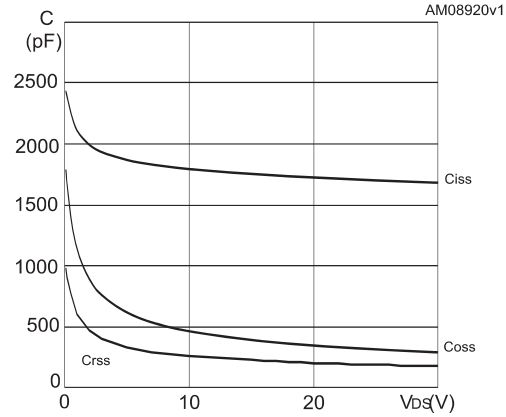


Figure 10: Normalized gate threshold voltage vs temperature

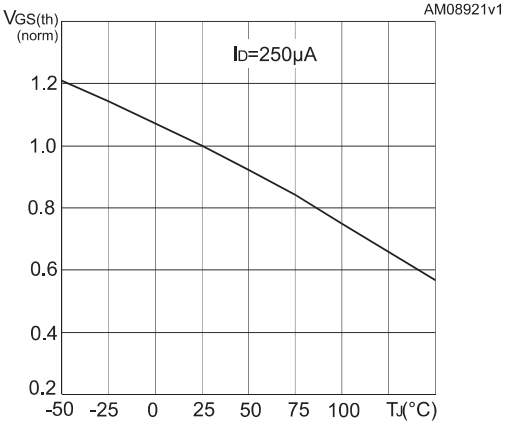


Figure 11: Normalized on resistance vs temperature

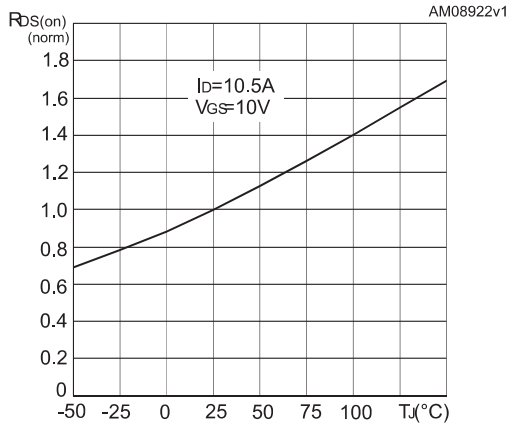
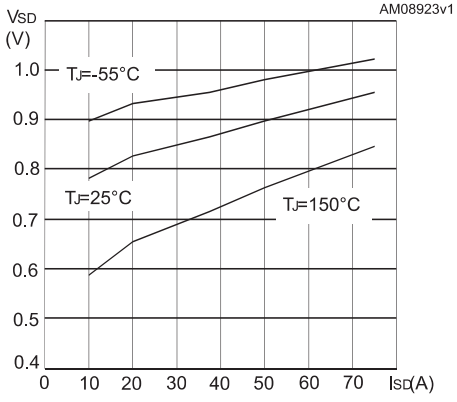


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times

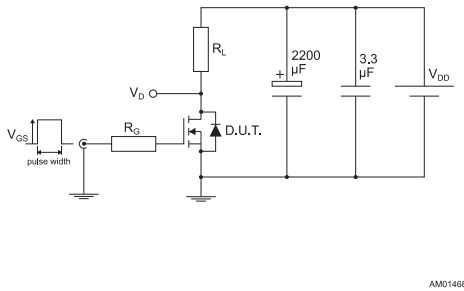


Figure 14: Test circuit for gate charge behavior

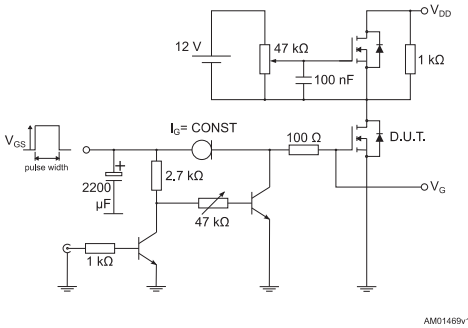


Figure 15: Test circuit for inductive load switching and diode recovery times

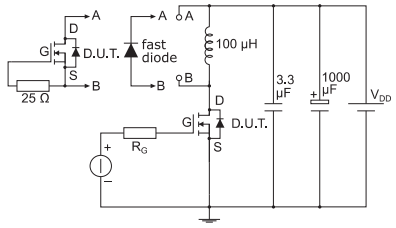


Figure 16: Unclamped inductive load test circuit

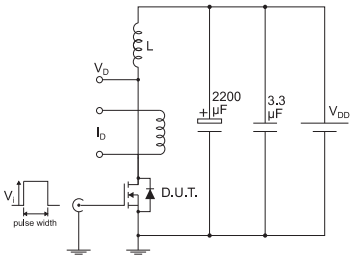


Figure 17: Unclamped inductive waveform

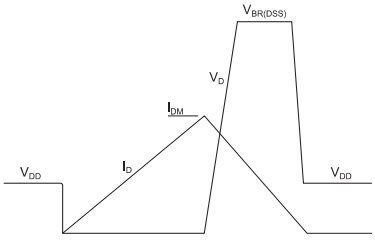
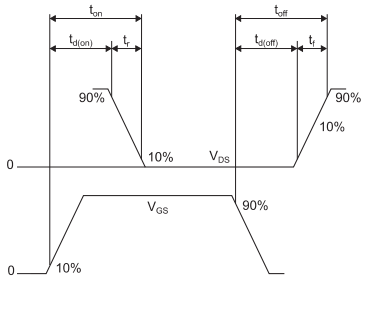


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT™5x6 WF type R package information

Figure 19: PowerFLAT™ 5x6 WF type R package outline

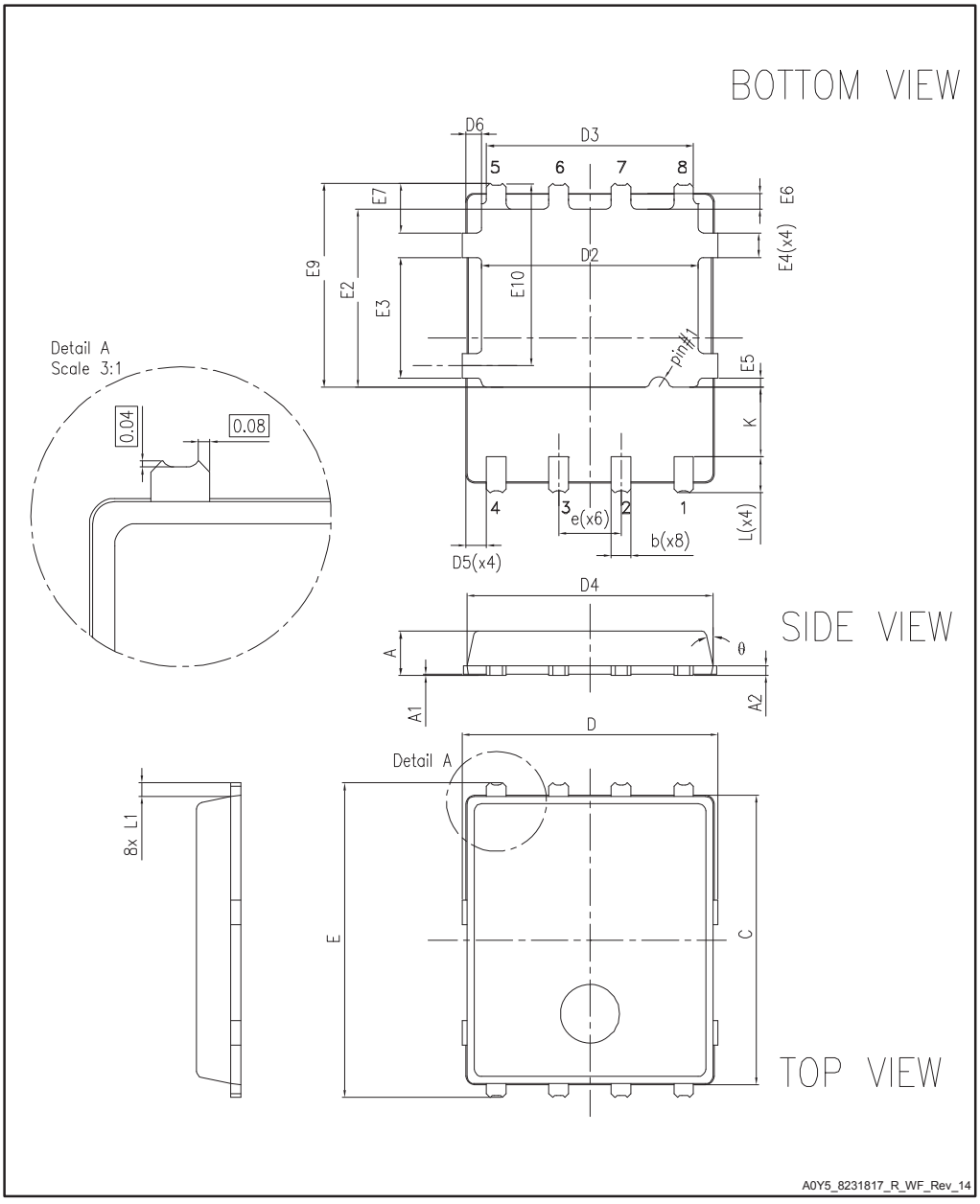
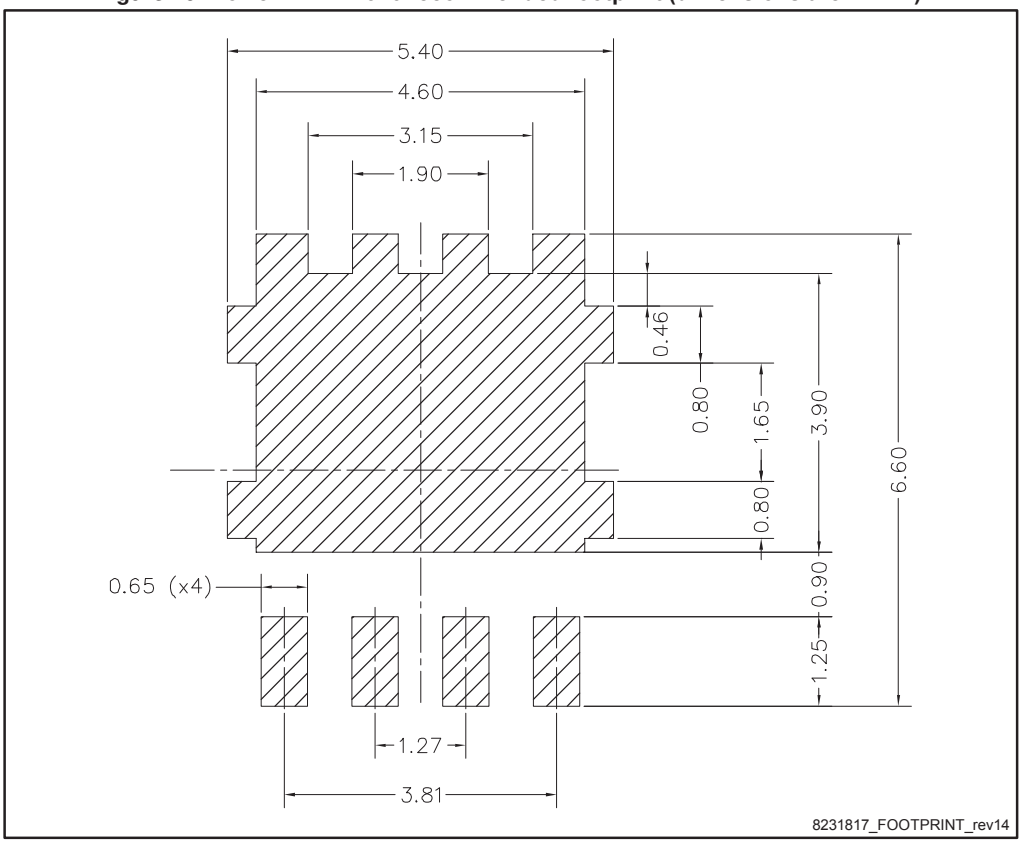


Table 8: PowerFLAT™ 5x6 WF type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.4	0.55
D6	0.15	0.3	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.275		1.575
L	0.725	0.825	0.925
L1	0.175	0.275	0.375
Θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 WF packing information

Figure 21: PowerFLAT™ 5x6 WF tape (dimensions are in mm)

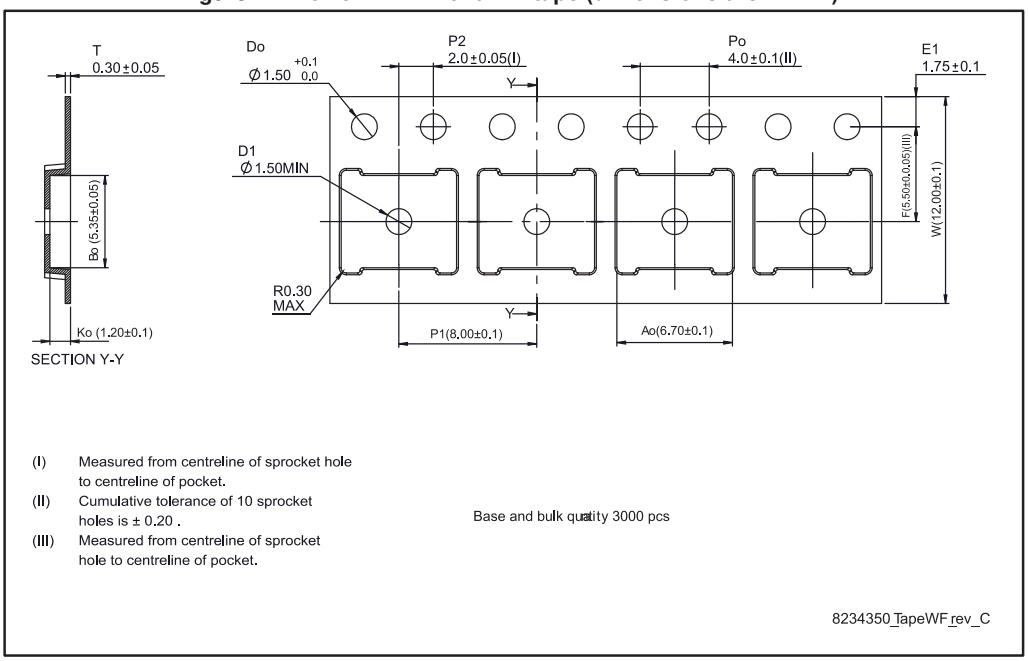


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

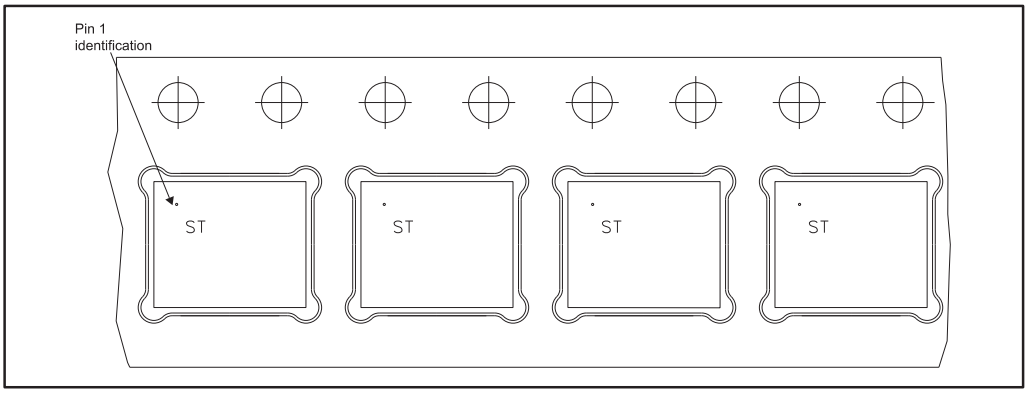
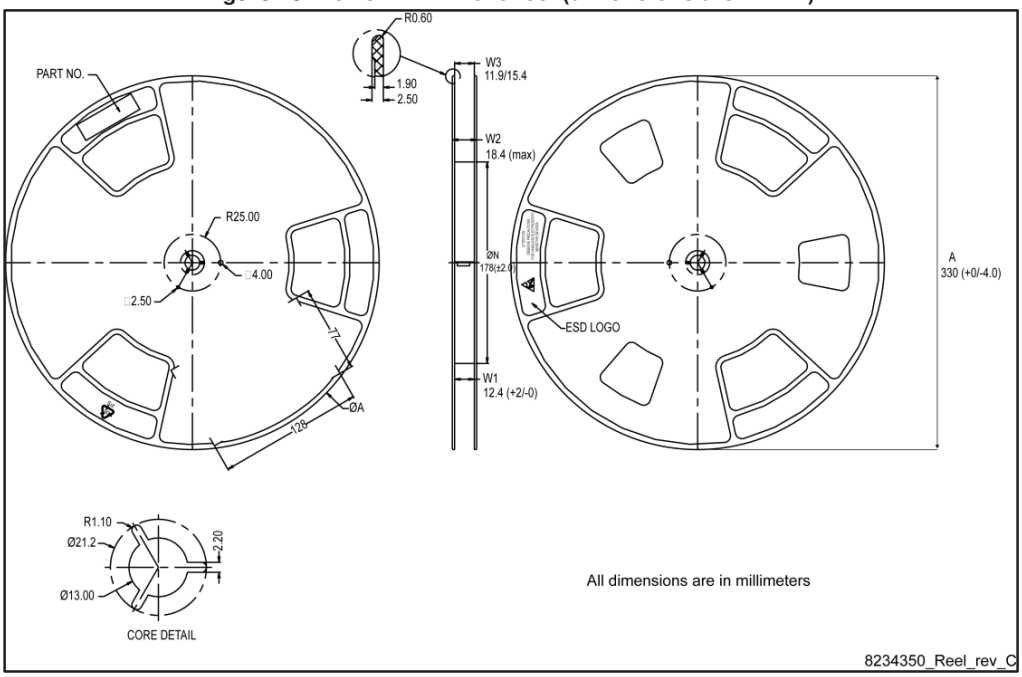


Figure 23: PowerFLAT™ 5x6 reel (dimensions are in mm)



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
26-Sep-2014	1	First release.
21-Jan-2015	2	Document status promoted from preliminary to production data. Updated *Section 4: Package mechanical data.*
03-Feb-2015	3	Updated title and features in cover page.
03-Oct-2016	4	Updated title and features in cover page. Updated *Table 2: "Absolute maximum ratings"* and *Table 4: "On/off-states"*. Changed *Figure 2: "Safe operating area"* and *Figure 3: "Thermal impedance"*.

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