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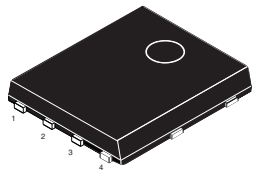
STL8DN10LF3

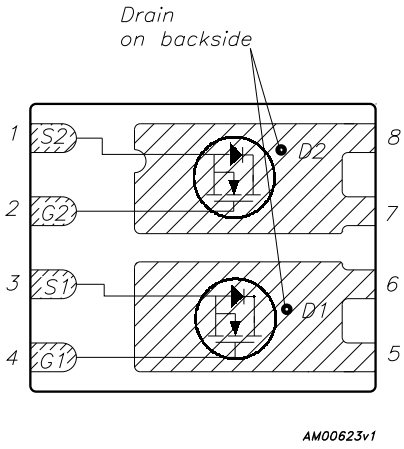
Automotive-grade dual N-channel 100 V, 25 mΩ typ., 7.8 A STripFET™ III Power MOSFET in a PowerFLAT™ 5x6 double island package

Datasheet — production data



PowerFLAT™ 5x6 double island

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D
STL8DN10LF3	100 V	35 mΩ	7.8 A

- Designed for automotive applications and AEC-Q101 qualified
- Logic level $V_{GS(th)}$
- 175 °C junction temperature
- 100% avalanche rated
- Wettable flank package

Applications

- Switching applications

Description

This device is an N-channel enhancement mode Power MOSFET produced using STMicroelectronics' STripFET™ III technology, which is specifically designed to minimize on-resistance and gate charge to provide superior switching performance.

Table 1. Device summary

Order code	Marking	Packages(1)	Packaging
STL8DN10LF3	8DN10LF3	PowerFLAT™ 5x6 double island	Tape and reel

1. For wettable flank option, please contact ST sale offices

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	±20	V
I_D (1),(2)	Drain current (continuous) at T_C = 25 °C	20	A
I_D	Drain current (continuous) at T_C = 100 °C	20	A
I_D (4)	Drain current (continuous) at T_{pcb} = 25 °C	7.8	A
I_D (4)	Drain current (continuous) at T_{pcb}=100 °C	5.5	A
I_{DM} (3),(4)	Drain current (pulsed)	31.2	A
P_{TOT}	Total dissipation at T_C = 25°C	70	W
P_{TOT} (4)	Total dissipation at T_{pcb} = 25°C	4.3	W
I_{AV}	Not-repetitive avalanche current	7.8	A
E_{AS} (5)	Single pulse avalanche energy	190	mJ
T_J	Operating junction temperature	-55 to 175	°C
T_{stg}	Storage temperature		°C

1. Specified by design. Not subject to production test.
2. Current is limited by bonding, with an R_{thJC} = 2.3 °C/W the chip is able to carry 32 A at 25 °C.
3. Pulse width limited by safe operating area.
4. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec
5. Starting T_J= 25 °C, I_D= 8 A, V_{DD}= 25 V, per channel, 100% tested.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.1	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	35	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS}= 0)	I_D = 250 µA	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 100 V			1	µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS}= 10 V, I_D= 4 A		25	35	mΩ
		V_{GS}= 5 V, I_D= 4 A		40	50	mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	970	-	pF
C_{oss}	Output capacitance		-	115	-	pF
C_{rss}	Reverse transfer capacitance		-	11.5	-	pF
Q_g	Total gate charge	V_{DD}=50 V, I_D = 7.8 A V_{GS} =10 V *Figure 13*	-	20.5	-	nC
Q_{gs}	Gate-source charge		-	4	-	nC
Q_{gd}	Gate-drain charge		-	5	-	nC
R_G	Intrinsic gate resistance	f=1 MHz open drain	-	3.65	-	Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}=50 V, I_D= 7.8 A, R_G=4.7 Ω, V_{GS}=10 V *Figure 14*	-	8.7	-	ns
t_r	Rise time		-	9.6	-	ns
$t_{d(off)}$	Turn-off delay time		-	50.6	-	ns
t_f	Fall time		-	5.2	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		7.8	A
I_{SDM}(1)	Source-drain current (pulsed)		-		31.2	A
V_{SD}(2)	Forward on voltage	I_{SD} = 7.8 A, V_{GS}=0	-		1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 7.8 A, di/dt = 100 A/µs, V_{DD}=48 V, Tj=150 °C	-	42.5		ns
Q_{rr}	Reverse recovery charge		-	87		nC
I_{RRM}	Reverse recovery current		-	4.08		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration= 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

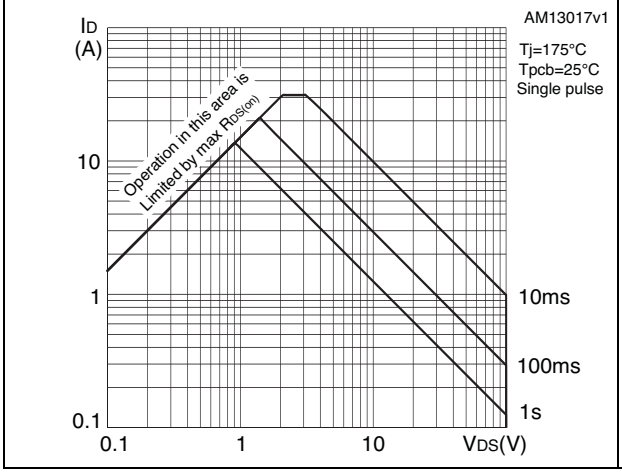


Figure 3. Thermal impedance

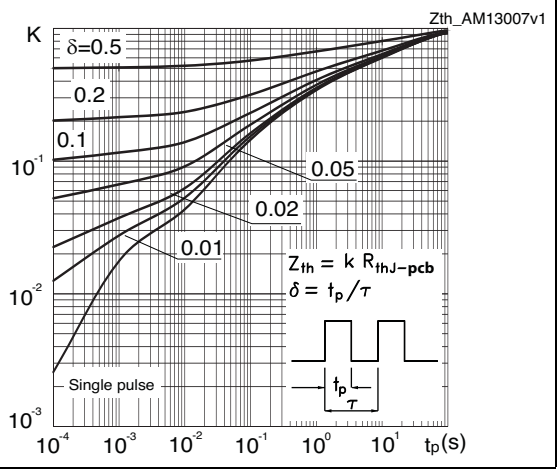


Figure 4. Output characteristics

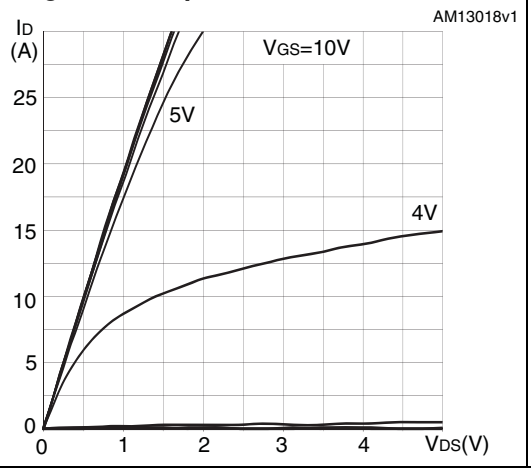


Figure 5. Transfer characteristics

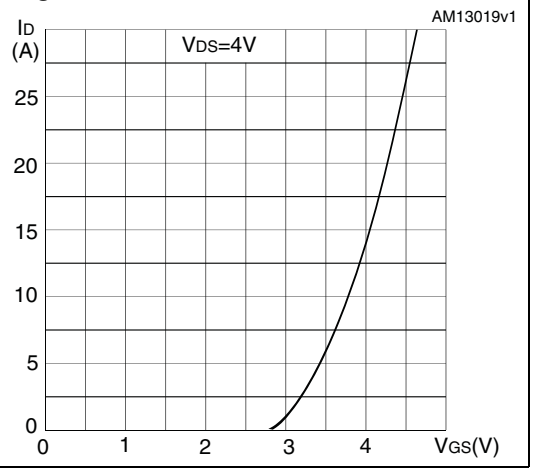


Figure 6. Normalized $V_{(BR)DSS}$ vs temperature

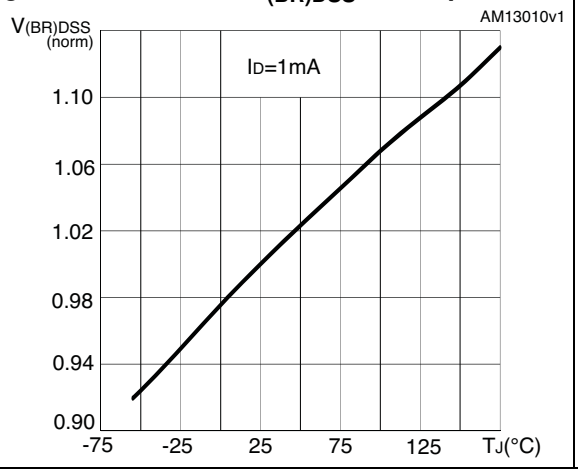


Figure 7. Static drain-source on-resistance

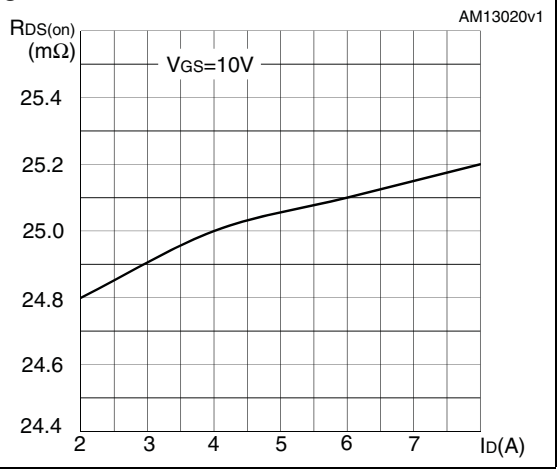


Figure 8. Gate charge vs gate-source voltage

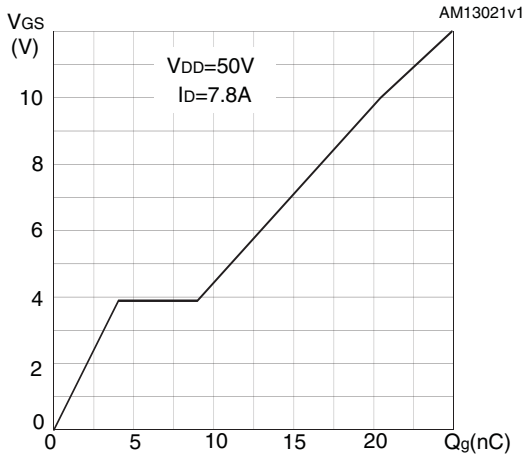


Figure 9. Capacitance variations

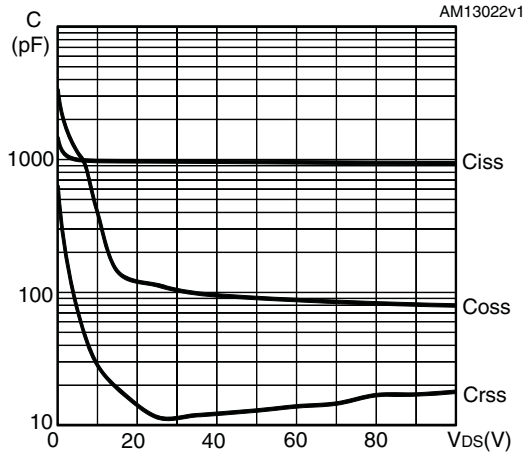


Figure 10. Normalized gate threshold voltage vs temperature

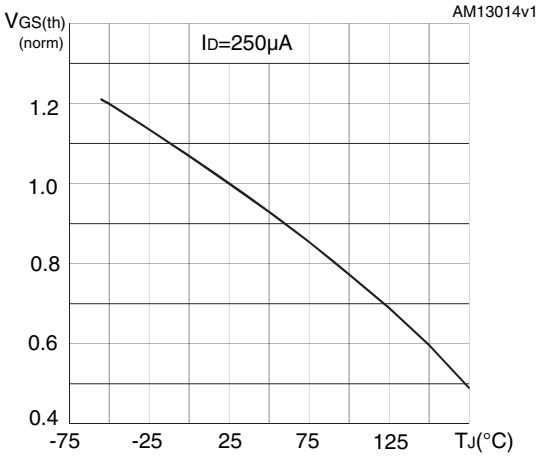
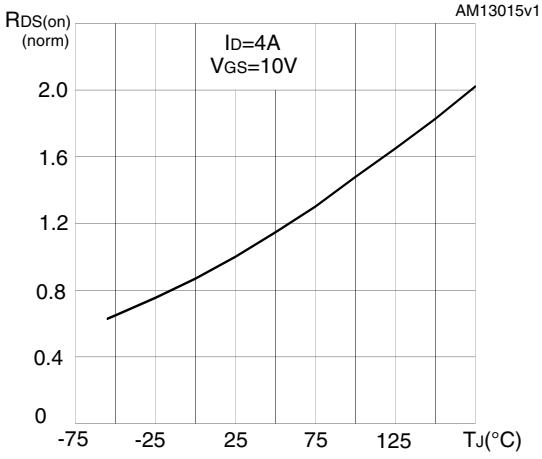


Figure 11. Normalized on-resistance vs temperature



3 Test circuits

Figure 12. Switching times test circuit for resistive load

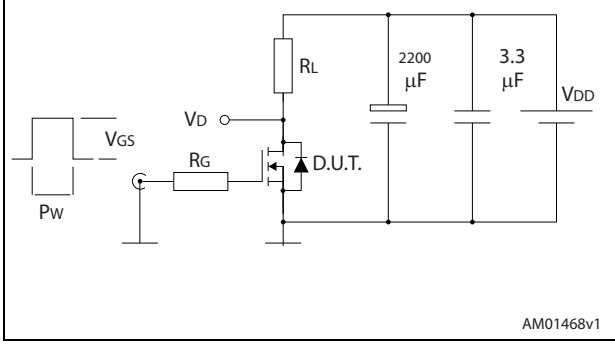


Figure 13. Gate charge test circuit

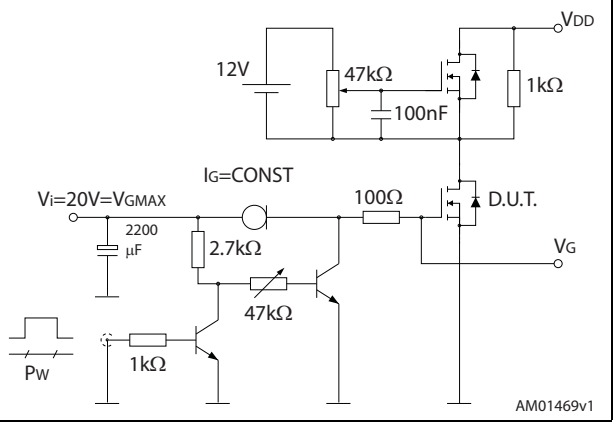


Figure 14. Test circuit for inductive load switching and diode recovery times

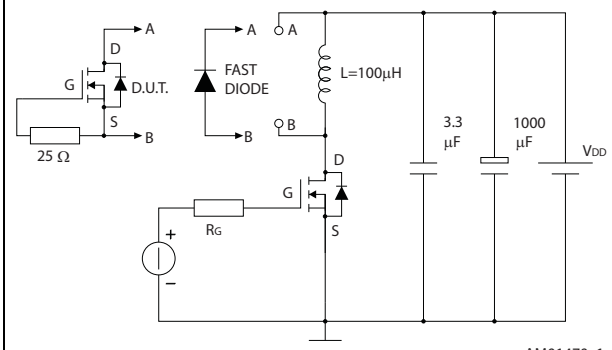


Figure 15. Unclamped inductive load test circuit

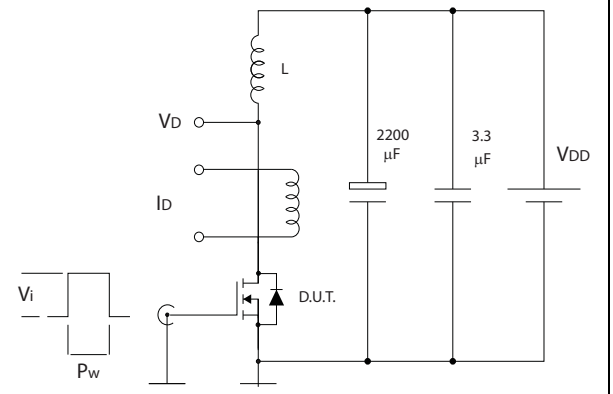


Figure 16. Unclamped inductive waveform

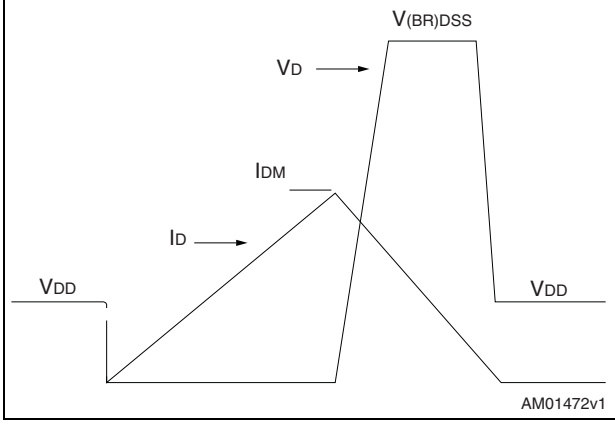
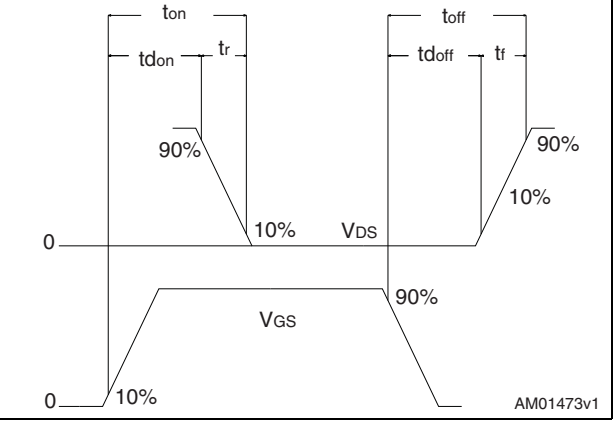


Figure 17. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

Figure 18. PowerFLAT™ 5x6 double island type R-B drawing

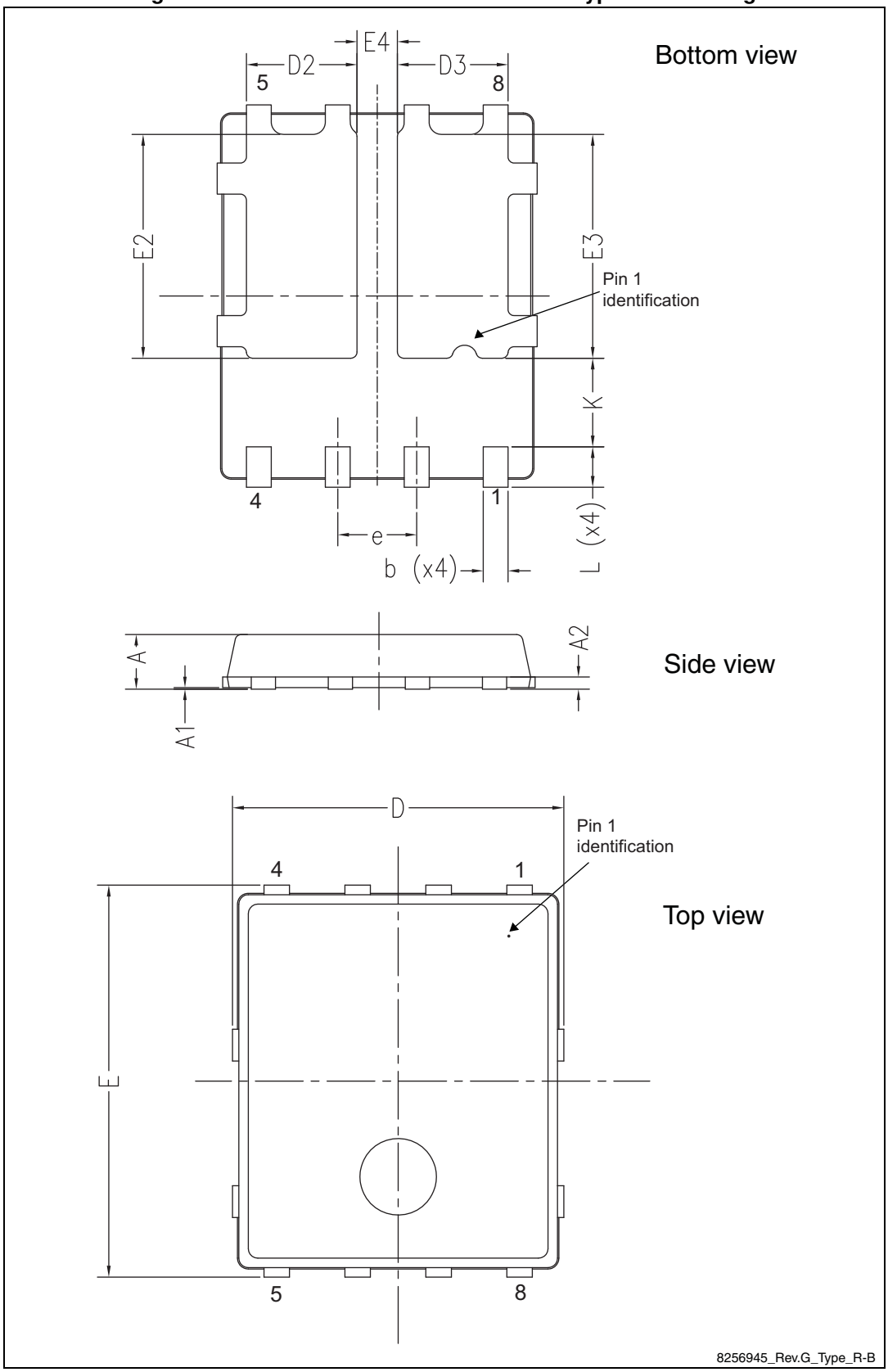


Table 8. PowerFLAT™ 5x6 double island type R-B mechanical data

Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	1.68		1.88
E2	3.50		3.70
D3	1.68		1.88
E3	3.50		3.70
E4	0.55		0.75
e		1.27	
L	0.60		0.80
K	1.275		1.575

Figure 19. PowerFLAT 5x6 double island type WF drawing

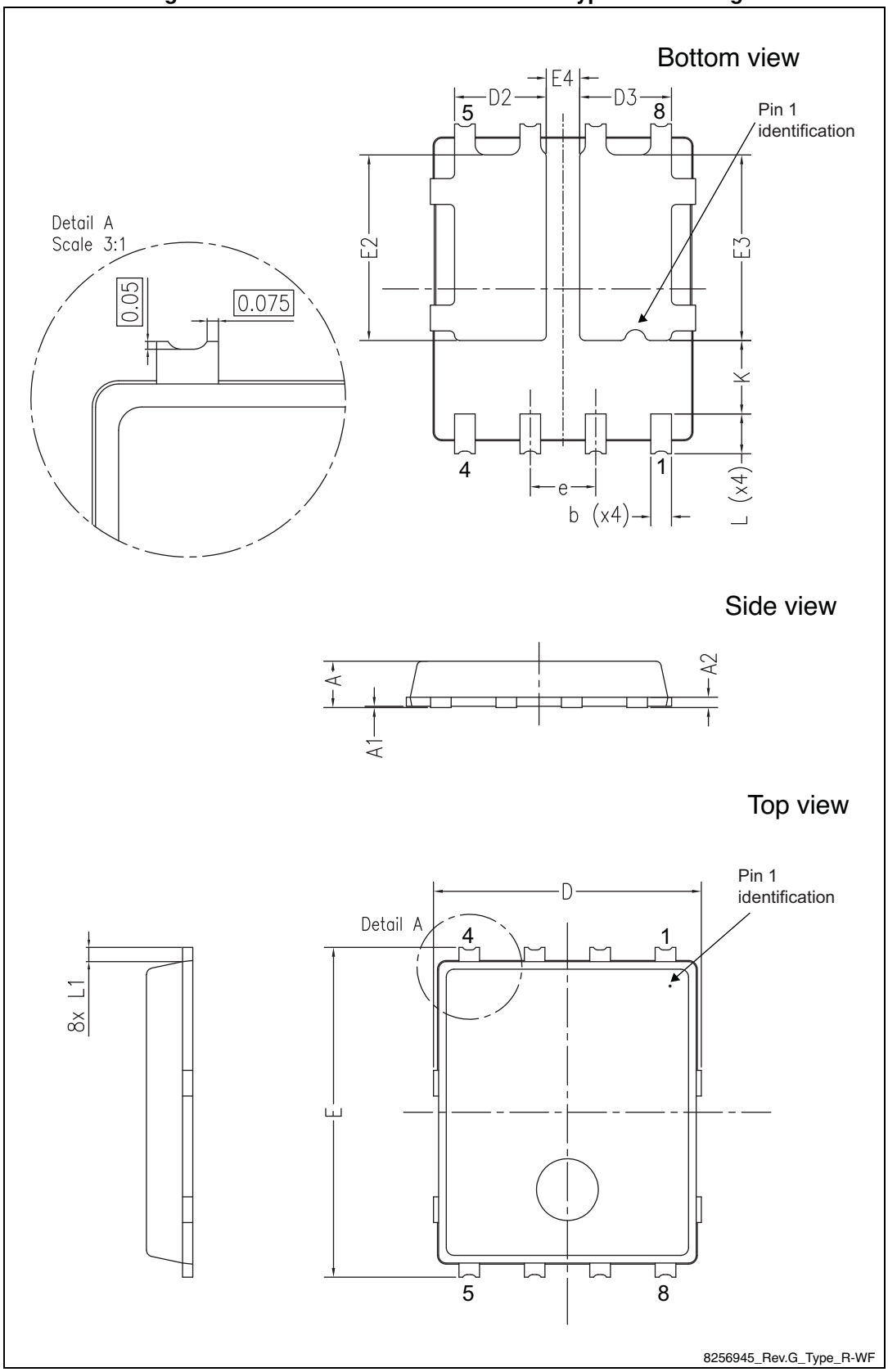
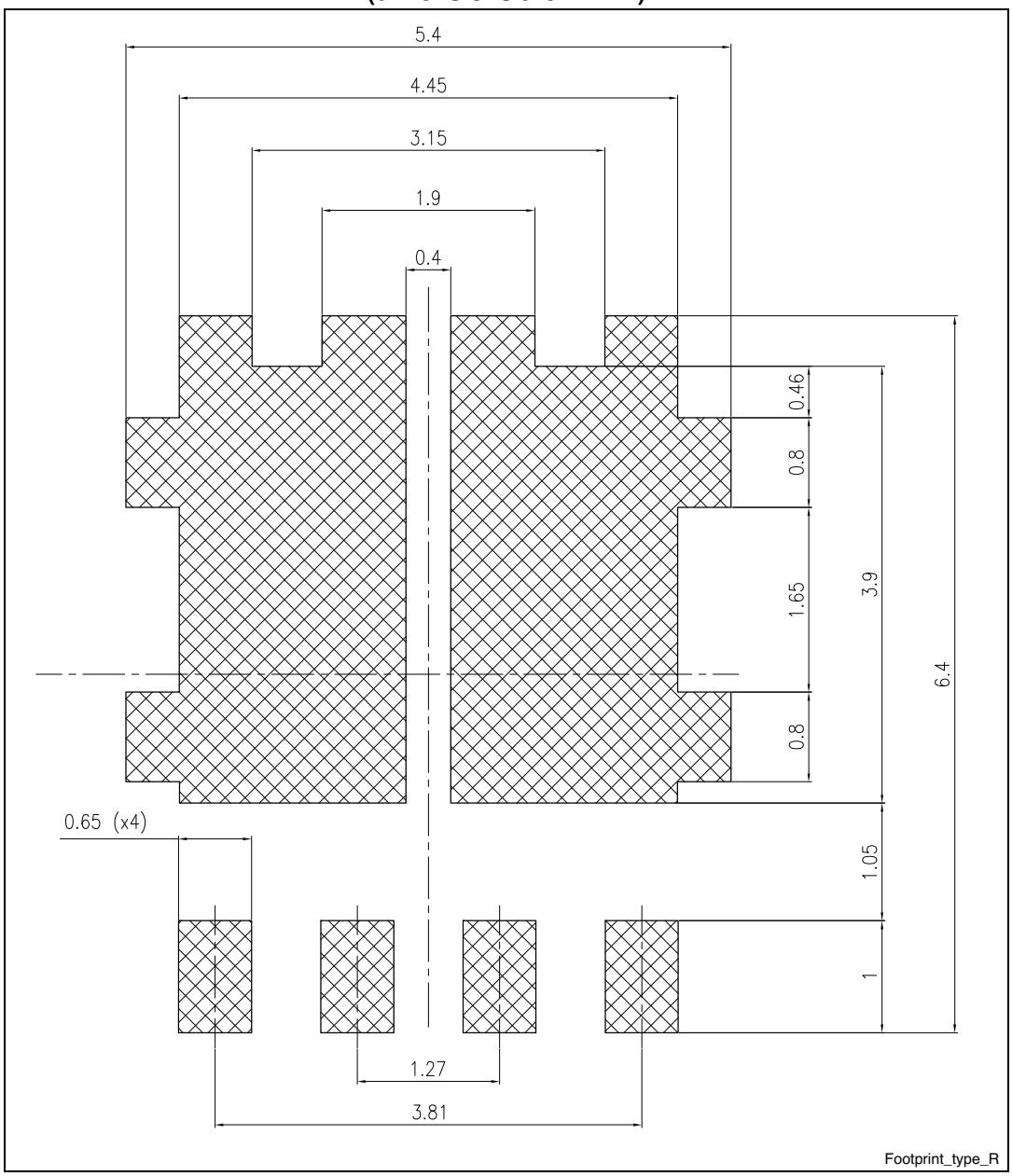


Table 9. PowerFLAT 5x6 double island type WF mechanical data

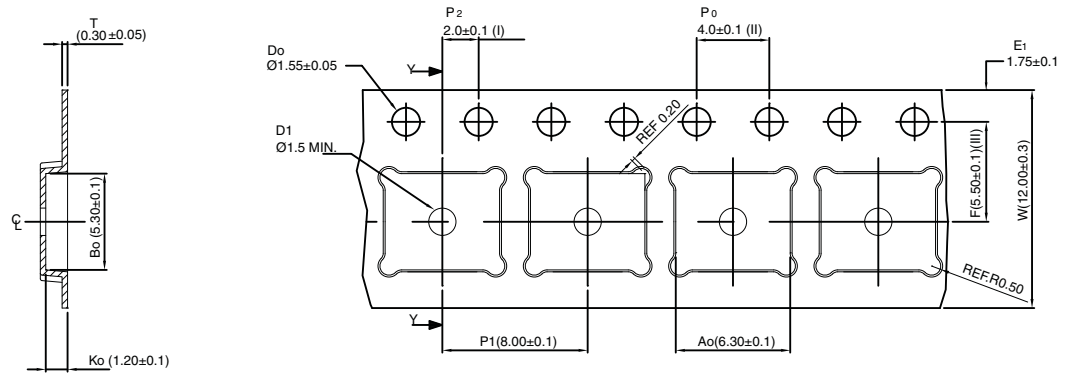
Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	6.20	6.40	6.60
D2	1.68		1.88
E2	3.50		3.70
D3	1.68		1.88
E3	3.50		3.70
E4	0.55		0.75
e		1.27	
L	0.70		0.90
L1		0.275	
K	1.275		1.575

Figure 20. PowerFLAT™ 5x6 double island type R drawing recommended footprint (dimensions are in mm)



5 Packaging mechanical data

Figure 21. PowerFLAT™ 5x6 double island type R-B tape[(a)]



(I) Measured from centerline of sprocket hole to centerline of pocket.

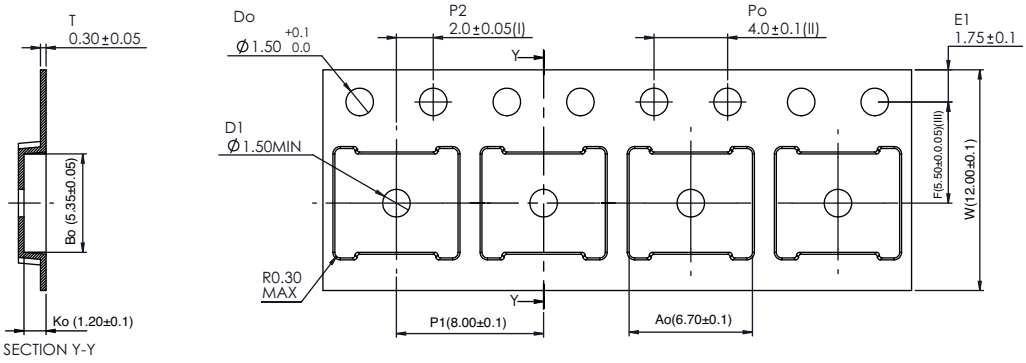
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .

(III) Measured from centerline of sprocket hole to centerline of pocket.

Base and bulk quantity 3000 pcs

8234350_Tape_rev_C

Figure 22. PowerFLAT 5x6 double island type WF tape[(a)]



(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .

(III) Measured from centreline of sprocket hole to centreline of pocket.

Base and bulk quantity 3000 pcs

8234350_TapeWF_rev_C

a. All dimensions are in millimeters.

Figure 23. PowerFLAT™ 5x6 package orientation in carrier tape

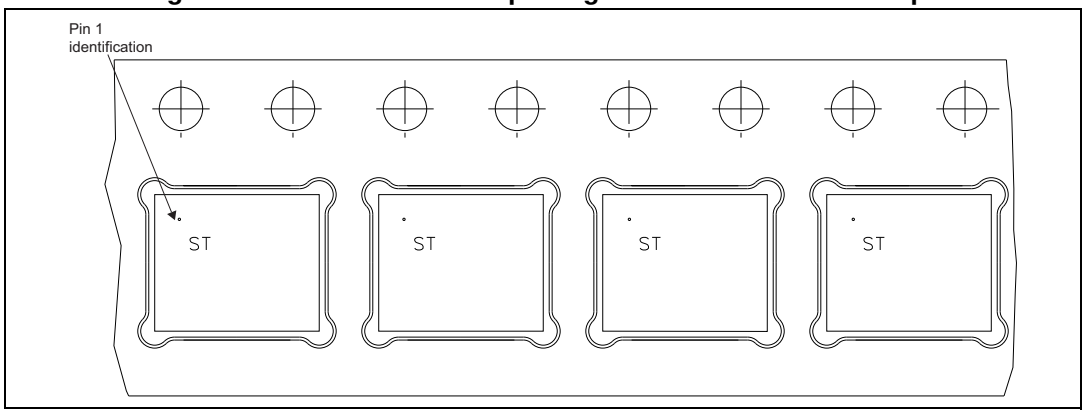
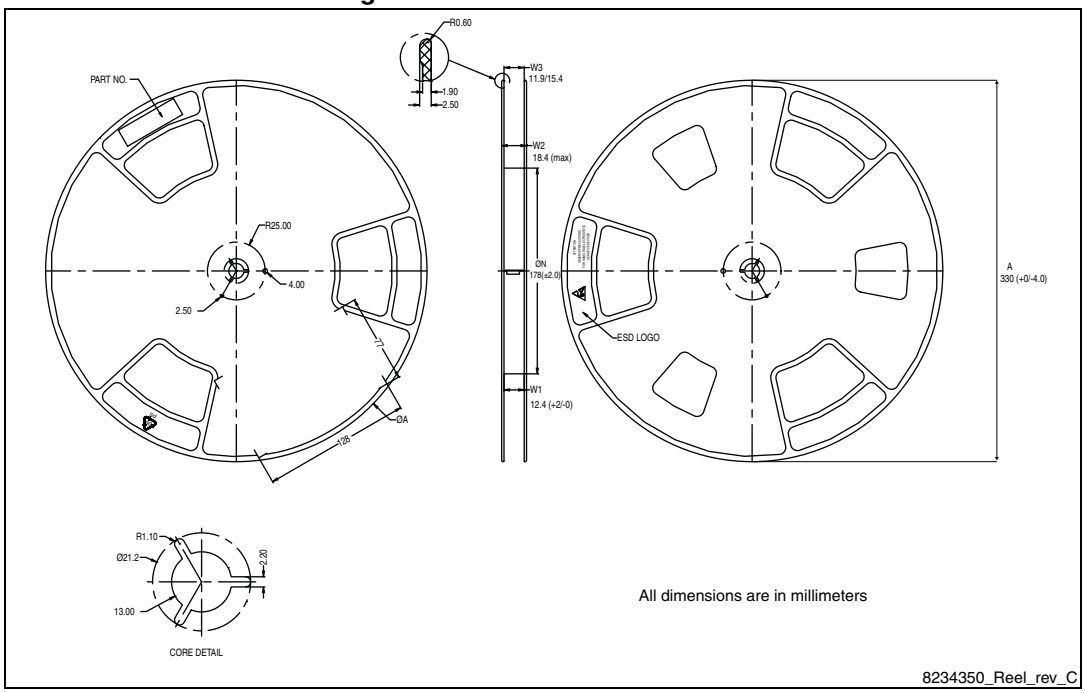


Figure 24. PowerFLAT™ 5x6 reel



6 Revision history

Table 10. Document revision history

Date	Revision	Changes
28-Mar-2012	1	First release.
20-Jun-2012	2	Added *Section 2.1: Electrical characteristics (curves)*. Updated *Section 4: Package mechanical data* and title on the cover page.
26-Jun-2012	3	Updated *Figure 9: Capacitance variations*. Document status promoted from preliminary to production data.
28-Oct-2013	4	– Updated: *Section 4: Package mechanical data* and *Section 5: Packaging mechanical data* – Updated title and features in cover page – Modified: $V_{GS(th)}$ value in *Table 4* – Minor text changes
20-Feb-2014	5	– Added: *Features* in cover page – Added: note *1* in *Table 1* – Added: *Table 19* and *Table 9* – Added: *Figure 22* – Minor text changes

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