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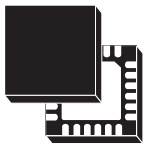
STLBC01

Bluetooth® low energy controller

Datasheet - production data



VFQFPN 24L

Features

- Bluetooth specification v4.0 compliant master and slave BLE controller
- Bluetooth protocol stack for STM32L and profiles provided separately
- Operating supply voltage from 1.9 to 3.6 V
- 13 mA maximum peak current allows standard coin cell battery usage
- Low power physical layer
- Link layer with embedded security engine
- UART and SPI available as HCI transport layers
- SPI interface allows proprietary low power mode to further reduce the power consumption
- ISM 2.4 GHz frequency band
- 1 Mbps on-air data rate
- Wide spread and low cost 26 MHz Xtal
- 200 Ω differential impedance of antenna port
- Very small number of external discrete components
- Programmable output power from -18 dBm to +3 dBm
- Digital RSSI
- Power management with integrated linear regulator
- Battery level detector function to keep control of the battery level detection
- Compliant with the following radio frequency regulations: ETSI EN 300 328, EN 300 440, FCC CFR47 Part 15, ARIB STD-T66
- QFN 24 5x5 mm RoHS package
- Operating temp. range from -40 °C to 85 °C

Applications

- Watches
- Fitness, wellness and sports
- Consumer medical
- Security/proximity
- Remote control
- Remote sensing
- Home and industrial automation
- Assisted living
- Mobile phone peripherals
- PC peripherals

Description

The STBLC01 is a very low power Bluetooth low energy (BLE) controller compliant with Bluetooth specification 4.0. The STBLC01 integrates a low power physical layer, a link layer with an embedded security engine, a host controller interface (HCI), and a power management. The STBLC01 allows the meeting of the tight advisable peak current requirements imposed by the use of standard coin cell batteries, and even in worst-case operating conditions 13 mA is the maximum current that is drawn from the input voltage source. Yet ultra low power sleep modes and very short transition time between operating modes allow a very low average current consumption to be achieved, which results in longer battery life. The STBLC01 offers the possibility of interfacing with several external microcontrollers using either UART or SPI as the transport layer for HCI communications.

Table 1. Device summary

Order code	Package	Packing
STBLC01QTR	VFQFPN 24L	Tape and reel

Contents

List of tables

List of figures

1 General description

The conceptual drawing in *Figure 1* shows the BLE stack partitioning; meanwhile a simplified application schematic is shown in *Figure 2*.

Figure 1. BLE stack

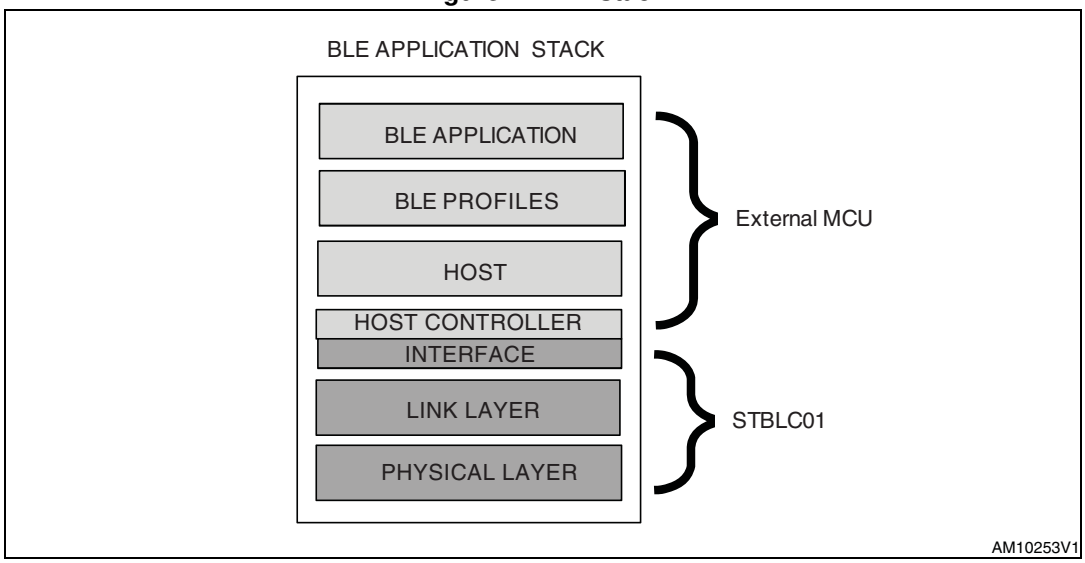
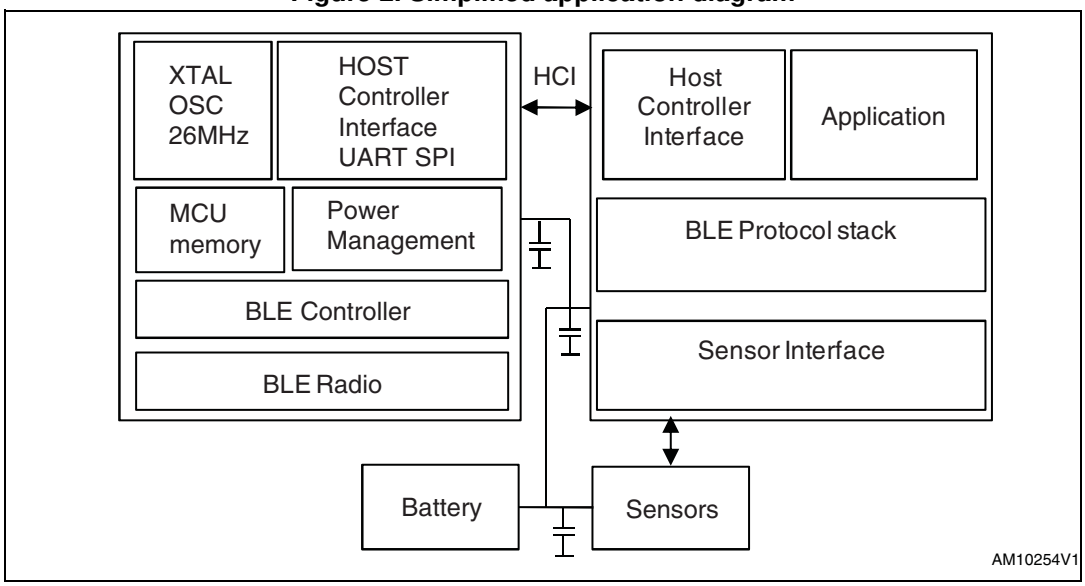


Figure 2. Simplified application diagram



The protocol stack running in the host is released separately in the form of static library for the STM32L. BLE qualified profiles are available separately.

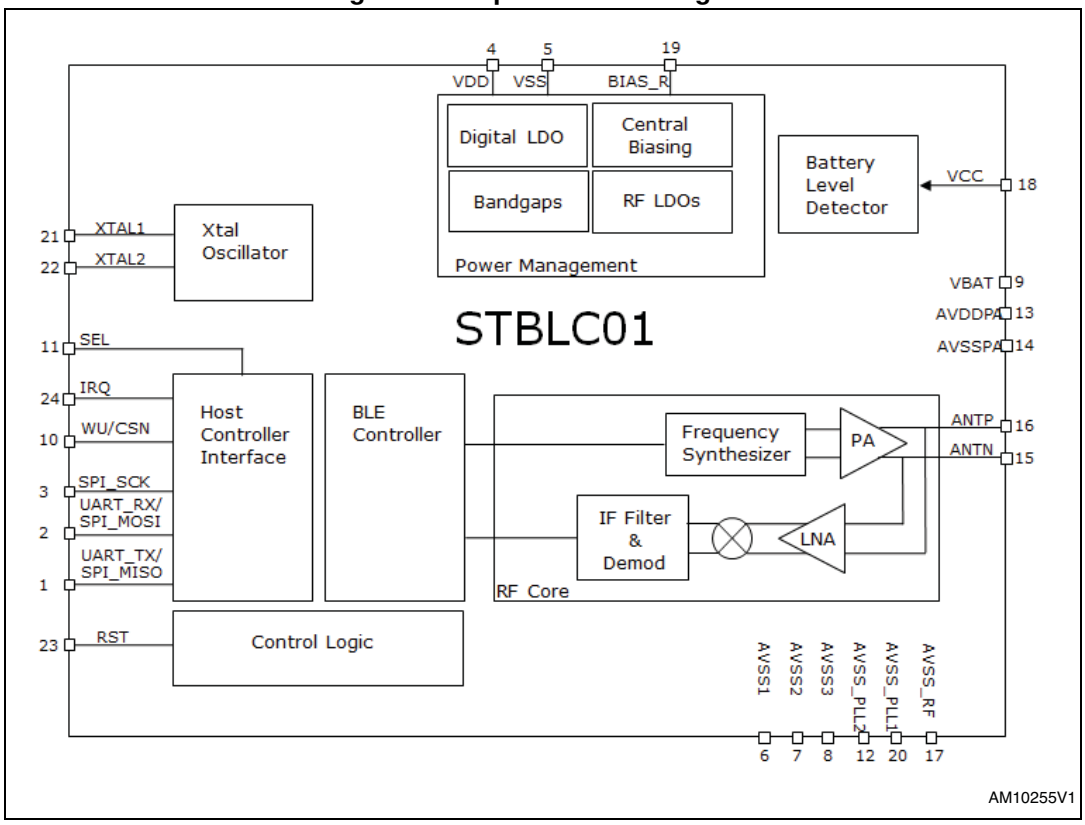
The STBLC01 radio has been designed specifically for low power applications. The TX output power can be controlled by the BLE host from -18 dBm to +3 dBm in order to optimize the current consumption for a wide set of applications.

The STBLC01 uses a very small number of external discrete components. The robust internal RX architecture allows the STBLC01 to operate without the need for expensive external filters to block undesired frequency bands. A simple matching network allows the adaptation of antenna impedance to the STBLC01 differential 200 Ω real impedance.

2 Block diagram

A simplified block diagram of the STBLC01 is shown in *Figure 3*.

Figure 3. Simplified block diagram



3 Typical application diagram and pin description

Figure 4. Suggested application schematic

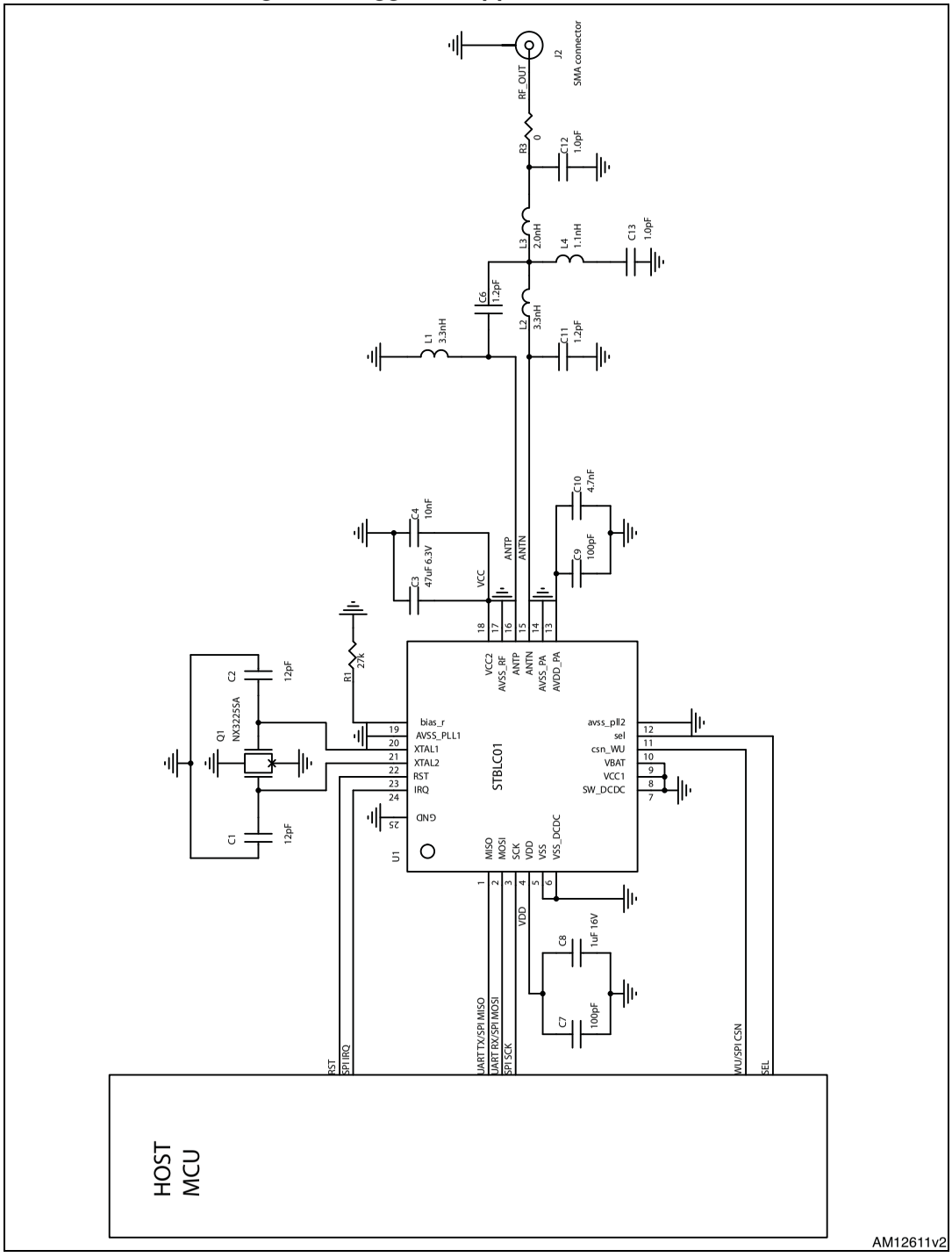


Table 2. External components of the typical application diagram

Components	Value	Descriptions
C1, C2	12 pF	Crystal loading capacitor
C3	47 μF	VCC decoupling capacitor
C4	10 nF	VCC decoupling capacitor
C6	1.2 pF	RF balun/matching capacitor
C7	100 pF	LDO-digital decoupling capacitor
C8	1 μF	LDO-digital decoupling capacitor
C9	100 pF	LDO-PA decoupling capacitor
C10	4.7 nF	LDO-PA decoupling capacitor
C11	1.2 pF	RF balun/matching capacitor
C12	1 pF	RF balun/matching capacitor
C13	1 pF	RF balun/matching capacitor
L1	3.3 nH	RF balun/matching inductor
L2	3.3 nH	RF balun/matching inductor
L3	2.0 nH	RF balun/matching inductor
L4	1.1 nH	RF balun/matching inductor
R1	27 kΩ	Bias resistor
Q1	26 MHz	NX3225SA crystal

Figure 5. STBLC01 pinout top view

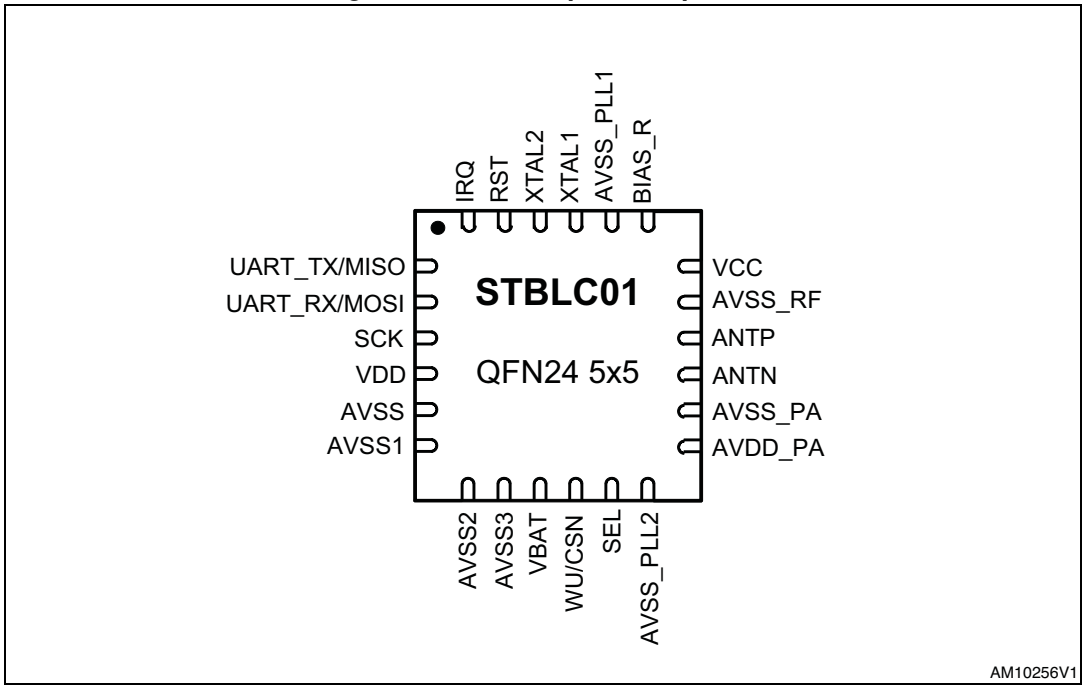


Table 3. STBLC01 pinout description

Pin	Name	Type	Description
1	UART_TX / SPI_MISO	Digital output	UART TX / SPI data output (SDO)
2	UART_RX / SPI_MOSI	Digital input	UART RX / SPI data input (SDI)
3	SPI_CLK	Digital input	SPI clock input (SCK)
4	VDD	Power	Positive supply for the digital part (1)
5	AVSS	Ground	Negative supply for the digital part(2)
6	AVSS1	Ground	Ground(2)
7	AVSS2	Ground	Ground(2)
8	AVSS3	Ground	Ground(2)
9	VBAT	Analog	Ground(2)
10	WU/CSN	Digital input	UART wake up from sleep/off mode / SPI chip select.
11	SEL	Digital input	Interface selection (0 = UART, 1 = SPI).
12	AVSS_PLL2	Ground	Negative supply of PLL(2)
13	AVDD_PA	Power	Regulated output voltage for the power amplifier(1)
14	AVSS_PA	Ground	Negative supply for the power amplifier(2)
15	ANTN	RF	Differential RF ports
16	ANTP	RF	
17	AVSS_RF	Ground	Negative supply of RF part(2)
18	VCC	Power	Main supply for the chip
19	BIAS_R	Analog	Pin for bias setting resistor
20	AVSS_PLL1	Ground	Negative supply of PLL(2)
21	XTAL1	Analog	Xtal oscillator ports
22	XTAL2	Analog	
23	RST	Digital input	Reset
24	IRQ	Digital input	SPI interrupt request

1. For proper operation of the chip, this terminal must not be loaded by any external circuitry.
2. For proper operation of the chip, this terminal must be connected to a common ground plane.

4 Electrical

4.1 Absolute maximum ratings

Table 4 summarizes the absolute maximum rating for the STBLC01. Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond the specified electrical characteristics may affect device reliability or cause malfunction. The STBLC01 is available in a green-mold and lead free QFN 5x5 package. The maximum soldering conditions are specified as in the JEDEC J-STD-020C standard.

Table 4. Absolute maximum ratings

Parameter	Symbol	Min.	Max.	Unit
System ground	GND	-0.2	0.2	V
Supply voltage	V_{SUP}	GND-0.2	3.6	V
Voltage at remaining pin	V_{PIN}	GND-0.2	V_{SUP}+0.2	V
Storage temperature	T_{st}	-50	150	°C
Electrostatic discharge referred to GND according to Mil-Std-883C, method 3015.7	V_{ESD}	-2000	+2000	V

4.2 Handling procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level unless otherwise specified.

4.3 General operating conditions

The general operating conditions for both STBLC01 versions are summarized in *Table 5*. These parameters are specified based on the component list and on the application schematic of *Figure 4*.

Table 5. STBLC01 general operating conditions

Parameter	Min.	Typ.	Max.	Unit
Supply voltage	1.9	3	3.6	V
Temperature range	-40		+85	°C

4.4 Electrical characteristics

4.4.1 Current consumption

This section summarizes the estimated current consumption of the STBLC01 at pin VCC. The parameters defined in *Table 6* are specified based on the component list defined in *Table 2* and on the application schematic of *Figure 4*. Functional modes used in the table are defined in *Section 5.3*. Unless otherwise specified, the voltage VCC is set to 2.5 V.

Table 6. Typical current consumption

Parameter	Symbol	Min.	Typ.	Max.	Unit
Off mode	I_{off}	-	9	-	µA
Sleep mode	I_{sleep}		19		µA
Idle mode	I_{idle}		200		µA
BLE transmit mode for 0 dBm output power	I_{tx}		12.1		mA
BLE receive mode	I_{rx}		12.9		mA
BLE sleep mode (crystal)	$I_{BLEsleep\_crystal}$		450		µA
BLE sleep mode (RC)	$I_{BLEsleep\_RC}$		60		µA

4.5 I/O characteristics

This section summarizes the I/O characteristics.

Table 7. I/O characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
HIGH level input voltage	V_{IH}	0.75*Vcc	-	Vcc	V
LOW level input voltage	V_{IL}	0		0.25*Vcc	V
Output HIGH current	I_{OH}	1			mA
Output LOW current	I_{OL}	1			mA

4.6 RF characteristics

This section summarizes the RF characteristics of the STBLC01. All parameters are based on the components in *Table 2* and on the application schematic of *Figure 4*. Unless otherwise specified, VCC = 2.5 V. Measurement conditions and device configuration are specified in [3] for PHY parameters and in [4] for LL parameters. When applicable, exceptions for some parameters are compliant to that described in [2], volume 6, part A.

Table 8. General RF characteristics

Parameter	Note	Min.	Typ.	Max.	Unit
Operating frequency	-	2400		2484	MHz
Differential antenna impedance			200		W
On-air data rate			1000		Kbps
Channel spacing			2		MHz
Crystal frequency			26		MHz
Crystal frequency accuracy(1)				±50	ppm

1. Frequency accuracy includes initial tolerance, stability over temperature range and aging of the quartz.

Table 9. Transmitter characteristics

Parameter	Note	Min.	Typ.	Max.	Unit
Output power for the lowest power setting		-	-18		dBm
Output power for the highest power setting			+3		dBm
RF power accuracy			±3		dB
Power transmitted at frequency offset $\|f_{offs}\|$ = ±2 MHz				-20	dBm
Power transmitted at frequency offset $\|f_{offs}\|$ = ±3 MHz				-30	dBm
Frequency deviation	(1)		±250		kHz
Deviation from the channel center frequency				±150	kHz
Frequency drift for any packet length				50	kHz
Drift rate				400	Hz/µs
Spurious emission f in the ranges – 30 MHz – 88 MHz – 88 MHz – 230 MHz – 230 MHz – 470 MHz – 470 MHz – 862 MHz – 862 MHz – 960 MHz – 960 MHz – 2396 MHz – 2487.5 MHz – 12750 MHz	(2)		 -57.3 -54.0 -51.3 -54.0 -51.3 -43.4 -43.4		dBm

1. Frequency deviation corresponding to a 10101010 sequence is at least 80% of the frequency deviation corresponding to a 00001111 sequence. Positive frequency deviations represent a logic level ‘1’ and negative frequency deviations represent a logic level ‘0’ as defined in [2], volume 6, part A, section 3.1
2. Measuring conditions and signal specifications are described in [3], [4] and [5]. These parameters are highly related to a correct matching network and PCB design. Refer to *Section 8* for design guidelines.

Table 10. Receiver characteristics

Parameter	Note	Min.	Typ.	Max.	Unit
Sensitivity level for 0.1% BER			-80		dBm
Maximum input power for 0.1% BER			-5		dBm
Spurious emission for 30 MHz < f < 1 GHz	(1)			-57	dBm
Spurious emission f > 1 GHz	(1)			-47	dBm
In band blocking C/I for a wanted signal level of -67 dBm: – Co-channel interference – Interference at frequency offset foffs = 1 MHz – Interference at frequency offset foffs = 2 MHz – Interference at frequency offset foffs = 3 MHz – Interference at image frequency foffs = -4 MHz – Interference at adjacent frequencies to image				 21 15 -17 -27 -9 -15	dBm
Out of band blocking for a required signal level of -67 dBm: – Frequency range 30-1999 MHz – Frequency range 2000-2399 MHz – Frequency range 2484-2999 MHz – Frequency range 3000-12750 MHz		 -30 -35 -35 -30			dBm

1. Measuring conditions and signal specifications are described in [3], [4] and [5]. These parameters are highly related to a correct matching network and PCB design. Refer to *Section 8* for design guidelines.

4.7 Timing characteristics

Table 11. Timing characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Start-up time (power up to standby mode)	$T_{start\text{-}up}$	-	-	15.5	-	ms
Sleep => Standby mode(1)	T_{sleep_std}		-	2.6	-	ms
Off => Standby mode(2)	T_{off_std}		-	2.7	-	ms

1. This time is dominated by the Xtal oscillator startup.
2. This time is dominated by the Xtal oscillator startup.

5 Functional description

5.1 STBLC01 startup

This section describes the STBLC01 startup procedure. The description is intended to be informational only, as it is independent of any external actions. That application does however select the preferred communication interface by setting the pin SEL[a] (SEL = 1 SPI, SEL = 0 UART).

5.1.1 Startup

When a 3 V battery is connected to the STBLC01, an internal RC oscillator starts up, providing a clock with fixed duty-cycle to the power check circuit. After the power check indicates enough voltage on VDD, the Xtal oscillator is enabled and when its startup procedure is completed, the main logic can use the Xtal clock as reference.

5.1.2 End of the boot-up procedure

Once the XTAL oscillator clock is available to the digital part of the controller, the STBLC01 enters idle state and an event is sent to the host through the selected communication interface. Refer to *Section 6* for a complete description of how to send commands and read events from the STBLC01.

At the end of the boot sequence, the STBLC01 returns an event STBLC_POWER_MODE_IDLE to the host to notify that the system has entered in Idle mode. If for any reason the first HCI event is corrupted after start-up, for example if the host needs a long time to initialize or if the SEL signal is not stable at start-up time, it is recommended that the host generates an additional reset to ensure a proper start-up.

5.2 STBLC01 power modes

The STBLC01 can be configured to work in three main power modes which are automatically chosen based on the selected chip state described in *Section 5.3*. These modes are, however, not directly selectable by application. For this reason this section is intended to be informational.

5.2.1 Standby mode

In this mode the Xtal is up and running and is the main clock source of the system. The internal RC oscillator is active.

5.2.2 Xtreme mode

In Xtreme mode, the Xtal oscillator is turned off but the internal RC is kept on. The supply voltage of the logic is lowered to reduce the effect of leakage. The complete controller status is kept.

a. In order to avoid issues at boot-up due to interface selection, it is advisable to pull up (SPI) or pull down (UART) the pin SEL with a 10 kΩ.

5.2.3 OFF mode

In this mode, all internal oscillators are off. The supply voltage of the logic is lowered to reduce the effect of leakage. The complete controller status is kept.

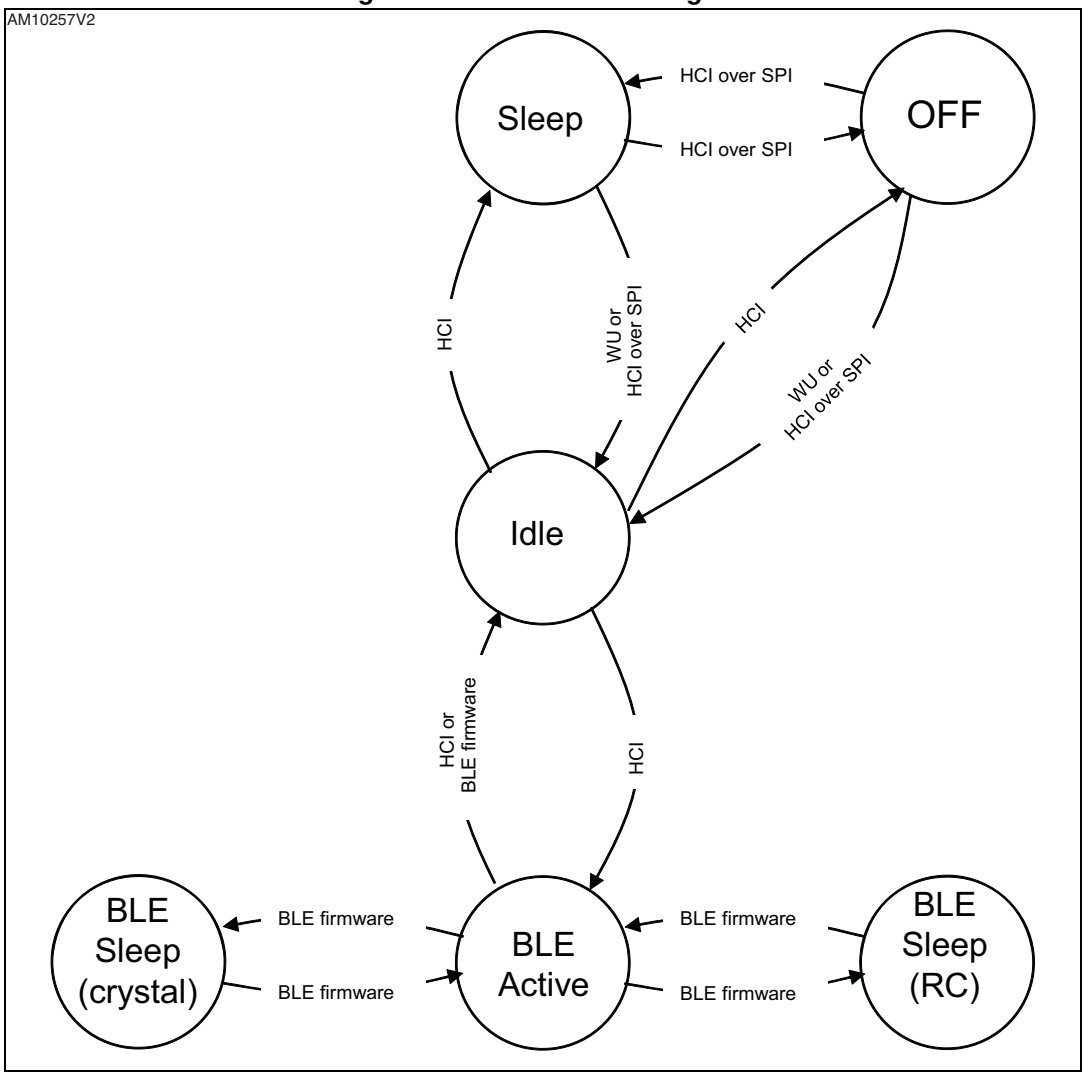
5.3 STBLC01 functional modes

5.3.1 State diagram

This part describes in which modes the STBLC01 can operate and how to switch from one mode to another. *Figure 6* shows a simplified state diagram of the STBLC01. The arrows indicate how the transaction from one state to the other can be achieved. Note that some operations in some states are only allowed for HCI over SPI transport layer, some others are achieved only by firmware.

As described in *Section 5.1*, after this initial step, the STBLC01 automatically enters Idle mode. Change of state is allowed through the HCI commands. In *Section 4.7* the time required to switch from one state to the other is defined.

Figure 6. STBLC01 state diagram



5.3.2 Idle mode

Idle is the mode that the STBLC01 enters as default after a reset. When this mode is entered, the HCI event STBLC_POWER_MODE_IDLE is reported to the host. The power mode for this configuration is Standby, as defined in *Section 5.2.1*. The HCI system is available and the host can communicate with the controller using the selected transport layer. The HCI is able to receive and decode any command sent by the host as well as send any event back to the host using either UART or SPI transport layers, according to the value of the SEL pin. Xtal is the clock source of STBLC01 logic. RF core is off in this state. The internal logic is in Halt mode, waiting for a HCI command from the host.

5.3.3 Sleep mode

Sleep mode is an STBLC01 low power mode. The power mode for this configuration is Xtreme, as defined in *Section 5.2.2*. RF cannot be activated from this state. When this mode

is exited, the STBLC01 goes into Idle mode. The HCI system is available but with limited functionality depending on the transport layer chosen:

- If UART has been chosen as transport layer, no HCI commands are accepted. The system can be woken up by setting the pin WU to high. Once this is done, the system restarts all internal oscillators and automatically goes into idle state asserting the STBLC_POWER_MODE_IDLE event.
- If SPI has been chosen as the transport layer, the STBLC01 is capable of executing a limited set of HCI commands with a limited speed. In particular, all commands which enable RF communications are not allowed in this mode. The flow control described in *Section 6.2.2* ensures that no overflow occurs in the communication. The HCI command STBLC_SET_POWER_MODE can be used to go into Standby mode.

5.3.4 Off mode

Off mode is the lowest STBLC01 power consumption mode. The power mode for this configuration is OFF as defined in *Section 5.2.3*. RF cannot be activated from this state. The HCI system is available but only to wake up the system. No HCI commands are accepted. When the system wakes up, the default mode is Idle. Depending on the transport layer chosen, the system can be woken up as follows:

- If UART has been chosen as the transport layer, the system can be woken up by setting the WU pin to '1'. Once this is done, the system restarts all internal oscillators and automatically goes into idle state, asserting the STBLC_POWER_MODE_IDLE event.
- If SPI has been chosen as the transport layer, the system can be woken up by sending any HCI command. Only a limited set of HCI commands are supported in this mode and with limited speed. In particular, all commands which enable RF communications are not allowed in this mode. Once the command has been received, the STBLC01 switches automatically in Sleep mode and tries to execute the command. The command STBLC_SET_POWER_MODE can be used to either go into Idle or into Off mode. In the first case the system restarts all internal oscillators and automatically goes into idle state asserting the STBLC_POWER_MODE_IDLE event. In the second case no special HCI event is sent but the STBLC01 returns in Off mode.

5.3.5 BLE active

BLE active is the mode where the STBLC01 is able to communicate to other BLE devices. This mode can be entered only from Idle mode. This mode represents the starting state for any Bluetooth low energy operation (scanning, advertisement, connection). The power mode for this configuration is Standby, as defined in *Section 5.2.1*. The HCI system is available and the host can communicate with the controller using the selected transport layer. HCI is able to receive and decode any command sent by the host as well as send any event back to the host using either UART or SPI transport layers, according to the value of the SEL pin. Xtal is the clock source of STBLC01 logic. Internal RC is calibrated during this phase. The RF core can be activated and controlled in order to optimize power consumption. The internal logic is in Halt mode, waiting for a HCI command from the host. In order to avoid possible noise coupling, it is highly recommended to reduce the host-controller communications when the on-air link is active.

5.3.6 BLE sleep (only for SPI transport layer)

BLE sleep mode is a special low power mode available only when the SPI transport layer is used. This mode can be enabled by the HCI command.

The STBLC01 offers two possible configurations for this mode: one employing the Xtal oscillator and another using the RC oscillator. When the Xtal oscillator is used, the high precision of the Xtal allows the STBLC01 to act as a master, slave, advertiser or scanner device. When the STBLC01 is a slave, advertiser or scanner device, the RC oscillator can be chosen, and the power consumption can be significantly reduced because the Xtreme power mode is used in that case.

The STBLC01 controls automatically the transitions between BLE Active and this mode; the host cannot influence them directly.

The use of the RC oscillator can be enabled using the HCI command STBLC_POWER_MODE_CONFIGURATION.

In this configuration, the RF core is turned off and the HCI system is active and able to receive any command.

- If UART has been chosen as transport layer, only the Xtal oscillator can be selected.
- If the transport layer is SPI, the Xtal oscillator or the RC oscillator can be selected.

5.4 STBLC01 reset structure

The STBLC01 has the following reset sources:

1. **Power On Reset (POR)**. This occurs after each power-up of the STBLC01. Once the boot-up procedure described in *Section 5.1* is completed, an STBLC_POWER_MODE_IDLE event is reported to the host, indicating that the STBLC01 has entered Idle mode. During POR, the RST pad is pulled to logic 0.
2. **RST pad**. The host can reset the STBLC01 by pulling up the RST pin for at least 5 ms. In this situation the STBLC01 reboots the firmware and an event STBLC_POWER_MODE_IDLE is sent as soon as the STBLC01 has entered Idle mode. The RST pad is pulled to logic 0 during POR.
3. **HCI reset**. Sending the standard BT command HCI_RESET, the host can reset the BLE functions of the STBLC01 as described in [*2*].

6 Host controller interface (HCI)

The STBLC01 includes a host controller interface as defined in [2], volume 2; part E. *Table 12* summarizes the command, *Table 13* the data format and *Table 14* the event format. A more detailed description of commands and events as well as all HCI related information can be found in [2].

Table 12. HCI command format

Byte #	Parameter	Size	Description
1	Packet_ID	1	Packet ID: packet Identifier – For HCI Command Packet_ID = 0x01
2-3	OpCode	2	OpCode is a unique identification of the command. It includes – OpCode Group Field (OGF) of 6 bits. Code 0x3F is reserved for Vendor command – OpCode Command Field (OCF) of 10 bits
4	Parameter_Total_Length	1	Lengths of all the parameters contained in the given command packet (N.B.: total length of parameters, not number of parameters)
	Parameter_0 ... Parameter_N		Each command has a specific number of parameters associated with it. These parameters and the size of each of the parameters are defined for each command. Each parameter is an integer number of octets in size

Table 13. HCI ACL data format

Byte #	Parameter	Size	Description
1	Packet_ID	1	Packet ID: Packet Identifier – For HCI Data Packet_ID = 0x02
2-3	Handle PB flag BC flag	2	Connection_Handle (12 bit) to be used for transmitting data packet or segment over primary controller. Range: 0x000-0xEFF (0xF00-0xFFF reserved for future use) Packet_Boundary_Flag (bit 4 and bit 5 of the second octet) Broadcast_Flag (bit 6 and bit 7 of the second octet)
4	Data_Total_Length	2	Length of data measured in octets.
	Data		ACL data (L2CAP PDU)

Table 14. HCI event format

Byte #	Parameter	Size	Description
1	Packet_ID	1	Packet ID: Packet Identifier – For HCI Event Packet_ID = 0x04
2	Event_Code	1	Each event is assigned a one-byte event code to uniquely identify different types of events. Range: 0x00 to 0xFF, where 0xFF is reserved for Vendor specific events.
3	Parameter_Total_Length	1	Lengths of all the parameters contained in the given event packet
	Event_Parameter_0		Each event has a specific number of parameters associated with it. These parameters and the size of each of the parameters are defined for each event. Each parameter is an integer number of octets in size.
	...		
	Event_Parameter_N		

In addition to standard commands, a set of HCI proprietary commands for dealing with the power modes and some parameters linked to RF performance are supported. The complete list of supported proprietary HCI commands is available in *Section 7*.

The STBLC01 supports the two different transport layers for HCI according to the level of the SEL pin:

1. SEL = 0: UART interface as defined in [*2*], volume 4, part A.
2. SEL = 1: SPI interface with proprietary flow control.

6.1 HCI UART transport layer

The STBLC01 contains a 2-pin UART compatible for communication protocol with 16450, 16550 and 16750 standards. The baud rate can be set by the host by sending the related HCI command (refer to *Section 7*). The default baud rate is 115.2 kbps.

6.1.1 UART interface

The UART interface is through the following pins:

- UART_RX: UART receiver line
- UART_TX: UART transmitting line

6.1.2 UART settings

The HCI UART transport layer uses the following settings for RS232:

- Baud rate: configurable via HCI
- The default baud rate is 115.2 kbps. The default value is only set by POR or the RST pin
- Number of data bits: 8
- Parity bit: no parity
- Start bit: 1 start bit
- Stop bit: 1 stop bit
- Flow control: not used

6.2 HCI SPI transport layer

The STBLC01 features a proprietary HCI SPI transport level which may allow the host/controller system to reach lower power consumption by using lower clock frequencies. HCI commands sent and events received over the SPI transport layer are identical to the ones sent/received over the UART transport level. The STBLC01 supports only slave mode SPI. The maximal SPI speed is 10 MHz. STBLC01 HCI events are signalled to host thought the assertion of the IRQ pin. When this occurs, the host sends a clock so that event can be read. Pin IRQ is also used to inform the host that the STBLC01 has data coming from RF communication to send. The procedures to read events or data are exactly the same.

6.2.1 SPI interface

The STBLC01 includes a 5-wire, 8-bit, MSB first, Motorola compatible with CPOL=0, CPHA=0 SPI interface. Only half-duplex transport is supported. The SPI interface is defined through the following pins:

- CSN: chip select signal. This signal is active low and it is mandatory, even when only 1 slave device is connected to the host
- SPI_SCK: SPI clock signal. When CSN is active, the host sends to the controller a number of clock cycles in multiples of 8 bits during each SPI transaction. When CSN is not active, the STBLC01 ignores any signal sent to this pin. This allows the host to set a clock signal to serve other devices
- SPI_MOSI: Host to controller transfer data line. The host generates data on the negative edge and samples data on the positive edge of the SPI_SCK signal. SPI data is sent in byte format, with the most significant bit (MSB) first.
- SPI_MISO: Controller to the host transfer data line. When CSN is active, controller generated data on the negative edge and sample data on the positive edge of the SPI_SCK signal. When CSN is inactive, the controller sets this output in tristate mode. SPI data is sent in byte format, with the most significant bit (MSB) first.
- IRQ: Interrupt request. This signal is set by the controller when an event needs to be sent to the host.

6.2.2 SPI flow control

The STBLC01 features a proprietary flow control for all communications over SPI both from the host to the controller and from the controller to the host. Each SPI transaction is done for 8 bits of data.

Host to controller flow

When the host needs to communicate with the controller, the following flow is followed:

1. Host sets the MOSI signal to '1'.
2. Host activates CSN after 100 ns.
3. Host polls MISO line. The first polling is done at least 100 ns after CSN is activated.
4. If MISO = '0' then the controller reception buffer is full and the host is not allowed to start the transaction.
5. If MISO = '1' then the controller reception buffer is not full and the host can start the transaction. After each set of 8 rising edges of SPI_SCK, the host polls the MISO line to check whether the controller reception buffer is not full. The first polling can be done on the first SPI_SCK falling edge.

Controller to host flow

When the controller needs to communicate with the host, the following flow is followed:

1. Controller sets IRQ line to '1'. This means that the controller has at least 1 byte of data to transmit.
2. Host pulls down the MOSI signal.
3. Host activates CSN after 100 ns.
4. Host starts an SPI transaction by sending a data byte equal to 0x00.
5. Host reads data sent by the controller on the MISO line.
6. If IRQ is set to '0' during an SPI transaction, then the controller has no other data to transmit. Once all bits of the transaction are read, the host can stop sending a clock.

7 Peripherals information

The STBLC01 includes several peripherals to fulfil all the requirements of the BLE standard. Although none of these peripherals are available for host use. This section gives a short description of STBLC01 internal peripherals to provide a better overview of the system.

7.1 AES

The STBLC01 includes a hardware encryption/decryption accelerator based on the advanced encryption system (AES) standard. For further information about AES please refer to the official page of NIST (http://csrc.nist.gov/CryptoToolkit/aes/).

This block provides the following functions:

1. BLE encryption key calculation
2. BLE message integrity code (MIC) calculation
3. BLE encryption stream generation

7.2 Random number generator (RNG)

The STBLC01 features an RNG block which is used to generate a non-deterministic bit stream as required in [2]. The result of this block is a non-deterministic 32-bit stream.

7.3 Battery level detector (SVLD)

The STBLC01 offers the possibility of monitoring the supply voltage of the system. The host can launch an SVLD measurement by sending the HCI command STBLC_SVLD_MEASUREMENT, as defined in *Section 9*. The measurement compares the supply voltage level with a predefined voltage level described in *Table 15*. After the measurement is completed, an event is reported to the host, as described in *Section 9.3.2*. All voltages specified in *Table 15* must be considered with a precision of ±10%.

Table 15. SVLD reference

Supply	Reference	Function
VCC	2.05 V	Battery low detection
	2.25 V	Battery low early warning