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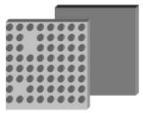
STLC2690

Bluetooth™ and FM transceiver system-on-chip

Datasheet - production data



WLCSP61R8

Features

- WLCSP 0.6 mm high, 0.4 mm pitch, lead-free/RoHs compliant, 61 pins
- 10 external components: 5 decoupling capacitors on the power supply, 1 B-BPF for Bluetooth, 1 inductor and 3 capacitors for FM RX
- PCB footprint < 36 mm^2
- Clocks
  - Fast clock input (digital or sine wave) at 13, 16, 16.8, 19.2, 26, 32, 33.6, 38.4, 52 MHz
  - Slow clock input at 32, 32.768 kHz
  - Direct external crystal input
- Power supply
  - Single power supply with internal regulators
- 1.65 V to 1.95 V I/O systems
- Various on-chip auto calibration features (VCO, Filters, …)

Description

The STLC2690 combines Bluetooth and FM transceiver functionality on a single chip and is fully optimized for mobile applications such as mobile phones, smart phones, PDAs and portable media players. The required board space has been minimized, power consumption levels are targeted for battery powered devices and the integration allows a cost effective solution. Amongst others the reduction of external components enables manufacturers to easily and fast integrate the STLC2690 on their product to enable a short time to market. Compared to its successful predecessor, the STLC2593, the STLC2690 is a system on chip device, it adds an FM transmitter, an audio processor and A2DP encapsulation and further optimizes in terms of RF performance and cost.

Table 1: Device summary

Order code	Package	Packing
STLC2690WTR	WLCSP61	Tape & Reel

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1 Introduction

The STLC2690 is a system-on-chip Bluetooth V3.0 transceiver and FM radio transceiver. The chip is packed in Wafer Level Chip Scale Package (WLCSP) of 0.6 mm high, 0.4 mm pitch.

The Bluetooth subsystem is the successor of the STLC2500D, a field-proven, single chip ROM-based Bluetooth solution for applications requiring integration up to HCI level. The STLC2690 supports in addition A2DP mediapacket encapsulation and SBC encoding/decoding. This allows to offload those functions from the Host for several use cases. Patch RAM is available, enabling multiple patches/upgrades and fast time to volume. The main interfaces are UART or SPI for HCI transport, PCM or I2S for voice and a WLAN coexistence interface. The radio has been designed specifically for single chip requirements, for low power and minimum BOM count.

The FM radio transceiver contains both a broadcast FM radio tuner and a broadcast FM radio transmitter for portable applications with worldwide FM band support. (De)multiplexing and (de)modulation are performed in a digital data path. A small embedded microcontroller manages the flexibility of the data path and the DSP parameters and takes care of the overall control of the transceiver. This microcontroller is also used for transmission and reception of the European Radio Data System (RDS) and the North American Radio Broadcast Data System (RBDS), including all required symbol decoding, block synchronization, error detection, and error correction functions. The FM can be controlled by the Host via a dedicated I2C interface or via the Bluetooth HCI interface. A Host-level API is offered in order to facilitate integration of the FM driver on the Host. Also a low-level API is supported.

The Bluetooth transceiver and FM transceiver are integrated on the same silicon, and they share at top-level power supplies, clocks and reset control. The chip integrates several regulators to generate the internally needed voltages from the Host platform supply input. The STLC2690 supports several use cases using simultaneous BT and FM and exchanging audio between the two subsystems.

For the Bluetooth transceiver, 5 decoupling capacitors and a band-pass filter are required as external BOM. For the FM transmitter, no external components are required, provided a loop antenna is used. For the FM receiver, 1 inductor and 3 capacitors are required. This results in a required PCB footprint smaller than 36 mm^2 (using 0201 components where possible and with a 0.3 mm spacing rule). The FM antenna matching network, which depends on the specific antenna implementation, is included in this footprint.

Bluetooth features

- Bluetooth™ specification compliance: V3.0
- Specific BT V3.0 features
  - Enhanced power control
  - Read encryption key size
- Adaptive frequency hopping (AFH)
- Channel quality driven data rate (CQDDR)
- Transmit Power
  - Power Class 2 and power Class 1.5 (above 4 dBm)
  - Programmable output power
- HCI
  - HCI H4 Transport Layer on UART and SPI
  - HCI proprietary commands (e.g. peripherals control)
  - Single HCI command for patch/upgrade download

  - (e)SCO over HCI
- Pitch-period error concealment (PPEC)
- Efficient and flexible support for WLAN coexistence scenarios
- Low power consumption
  - Ultra low power architecture with 3 different low-power levels
  - Deep sleep modes, including host-power saving feature
  - Dual wakeup mechanism
- Communication interfaces
  - UART (up to 4 MHz), SPI (up to 52 MHz), PCM/I2S, I2C
  - Up to 22 additional flexibly programmable GPIOs
  - External interrupts possible through the GPIOs
- Main processor
  - ARM7TDMI CPU
  - On-chip RAM, including provision for patches
  - On-chip ROM, preloaded with SW up to HCI and A2DP mediapacket encapsulation
- CoProcessor
  - Audio processor including RAM and ROM
  - ROM preloaded with SBC en-/decoding
- Ciphering support up to 128 bits key

FM receiver features

- Worldwide FM band (65.9 - 108 MHz)
- RDS/RBDS
- State of the art receiver sensitivity
- Excellent receiver selectivity for audio and RDS
- DSP-demodulation
- Adaptive signal processing, to provide best audio quality versus received signal quality or in-band blockers.
- Embedded microcontroller to control flexible DSP, to handle and (de)code RDS messages, supporting high-level and low level API
- Ultra fast checking for AF
- Analog and digital audio output
- Dual RF input with embedded FM TX/RX antenna switch to optimize for wire antennas and integrated antennas

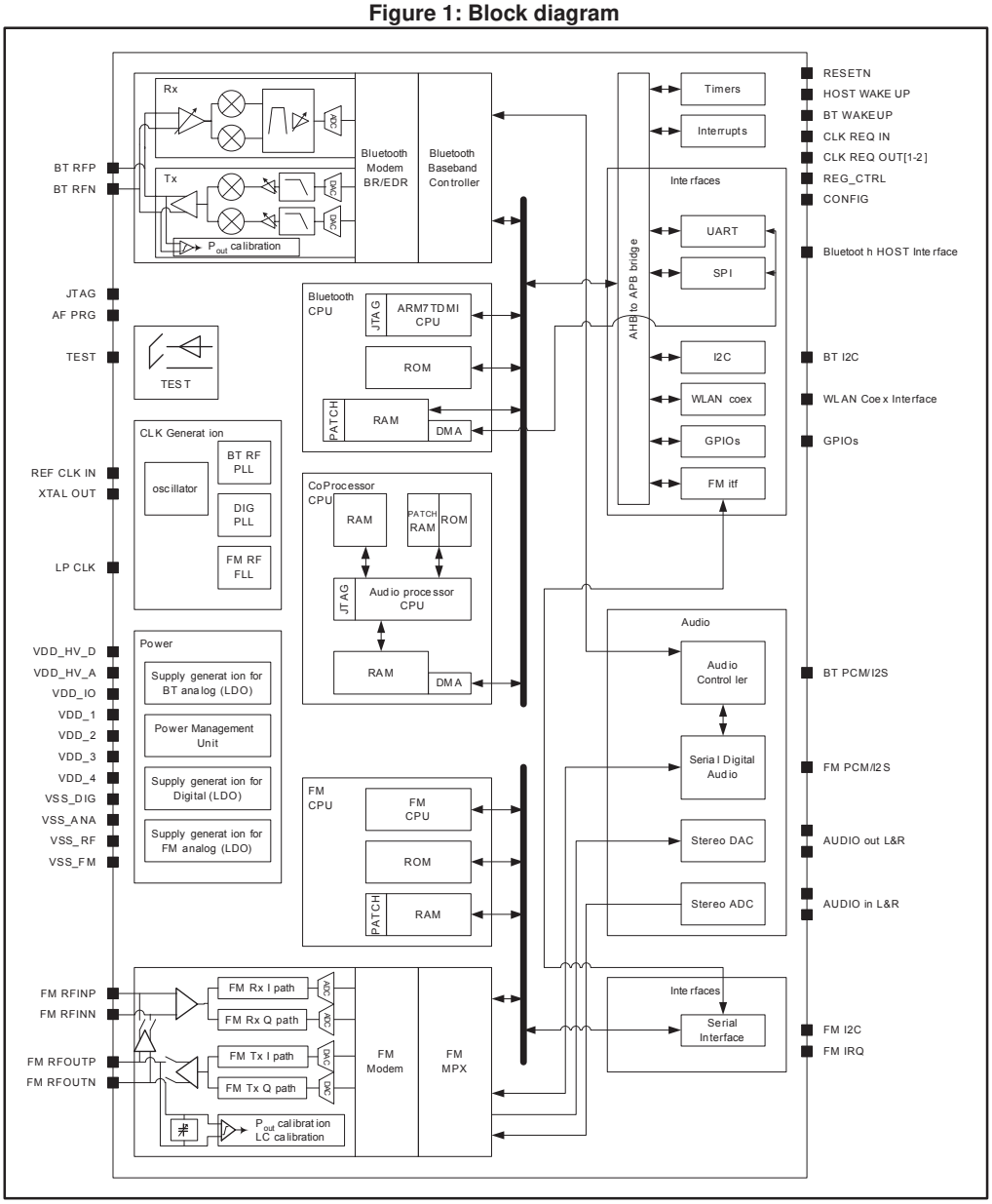
FM transmitter features

- Worldwide FM band (76 - 108 MHz)
- RDS/RBDS
- High output power (120 dBµVpdiff) linear transmitter
- Dual TX channel mode using AF list, with programmable separation
- SureTune™ to automatically select the optimal transmit frequency
- Embedded filtering for coexistence in mobile handset
- RF output optimized for integrated antennas
- Programmable AGC for optimized frequency deviation
- Programmable limiter to prevent over-modulation
- Highly flexible DSP (shared with FM RX)
- Embedded microcontroller (shared with FM RX)
- Analog and digital audio input

2 Generic description

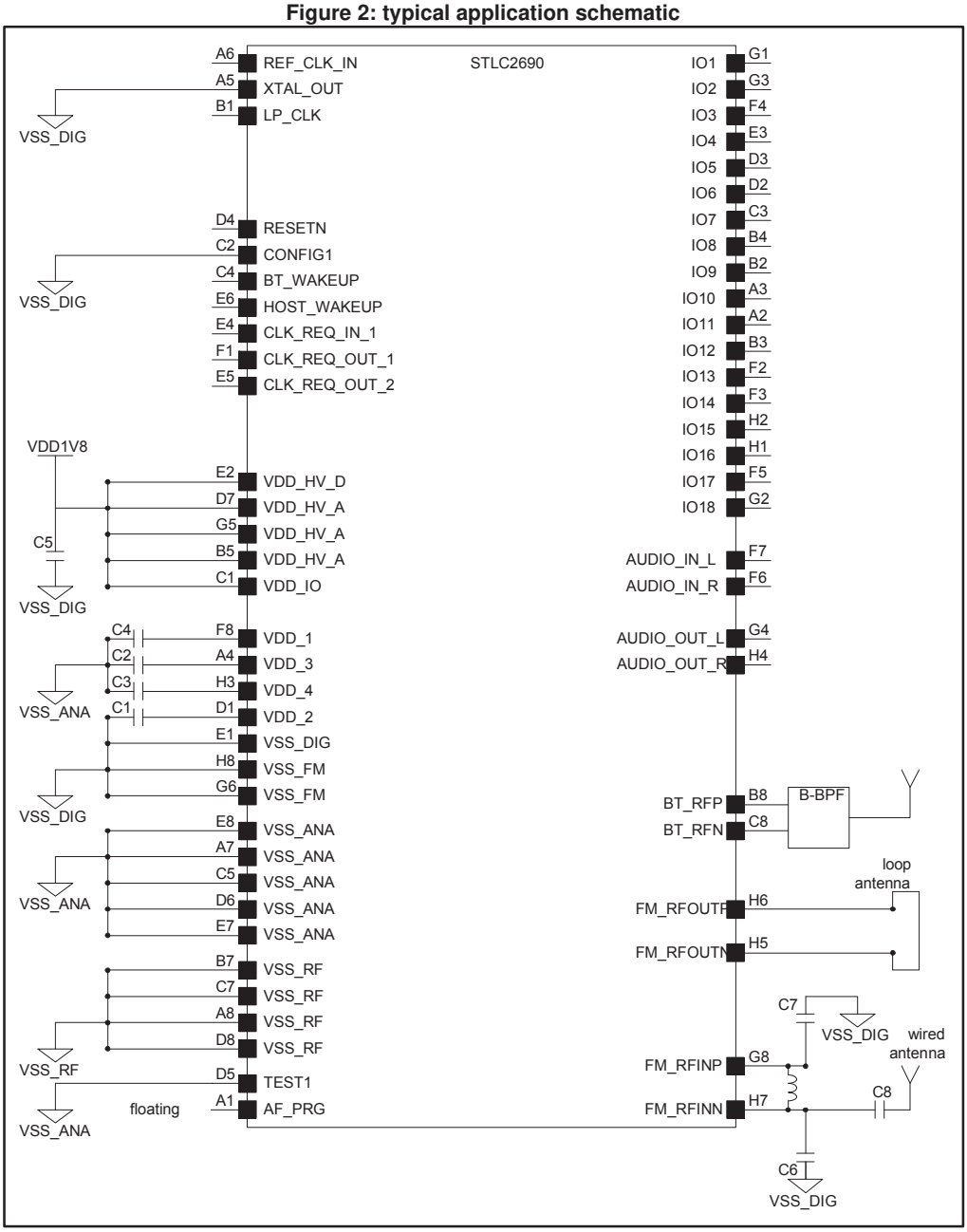
2.1 Block diagram

Figure 1: Block diagram



2.2 Application schematic

Figure 2: typical application schematic



For values of the components, refer to the HW manual.

Note that the application schematic shown is for a certain configuration. Other configurations are possible:

- The fast clock is provided from a digital or analog clock signal. This clock can also be generated from an external crystal directly connected to the chip, see *Section 3.6: "Clocks"*.

- FM RX is connected to a wired antenna. It can also be connected to the loop antenna, see *Section 5.2.1: "Dual RF input with RX/TX antenna switch"* for more details.
- VDD_HV_D, VDD_HV_A and VDD_IO are connected to the platform supply. Other configurations are possible, see *Section 3.5: "Power supply"*.
- The control signals and digital interfaces are not shown in the application schematic, since they depend on which digital interfaces are used in the application. See *Section 3.4: "Pinout"* and *Section 3.5: "Power supply"*.

2.3 Electrical data

VDD_HV_x means VDD_HV_A and VDD_HV_D.

2.3.1 Absolute maximum ratings

The absolute maximum rating (AMR) corresponds to the maximum value that can be applied without leading to instantaneous or very short-term unrecoverable hard failure (destructive breakdown).

Table 2: Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
VDD_HV_x	Core supply voltages (in case of pre-regulated power supply from the platform)	-0.3	2.5	V
VDD_IO	Supply voltage I/O	-0.3	2.5	V
Vin	Input voltage on any digital pin	-0.3	2.5	V
Vssdiff	Maximum voltage difference between different types of Vss pins.	-0.3	0.3	V
Tstg	Storage temperature	-65	+150	°C

2.3.2 Operating ranges

Operating ranges define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not guaranteed.

Table 3: Operating ranges

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{amb}	Operating ambient temperature	-40	25	+85	°C
VDD_HV_x	Core supply voltages (in case of pre-regulated power supply from the platform)	1.65	1.8	1.95	V
VDD_IO	I/O supply voltage	1.65	1.8	1.95	V

2.3.3 I/O specifications

The I/Os comply with the EIA/JEDEC standard JESD8-B.

Table 4: DC input specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	-0.2		0.35 * VDD_IO	V
V_{IH}	High level input voltage	0.65 * VDD_IO		(VDD_IO + 0.2) and (≤ 2.0)	V

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{in}	Input capacitance, including package[1]			5	pF
R_{pu}	Pull-up equivalent resistance (with V_{in} = 0 V)		50		kΩ
R_{pd}	Pull-down equiv. resistance (with V_{in} = VDD_IO)		50		kΩ
V_{hyst}	Schmitt trigger hysteresis	150			mV

Notes:

(1) Typical input capacitance without package is 0.9 pF.

Table 5: DC output specification

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OL}	Low level output voltage	Id = X[1] mA			0.2	V
V_{OH}	High level output voltage	Id = X[1] mA	VDD_IO - 0.2			V

Notes:

(1)X is the source/sink current under worst-case conditions according to the drive capabilities (see *Section 3.4.1: "Pinout"*).

2.3.4 Clock specifications

For more details on the clocks see *Section 3.6: "Clocks"*.

Table 6: Fast clock supported frequencies

Symbol	Parameter	Values	Unit
F_{IN}	Clock input frequency list	13, 16, 16.8, 19.2, 26, 32, 33.6, 38.4, 52	MHz

Table 7: Fast clock overall specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{INTOL}	Tolerance on input frequency	-20		20	ppm

Table 8: Fast clock, sine wave specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VPP	Peak to peak voltage range	0.2	0.5	1.8	V
NH	Total harmonic content of input signal			-25	dBc
ZINRe	Real part of parallel input impedance at pin	30	100		kΩ
ZINIm	Imaginary part of parallel input impedance at pin		2	4.7	pF
ZIDRe	Change in real part of parallel input impedance at pin, when changing mode (expressed in equivalent parallel resistance added or removed)	150			kΩ
ZIDim	Change in imaginary part of parallel input impedance at pin, when changing mode (expressed in equivalent parallel capacitance added or removed)			500	fF
	Phase noise @ 10 kHz			-130	dBc/ Hz

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Phase noise @ 100 kHz			-135	dBc/ Hz

Table 9: Fast clock, digital clock AC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{RISE}	10% - 90% rise time			70% of the clock period	ns
T_{FALL}	90% - 10% fall time			70% of the clock period	ns
D_{CYCLE}	Duty cycle	35	50	65	%
	Phase noise @ 10 kHz			-130	dBc/ Hz
	Phase noise @ 100 kHz			-135	dBc/ Hz

Table 10: Slow clock specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{IN}	Clock input frequencies	32, 32.768			kHz
	Duty cycle	30		70	%
	Tolerance on input frequency	•-250		250(1)	ppm
V_{IL}	Low level input voltage			0.35 * VDD_IO	V
V_{IH}	High level input voltage	0.65 * VDD_IO			V
V_{hyst}	Schmitt trigger hysteresis	150			mV
C_{IN}	Input capacitance			5	pF
T_{RISE}	10% - 90% rise time (1)			500	ns
T_{FALL}	90% - 10% fall time(2)			500	ns
	Total jitter(3)			250(3)	ppm

Notes:

(1) For use of the slow clock for FM, in case the accuracy of the externally applied slow clock is not sufficient, the STLC2690 provides a calibration mechanism to calibrate the slow clock versus the fast clock.

(2) The rise and fall time are not the most important parameters for the slow clock input due to the Schmitt trigger logic. It is more important that the noise on the slow clock line remains substantially below the hysteresis in amplitude.

(3) The total jitter is defined as the error that can appear on the actual frequency between two clock edges compared to the perfect frequency. Due to this, the total jitter value must contain the jitter itself and the error due to the accuracy on the clock frequency. The lower the accuracy, the smaller the jitter is allowed to be.

2.3.5 Current consumption

Current consumption of the Bluetooth subsystem

(Tamb = 25 °C, 26 MHz digital clock, 4 dBm output power for BR packets, 3 dBm output power for EDR packets, VDD_HV_x = VDD_IO = 1.8 V. With HCI interface in sleep mode.)

Table 11: Current consumption - Bluetooth subsystem

State	Typ.	Unit
Complete power down	1	µA
Deep Sleep mode	18	µA
Functional Sleep mode(1)	1.47	mA
HW Inquiry scan (1.28 s period, 11.25 ms window), combined with H4 UART Deep Sleep mode (*Section 4.3.1: "HCI transport layer"*)	210	µA
HW page scan (1.28 s period, 11.25 ms window), combined with H4 UART Deep Sleep mode (*Section 4.3.1: "HCI transport layer"*)	210	µA
HW inquiry and page scan (1.28 s period, 11.25 ms window), combined with H4 UART Deep Sleep mode (*Section 4.3.1: "HCI transport layer"*)	390	µA
Sniff mode (1.28 s, 4 attempts, 0 timeouts), combined with H4 UART Deep Sleep mode (*Section 4.3.1: "HCI transport layer"*) - Master - Slave	 79 105	 µA µA
Idle ACL connection - Master - Slave	 2.9 4.9	 mA mA
Active: data: DH1/DH1 symmetrical transfer (172.8 kbps), Master or Slave	21	mA
Active: data: DH5/DH1 asymmetrical transfer (TX 723.2 kbps & RX 57.6 kbps), Master or Slave Active: data: DH5/DH5 symmetrical transfer (433.9 kbps), Master or Slave	30.7 27.1	mA mA
Active: data: 2-DH5/2-DH5 symmetrical transfer (869.7 kbps), Master or Slave	28	mA
Active: data: 3-DH5/3-DH5 symmetrical transfer (1306.9 kbps), Master or Slave	28	mA
Active: audio: HV3, Master, not sniffed	8.7	mA
Active: audio: HV3, Slave, Sniff (1.28 s, 2 attempts, 0 timeouts)	8.3	mA
Active: audio: eSCO (EV3), (64 kbps symmetrical, T_{SCO} = 6) - Master - Slave (1 retransmission)	 9 9.4	 mA mA
Active: audio: eSCO (2-EV3), (64 kbps symmetrical, T_{SCO} = 12) - Master - Slave (1 retransmission)	 5.9 5.4	 mA mA
Active: audio: eSCO (3-EV3), (64 kbps symmetrical, T_{SCO} = 18) - Master - Slave (1 retransmission)	 5 4.3	 mA mA

Notes:

(1) In functional Sleep mode, the baseband clock is still running.

Current consumption of the FM subsystem

(Tamb = 25 °C, VDD_HV_x = VDD_IO = 1.8 V. With HCI interface in sleep mode. Using dedicated I2C and I2S interfaces. FM in mono operation. Using the HCI interface for control would add typically the Sleep mode current of the Bluetooth subsystem except if the HCI interface is put in Sleep mode.)

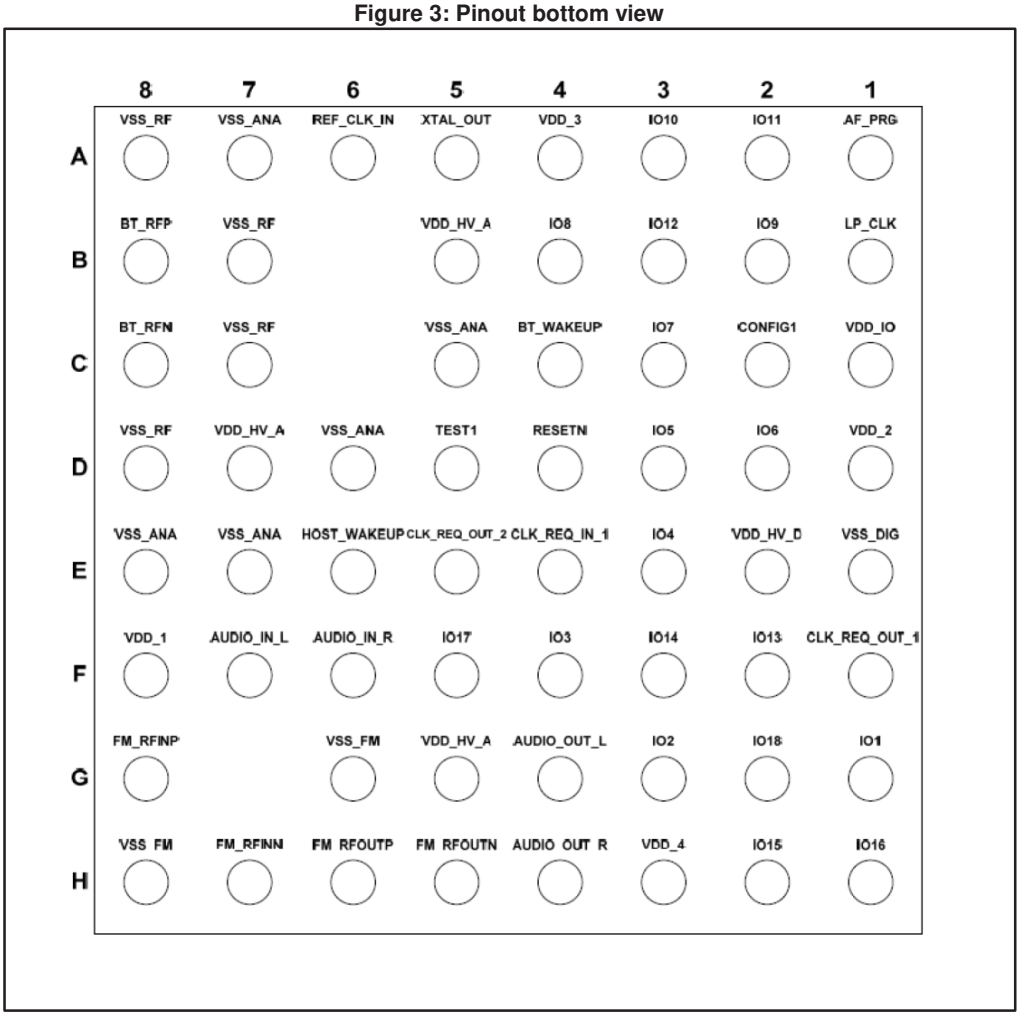
Table 12: Current consumption - FM subsystem

State	Typ.	Unit
Complete power down	1	µA
Active RX on slow clock	15	mA
Active TX (at 120 dBµVpdiff output power)	21	mA

2.4 Pinout

2.4.1 Pinout

Figure 3: Pinout bottom view



2.4.2 Pin list

Table 13: "The STLC2690 pin list (functional and supply)" shows the pin list of the STLC2690 during and after reset.

In columns “Reset” and “Default after reset”, the “PD/PU” shows the pads implementing an internal pull-down/up.

The column “Reset” shows the state of the pins during hardware reset; the column “Default after reset” shows the state of the pins after the hardware reset state is left, but before any Host activity on the Host interface and before the SW Parameter File download.

The column “Type” describes the pin directions:

- I for Input (All digital inputs have a Schmitt trigger function.)
- O for Output
- I/O for Input/Output (All digital inputs have a Schmitt trigger function.)
- O/t for tri-state output

For the output pins the default drive capability is 2 mA, except for the pins HOST_WAKEUP, IO7, IO9 and IO11 where it is 8 mA.

Table 13: The STLC2690 pin list (functional and supply)

Name	Pin#	Type	Description	Function during and after reset	Reset(1)	Default(2) after reset
Clock signals						
REF_CLK_IN	A6	I	Fast clock input when XTAL_OUT is strapped to VSS_DIG Otherwise XTAL input		Input	Input
XTAL_OUT	A5	I/O	Strapped to VSS_DIG when fast clock on REF_CLK_IN Otherwise XTAL feedback			
LP_CLK	B1	I	Slow clock input		Input	Input
Digital control signals						
RESETN	D4	I	Global reset – active low		Input	Input
CONFIG1	C2	I	Configuration pin, strapped to VSS_DIG		Input = 0	Input = 0
BT_WAKEUP	C4	I	Wake-up signal to Bluetooth (active high), should be strapped to VSS_DIG if not used		Input	Input
HOST_WAKEUP	E6	I/O(3)	Programmable pin	HOST_WAKEUP / SPI_INT	Input PD	Output low
CLK_REQ_IN_1	E4	I/O(3)	Programmable pin	CLK_REQ_IN	Input PD	Input PD
CLK_REQ_OUT_1	F1	I/O(3)	Programmable pin	CLK_REQ_OUT	Input PD	Output high
CLK_REQ_OUT_2	E5	I/O(3)	Programmable pin	CLK_REQ_OUT_N	Input PU	Output low
Digital interfaces						
IO1	G1	I/O(3)	Programmable pin	UART_RXD	Input PU	Input PU
IO2	G3	I/O(3)		UART_TXD	Input PU	Output high
IO3	F4	I/O(3)		UART_CTS	Input PU	Input PU

Name	Pin#	Type	Description	Function during and after reset	Reset(1)	Default(2) after reset
IO4	E3	I/O(3)		UART_RTS	Input PU	Output high
IO5	D3	I/O(3)	Programmable pin	SPI_CLK	Input PD	Input PD
IO6	D2	I/O(3)		SPI_DI	Input PD	Input PD
IO7	C3	I/O(3)		SPI_DO	Input PD	Tristate PD
IO8	B4	I/O(3)		SPI_CSN	Input PU	Input PU
IO9	B2	I/O(3)	Programmable pin	Not used	Input PD	Input PD
IO10	A3	I/O(3)		Not used	Input PD	Input PD
IO11	A2	I/O(3)		Not used	Input PD	Input PD
IO12	B3	I/O(3)		Not used	Input PD	Input PD
IO13	F2	I/O(3)	Programmable pin	FM_I2C_CLK	Input PU	Input PU
IO14	F3	I/O(3)		FM_I2C_DATA	Input PU	Input PU
IO15	H2	I/O(3)	Programmable pin	Not used	Input PD	Input PD
IO16	H1	I/O(3)		Not used	Input PD	Input PD
IO17	F5	I/O(3)		Not used	Input PD	Input PD
IO18	G2	I/O(3)		Not used	Input PD	Input PD
Bluetooth RF interface						
BT_RFP	B8	I/O	Differential Bluetooth RF port			
BT_RFN	C8	I/O				
FM RF interfaces						
FM_RFINP	G8	I	Differential FM RF input			
FM_RFINN	H7	I				
FM_RFOUTP	H6	I/O	Differential FM RF output and input, see *Section 5.2.1: "Dual RF input with RX/TX antenna switch"*			
FM_RFOUTN	H5	I/O				
Analog audio interfaces						
AUDIO_IN_L	F7	I	Left analog audio input			
AUDIO_IN_R	F6	I	Right analog audio input			
AUDIO_OUT_L	G4	I/O	Left analog audio output			

Name	Pin#	Type	Description	Function during and after reset	Reset(1)	Default(2) after reset
AUDIO_OUT_R	H4	I/O	Right analog audio output			
Power supply						
VDD_HV_D	E2		Power supply – Connect to platform supply			
VDD_HV_D	D7		Power supply – Connect to platform supply			
	G5					
	B5					
VDD_IO	C1		I/Os supply			
VDD_1	F8		Internal supply decoupling / Regulator output. Need 220 nF decoupling capacitor to VSS_ANA.			
VDD_2	D1		Internal supply decoupling / Regulator output. Need 220 nF decoupling capacitor to VSS_DIG.			
VDD_3	A4		Internal supply decoupling / Regulator output. Need 220 nF decoupling capacitor to VSS_ANA.			
VDD_4	H3		Internal supply decoupling / Regulator output. Need 220 nF decoupling capacitor to VSS_ANA.			
VSS_DIG	E1		Digital ground			
VSS_ANA	A7		Analog ground			
	E8					
	C5					
	E7					
	D6					
VSS_RF	B7		RF ground			
	C7					
	A8					
	D8					
VSS_FM	G6		FM ground			
	H8					
Other pins						
TEST1	D5		Test pin, to be strapped to VSS_ANA			
AF_PRG	A1	I/O	Test pin (leave unconnected)(4)		Open	Open

Notes:

(1) Pin behavior during HW reset (RESETN low).

(2) Pin behavior immediately after HW reset and internal chip initialization, but before any Host activity on the Host interface and the SW Parameter File download.

(3) Reconfigurable I/O pin. The functionality and type of these I/Os can be configured through different procedures (see *Section 3.4.3: "Pin mapping"*).

(4) Pin is ST-reserved for test function and it must be soldered to an isolated pad (not connected to anything, just floating).

2.4.3 Pin mapping

Some control signals and the digital interface pins are programmable pins, see . Different functions and different pull-up/down can be mapped on these pins. The control signals, digital interfaces and GPIOs of *Section 3.5: "Power supply"* can be mapped to these programmable pins.

Following procedure determines the final pin mapping.

- When using SPI as Host interface, the Host has the option to change the default settings of the SPI by writing in the SPI configuration register. One of the configurations is the mapping of the flow control, SPI_FLOW, to a pin.
- After reset, when the Host starts sending data over UART or SPI, this interface is recognized as being the Host interface. The I/Os are automatically remapped as indicated in *Section 7: "References"*.
- After the procedures described above are finished, a SW Parameter File can be downloaded to remap some of the pins and to configure pulls, see also *Section 4.1.7: "Download of the SW parameter file"*. This can also be done with HCI commands.

A detailed list of which functions map to which pins is available in *Section 7: "References"*.

2.5 Power supply

The chip runs from one single pre-regulated power supply from the platform for the core functions, VDD_HV_D (digital functions) and VDD_HV_A (analog functions), and one supply for the I/Os, VDD_IO. These supplies could be connected to the same platform supply or to different supplies. A decoupling capacitor is needed on these supplies. Also a dedicated regulator can be used, see *Section 3.5.1: "Dedicated STLC2690 regulator operation"*.

Internal regulators generate the core voltages. VDD_1, VDD_2, VDD_3, VDD_4 are the outputs of these internal regulators. Supply decoupling capacitors are needed on these outputs.

The grounds VSS_DIG, VSS_ANA, VSS_RF and VSS_FM have to be connected to the platform ground.

Specific layout guidelines need to be taken into account to ensure the full chip performance, see *[11]*.

For the absolute maximum ratings and operating conditions, see *Section 3.3.1: "Absolute maximum ratings"*.

2.5.1 Dedicated STLC2690 regulator operation

The signal REG_CTRL allows the control of an external battery regulator dedicated to the STLC2690. This regulator is meant to supply the STLC2690 with 1.8 V. It allows to partly decouple the core supply of the STLC2690 from the platform, while keeping the best implementation in terms of power consumption.

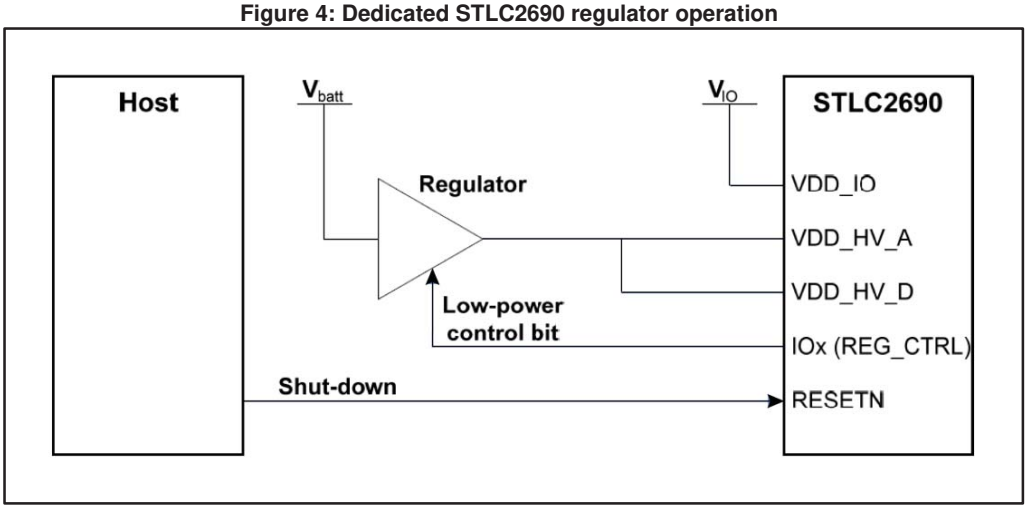
This mode requires a regulator that supports low power mode providing for two modes of operations:

- **Active mode**: High current/accuracy capability;
- **Low power mode**: Small current/lower accuracy, with internal consumption of a few µA.

The low power control bit of this regulator is connected to the REG_CTRL. When REG_CTRL = 0, the regulator is in low power mode, when REG_CTRL = 1, the regulator is in active mode.

The next picture gives an example of the connections. Possible decoupling capacitors are not shown on this drawing.

Figure 4: Dedicated STLC2690 regulator operation

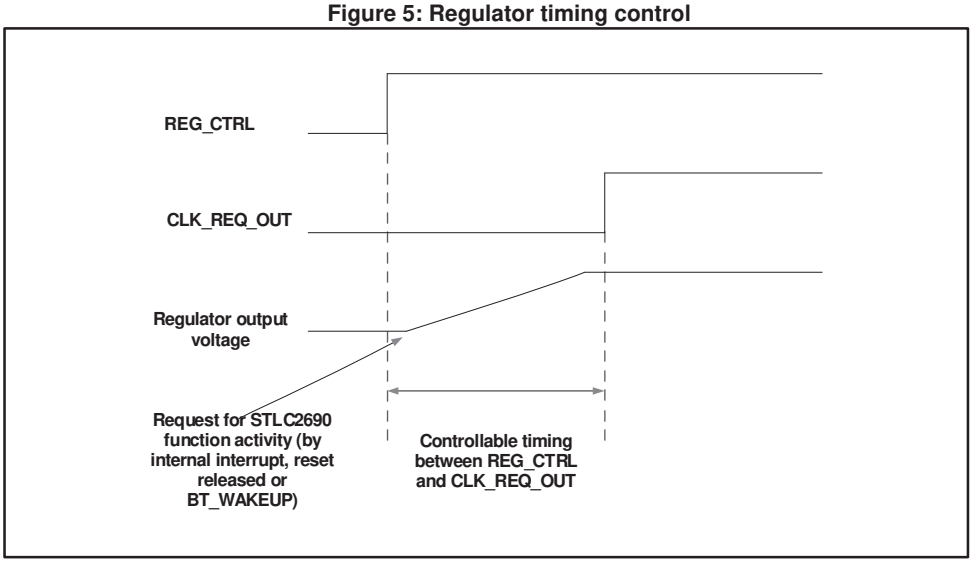


The low power mode usage or active mode of the external regulator is linked with the low power modes of the Bluetooth subsystem (Deep Sleep mode and Complete Power Down) and FM subsystem (Deep Sleep mode and Complete Power Down).

This means that REG_CTRL is low when the Bluetooth and FM subsystem go in low power mode and is high in all other cases.

Based on the time it takes for an external regulator to settle the voltage, the timing of REG_CTRL can be adjusted to become active before CLK_REQ_OUT_x is active. The picture below shows the behavior for both signals.

Figure 5: Regulator timing control



The timing of REG_CTRL is controllable between 0 and 30 ms in several steps and is set to 30 ms at startup. This parameter is defined via the SW Parameter File download and depends on the regulator and the platform behavior.

2.6 Clocks

2.6.1 Fast clock (system clock)

This clock is the main clock of the chip. It is used for most of the Bluetooth operation like transmission, reception, Host communication, ... The FM transmitter and receiver can work with this clock in all their modes. It is selected by an FM Parameter, whether the FM works with this clock (and requests it via CLK_REQ_OUT_x) or with the slow clock.

This clock needs only to be present when the STLC2690 is requesting it via CLK_REQ_OUT_x, see *Section 3.6.4: "Clock request signals"*. When the fast clock is generated from an external crystal directly connected to the chip, these clock request signals are not used.

This clock is provided to the chip either as a digital square wave input, a sinusoidal low amplitude signal, or is generated using an external crystal directly connected to the chip.

- When the clock is provided as a digital square wave or as an analog sine wave from the platform, the supported frequencies are 13, 16, 16.8, 19.2, 26, 32, 33.6, 38.4 and 52 MHz. The clock input pin is REF_CLK_IN. In this case the XTAL_OUT should be strapped to ground.
- When the fast clock is generated from an external crystal directly connected to the chip, the supported crystal frequencies are 13, 16, 16.8, 19.2, 26, 32, 33.6 and 38.4 MHz. The integrated oscillator cell supports the crystal characteristics listed in the table below. The input pin of the crystal is REF_CLK_IN, the feedback pin of the crystal is XTAL_OUT.

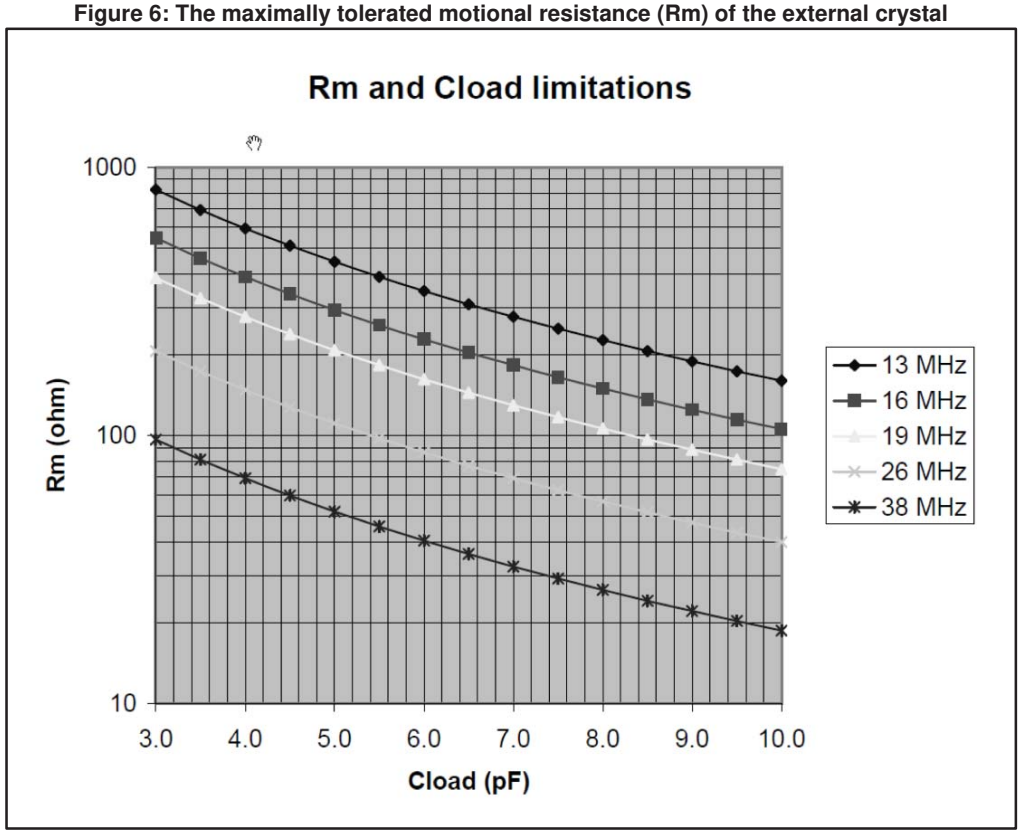
For detailed characteristics, see *Section 3.3.4: "Clock specifications"*.

Table 14: External crystal characteristics

Specification	Min.	Typ.	Max.	Unit
Initial crystal frequency accuracy			± 25	ppm
Crystal pullability	10		150	ppm/pF
Crystal drift (aging & temperature drift)			± 15	ppm

The maximally tolerated motional resistance (R_m) of the crystal depends both on the frequency and load capacitance seen by the crystal, as shown in *Figure 6: "The maximally tolerated motional resistance (Rm) of the external crystal"*.

Figure 6: The maximally tolerated motional resistance (Rm) of the external crystal



2.6.2 Slow clock (low power clock)

This clock is used for the low power modes support of BT. The FM transmitter and receiver can work with this clock in all their modes. It is selected by an FM parameter, whether the FM works with this clock or with the fast clock.

After power-up, the slow clock must be available before the reset is released. It must remain active all the time until the chip is powered off.

This clock is provided to the chip through a standard digital input, LP_CLK, with default characteristics. The input contains a Schmitt trigger and does not contain any pull, see also .

The slow clock can be 32 kHz or 32.768 kHz with an accuracy of ±250 ppm. For detailed characteristics, see *Section 3.3.4: "Clock specifications"*.

For use of the slow clock for FM, in case the accuracy of the externally applied slow clock is not sufficient, the STLC2690 provides a calibration mechanism to calibrate the slow clock versus the fast clock.

2.6.3 Clock detection

An integrated automatic detection algorithm detects the system and slow clock frequencies after a hardware reset. The steps in the clock detection routine are:

- Identification of the fast clock frequency (13 MHz, 16 MHz, 16.8 MHz, 19.2 MHz, 26 MHz, 32 MHz, 33.6 MHz, 38.4 MHz, 52 MHz)
- Identification of the slow clock (32.768 kHz or 32 kHz)

- The slow clock frequency can be confirmed during parameter download and is mandatory if 32 kHz frequency is used

2.6.4 Clock request signals

To allow minimum power consumption, a clock request feature is available so that the fast clock (REF_CLK_IN) can be stopped when not needed by the Bluetooth or FM system. The clock request signal can be active high or active low, and the STLC2690 supports internal propagation of clock request signal coming from another device in the system. When the fast clock is generated from an external crystal directly connected to the chip, these clock request signals are not used.

Different configurations as described below are supported during reset and in all operation modes, provided that VDD_IO is available. For the propagation of the external request signal, both VDD_HV_D and VDD_IO need to be present.

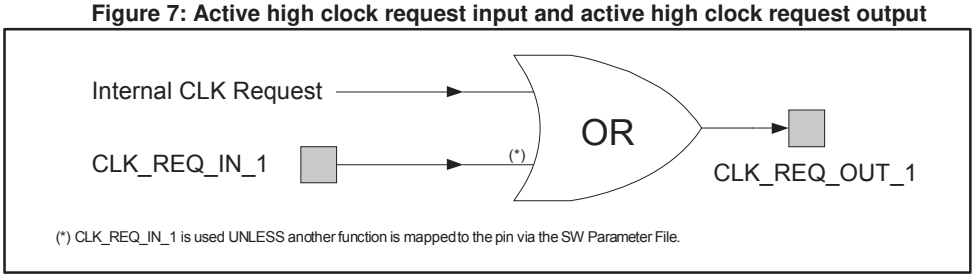
The clock request functionality is based on three different signals: CLK_REQ_OUT_1, CLK_REQ_OUT_2 and CLK_REQ_IN_1, with the following function. The signals are available depending on the pin mapping, see *Section 3.4.3: "Pin mapping"*.

- CLK_REQ_OUT_1: active high clock request output. Support for either push-pull or open drain output.
- CLK_REQ_OUT_2: active low clock request output. Support for either push-pull or open drain output.
- CLK_REQ_IN_1: active high clock request input from another device.

The following modes are supported:

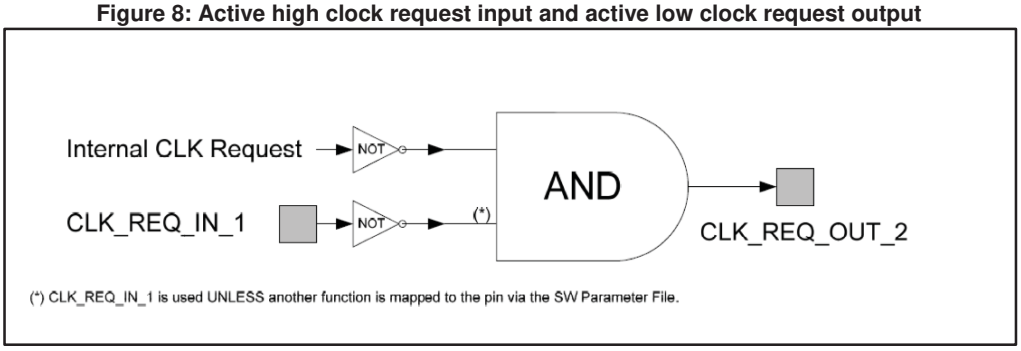
- Active high clock request input and active high clock request output:

Figure 7: Active high clock request input and active high clock request output



- Active high clock request input and active low clock request output:

Figure 8: Active high clock request input and active low clock request output



2.7 Reset and power-up

The behavior of the chip is independent of the power supplies (VDD_HV_x and VDD_IO) activation sequence.

In case of pre-regulated power supply from the platform, the RESETN pin should be active while powering up VDD_HV_x and should stay active at least two cycles of the slow clock (LP_CLK) after power-up is completed.

The chip is able to start without the fast clock being present. It requests it through CLK_REQ_OUT_x before using it.

The time between the Bluetooth subsystem making CLK_REQ_OUT_x active and the platform providing a stable clock should maximally be 15 ms. If the clock is starting faster on the platform, this timing can be reduced through parameter download.

As the FM radio and the Bluetooth are sharing the same reset pin in STLC2690, the start-up sequences of both functions are not completely independent. Hence, a typical start-up should be compliant with the sequence below:

- Supplies are powered up
- LP_CLK (slow clock) is running and stable
- RESETN pin is released after at least two LP_CLK cycles.
- After around 30 ms, CLK_REQ_OUT_x is set to request the fast clock (REF_CLK_IN).
- After 15 ms, REF_CLK_IN should be stable and the system can start using it. The SW is starting, doing clock recognition, internal configuration, and the HCI interface becomes operational.
- The host performs the SW Parameter File download of the Bluetooth subsystem. This allows the Bluetooth subsystem to correctly operate, but this allows also and mainly to set the device in the optimal power mode for the application in which it resides.
- From this point on, the Host can either decide to use Bluetooth only, or it can also start configuring or using the FM radio, either through the FM I2C interface, or through the BT HCI interface. The signals REG_CTRL and CLK_REQ_OUT_x indicate which supply is needed and whether the fast clock is needed or can be shut down.

However, it is possible to use the FM radio through the FM I2C interface without doing the Bluetooth SW Parameter File download.

2.8 Power down

The power down of the chip does not contain any constraints. It is possible to power-off VDD_IO and VDD_HV_x independently and in whatever order without resulting in increased static current consumption. If any of the two supplies is removed, the chip goes back to reset state. It is however recommended that the platform activates the RESETN at least 2 LP_CLK cycles before powering-off of the supplies.

2.9 Low power modes

2.9.1 Overview

The STLC2690 is designed for lowest power operation in all modes. To achieve this, several power modes are supported. Due to their different ways of operating (in bursts for Bluetooth, constant for FM), different low power modes are defined both for Bluetooth and FM as listed below.

On top of these internal power modes, and linked to them, the HCI interface also has the capability to be put in a low power mode (called Sleep mode). This is the only way for the Bluetooth subsystem of the system to go in Deep Sleep mode or Complete Power Down. When no data have to be transferred on the HCI interface for some time, the Host should place it in Sleep mode so that the power consumption is always minimized for the system.

Table 15: Bluetooth low power modes

Low power mode	Description
Sleep mode	The Bluetooth subsystem: - Accepts HCI commands from the Host. - Supports all types of Bluetooth links. - Can transfer data over Bluetooth links. - Dynamically switches between sleep and active mode when needed. - The fast clock is still active in part of the design. - Parts of the chip are dynamically powered off depending on the Bluetooth activity.
Deep sleep mode	The Bluetooth subsystem: - Does not accept HCI commands from the host. - Supports Page and Inquiry scans. - Supports Bluetooth links that are in Sniff or Sniff Subrating. - Dynamically switches between deep sleep and active mode during Bluetooth activity. The deep sleep mode entry is initiated by the Host, the Bluetooth subsystem acknowledges or not. The wake-up mechanism must be enabled by the SW Parameter File download before it can be used. - The fast clock is not active in any part of the design. - Parts of the chip are dynamically powered off depending on the Bluetooth activity.
Complete power down	The Bluetooth subsystem is effectively powered down: - No Bluetooth activity is supported. - The HCI interface is shut down. - The fast clock is not active in any part of the design. - Most parts of the chip are completely powered off. - RAM content is not maintained (initialization is required at wake-up). - Some pins (4 UART, CLKREQIN) keep their previous configuration (input or output, pull behavior) during Complete Power Down. - The host needs to send once an HCI command to allow the Bluetooth subsystem to go in Complete Power Down. The Bluetooth subsystem then goes into Complete Power Down each time the Host sends a Deep Sleep command and there is no activity anymore on the Bluetooth subsystem, this in order to ensure a smooth transition from active to Complete Power Down state. In order to go out of this mode, either a HW reset or BT_WAKEUP = ‘1’ is needed.

Table 16: FM low power modes

Low power mode	Description
Active mode	The FM radio is running and is either receiving or transmitting FM signal. The necessary logic for operation is powered and clocked. The user can define what operation mode is selected and can transfer audio or RDS data through I2C, I2S or analog audio interfaces.
Complete Power Down	The FM radio is not operating. FM radio restart is done either through a dedicated command through the FM I2C interface or through the BT HCI interface. Most parts of the FM radio are powered off to reduce leakage to the minimum. If SW download is necessary for FM operation, the SW needs to be downloaded again when going out of Complete Power Down mode. The switch between Active and Complete Power Down mode for FM is done on request of the Host.