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![ST logo]

STLC5048

Fully programmable four-channel codec and filter

Features

- Fully programmable monolithic 4-channel codec/filter
- Single +3.3 V supply
- A/m law programmable
- Linear coding (16 bits) option
- PCM highway format automatically detected: 1.536 or 1.544 MHz, 2.048, 4.096, 8192 MHz
- Two PCM ports available
- TX gain programming: 33 dB range; <0.01 dB step
- RX gain programming: 42 dB range; <0.01 dB step
- Programmable SLIC input impedance
- Programmable transhybrid balance filter
- Programmable equalization (frequency response)
- Programmable time slot assignment
- Digital and analog loopbacks
- SLIC control port static (16 I/Os), dynamic (12 I/Os + 4 CS)
- Built-in test mode with tone generation, MCU access to PCM data
- 64 TQFP (10x10mm) package
- Programmable SLIC line current limitation
- Programmable SLIC off-hook detection threshold

TQFP64 (10x10x1.4mm)
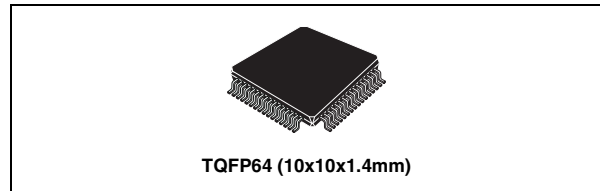
Description

The STLC5048 is a monolithic fully programmable 4-channel codec and filter. It operates with a single +3.3V supply.

The analog interface is based on a receive output buffer driving the SLIC RX input and on an amplifier input stage normally driven by the SLIC TX output. Due to the single supply voltage a mid-supply reference level is generated internally by the device and all analog signals are referred to this level (AGND). The PCM interface uses one common 8 kHz frame sync. pulse for transmit and receive direction. The bit clock is automatically detected between four standards: 1.563/1.544 MHz, 2.048 MHz, 4.096 MHz, 8192 MHz.

Two PCM port are provided: the channels can be connected to port A or/and B.

Device programmability is achieved by means of several registers and commands allowing to set the different parameters like TX/RX gains, line impedance, transhybrid balance, equalization (frequency response), encoding law (A/m), time slot assignment, independent channels power up/down, loopbacks, PCM bits offset.

The STLC5048 can be programmed via serial interface running up to 8 MHz. One interrupt output pin is also provided.

A GUI interface is also available to emulate and program the coefficients for impedance synthesis, echo cancelling and channel filtering.

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Figure 1. Block diagram
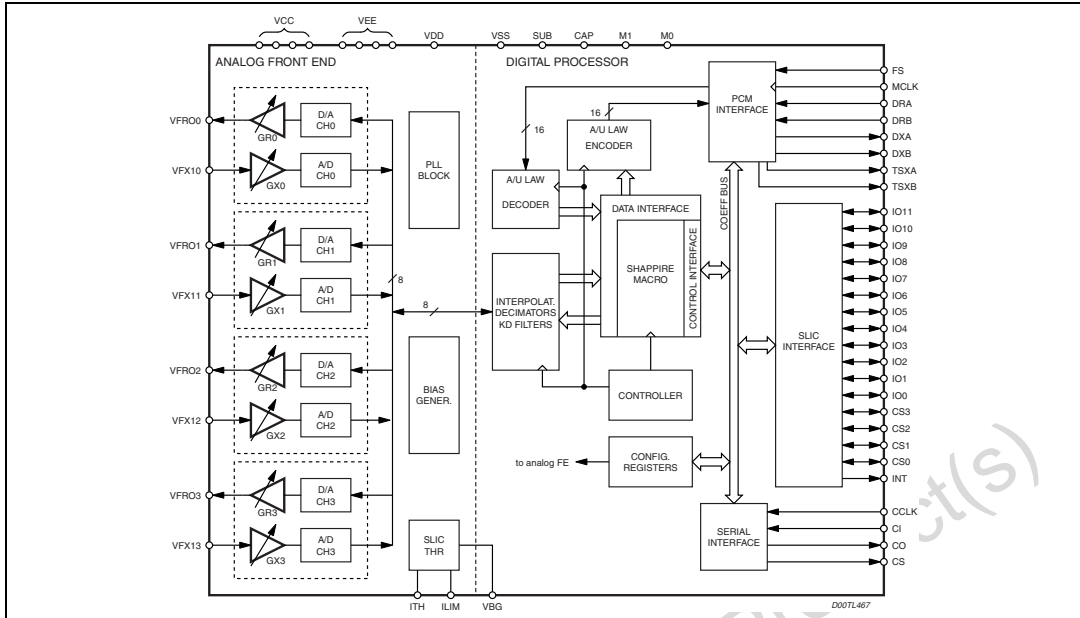
2   Absolute maximum ratings and operating conditions

Table 1.   Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to V_{EE}	4.6	V
V_{DD}	V_{DD} to V_{SS}	4.6	V
VD_{IN}	Digital input pin voltage	5.5	V
$VAin$	Analog input pin voltage ($V_{DD}=V_{CC}$; $V_{EE}=V_{SUB}$)	$V_{CC} + 0.5$; $V_{EE} - 0.5$	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_{LEAD}	Lead temperature (soldering, 10s)	300	°C

Table 2.   Operating range

Symbol	Parameter	Value	Unit
V_{CC} , V_{DD}	Supply voltage	3.3 +/- 5%	V
T_{OP}	Operating temperature range	-40 to +85	°C

Table 3.   Thermal data

Symbol	Parameter	Value	Unit
$R_{th\,j-amb}$	Thermal resistance junction-ambient	70	°C/W

3 Pin assignments and descriptions

Figure 2.   Pin assignments (top view)
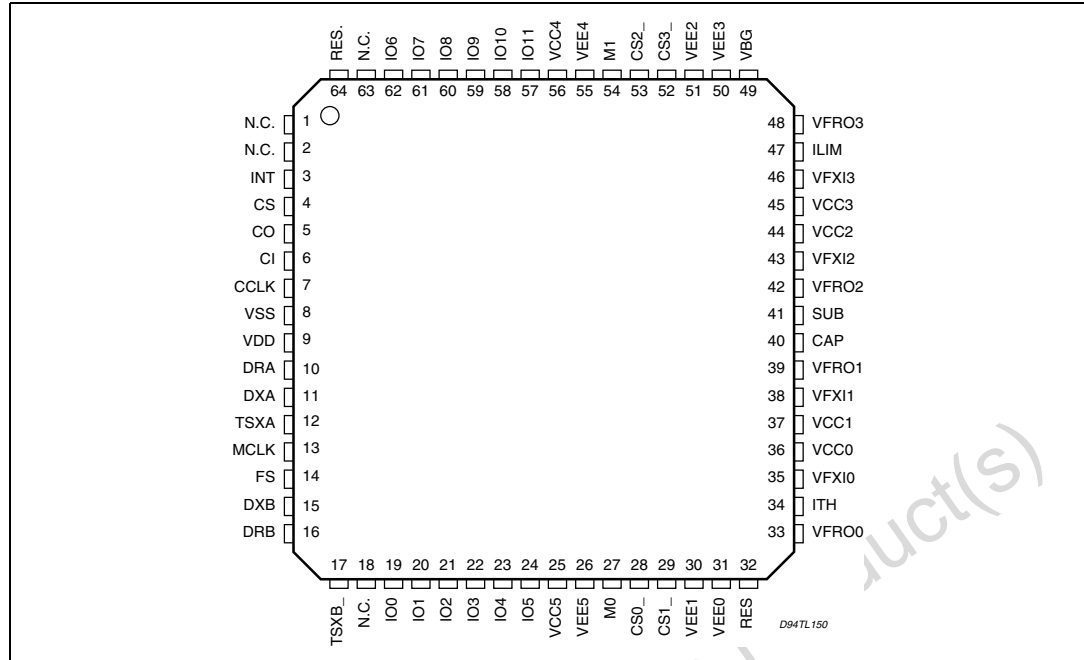
Table 4.   I/O definitions

Type	Definition
AI	Analog input
AO	Analog output
ODO	Open drain output
DI	Digital input
DO	Digital output
DIO	Digital input / output
DTO	Digital tristate output
DPS	Digital power supply
APS	Analog power supply

Table 5.   Pin descriptions

No.	Name	Type	Description
Analog pins			
33	VFRO0	AO	Receive analog amplifier output channel 0. PCM data received on the programmed time slot on DR input is decoded and appears at this output.
39	VFRO1	AO	Receive analog amplifier output channel 1. PCM data received on the programmed time slot on DR input is decoded and appears at this output.
42	VFRO2	AO	Receive analog amplifier output channel 2. PCM data received on the programmed time slot on DR input is decoded and appears at this output.
48	VFRO3	AO	Receive analog amplifier output channel 3. PCM data received on the programmed time slot on DR input is decoded and appears at this output.
35	VFXI0	AI	TX input amplifier channel 0. Typ 1MΩ input impedance
38	VFXI1	AI	TX input amplifier channel 1. Typ 1MΩ input impedance
43	VFXI2	AI	TX input amplifier channel 2. Typ 1MΩ input impedance
46	VFXI3	AI	TX input amplifier channel 3. Typ 1MΩ input impedance
40	CAP		AGND voltage filter pin: a 100 nF capacitor must be connected between ground and this pin.
34	ITH	AO	SLIC off-hook detection threshold.
47	ILIM	AO	SLIC line current limitation.
49	VBG	AI	SLIC VBG reference for DC characteristics programmability.
Power supply			
25,36, 37,44, 45,56	VCC0..5	APS	Total 6 pins: 3.3 V analog power supplies, should be shorted together, require 100 nF decoupling capacitor to VEE.
26,30, 31,50, 51,55	VEE0..5	APS	Total 6 pins: analog ground, should be shorted together.
9	VDD	DPS	Digital power supply 3.3 V, require 100 nF decoupling capacitor to VSS.
8	VSS	DPS	Digital ground.
41	SUB	DPS	Substrate connection. Must be shorted together with VEE and VSS pins.
Digital pins			
27 54	M0 M1	DI	Mode select: M1 M0 Mode select 0 0 Reset status 1 0 Normal operation 0 1 Not allowed 1 1 Not allowed
14	FS	DI	Frame sync. Pulse. A pulse or a square waveform with an 8 kHz repetition rate is applied to this pin to define the start of the receive and transmit frame. Effective start of the frame can be then shifted of up to 7 clock pulses independently in receive and transmit directions by proper programming of the PCMSH register.

Table 5.   Pin descriptions (continued)

No.	Name	Type	Description
13	MCLK	DI	Master clock input. Four possible frequencies can be used: 1.536/1.544 MHz; 2.048 MHz; 4.096 MHz; 8.192 MHz. The device automatically detect the frequency applied. This signal is also used as bit clock and it is used to shift data into and out of the DRA/B and DXA/B pins.
12	TSXA	ODO	Transmit time slot (open drain output, 3.2mA). Normally it is floating in high impedance state except when a time slot is active on the DXA output. In this case TSXA output pulls low to enable the backplane line driver.
11	DXA	DTO	Transmit PCM interface A. It remains in high impedance state except during the assigned time slots during which the PCM data byte is shifted out on the rising edge of MCLK.
10	DRA	DI	Receive PCM interface A. It remains inactive except during the assigned receive time slots during which the PCM data byte is shifted in on the falling edge of MCLK.
24	IO5	DIO	General control I/O pin #5. Can be programmed as input or output via DIR register. Depending on content of CONF register can be a static input/output or a dynamic input/output synchronized with the CSn output signals controlling the SLICs.
62	IO6	DIO	General control I/O pin #6. (see IO5 description).
61	IO7	DIO	General control I/O pin #7. (see IO5 description).
60	IO8	DIO	General control I/O pin #8. (see IO5 description).
59	IO9	DIO	General control I/O pin #9. (see IO5 description).
58	IO10	DIO	General control I/O pin #10. (see IO5 description).
57	IO11	DIO	General control I/O pin #11. (see IO5 description).
19	IO0	DIO	General control I/O pin #0. (see IO5 description).
20	IO1	DIO	General control I/O pin #1. (see IO5 description).
21	IO2	DIO	General control I/O pin #2. (see IO5 description).
22	IO3	DIO	General control I/O pin #3. (see IO5 description).
23	IO4	DIO	General control I/O pin #4. (see IO5 description).
28	CS0	DIO	SLIC CS control #0. Depending on CONF reg. content can be a CS output for SLIC #0 or a static I/O. When configured as CS output it is automatically generated by the CODEC with a repetition time of 31.25ms. In this mode also the IO0..11 are synchronized and carry proper data in and out synchronous with CS. When configured as static I/O, the direction is defined by CSDIR register content.
29	CS1	DIO	SLIC CS control #1, (see CS0 description).
53	CS2	DIO	SLIC CS control #2, (see CS0 description).
52	CS3	DIO	SLIC CS control #3, (see CS0 description).

Table 5.   Pin descriptions (continued)

No.	Name	Type	Description
4	CS	DI	Chip select input, when this pin is low control information can be written to or read from the device via the CI and CO pins.
7	CCLK	DI	Clock of serial control bus. this clock shifts serial control information into or out of CI or CO when CS input is low depending on the current instruction. CCLK may be asynchronous with the other system clocks.
6	CI	DI	Control data input of serial control bus. Control data is shifted in the device when CS is low and clocked by CCLK. Depending on the addressed register different numbers of consecutive bytes can be loaded.
5	CO	DI	Control data output of serial control bus. Control data is shifted out the device when CS is low and clocked by CCLK. Depending on the addressed register different numbers of consecutive bytes can be shifted out.
3	INT	ODO	Interrupt output (open drain), goes low when a data change has been detected in the I/O pins or another interrupt source is active. One mask register allows to mask any I/O pin. Interrupt is reset when the I/O register is read.
17	TSXB	ODO	Transmit time slot (open drain output, 3.2 mA). Normally it is floating in high impedance state except when a time slot is active on the DXB output. In this case TSXB output pulls low to enable the backplane line driver.
15	DXB	DTO	Transmit PCM interface B. It remains in high impedance state except during the assigned time slots during which the PCM data byte is shifted out on the rising edge of MCLK.
16	DRB	DI	Receive PCM interface B. It remains inactive except during the assigned receive time slots during which the PCM data byte is shifted in on the falling edge of MCLK.
Not connected			
2, 18, 63, 1	N.C.		Not connected, must be left open
32, 64	RES		Reserved pins, must be connected to ground

4 Functional description

The STLC5048 is a fully programmable device with embedded ROM and RAM. The ROM is used to contain the default state coefficients for the programmable filters, while the RAM is used to load the desired coefficient values.

4.1 Power on initialization

When power is first applied it is recommended to reset the device (M1=M0=0) in order to set all the internal registers to the reset value (see *Chapter 5: Register description*; this means also power down mode for all the four channels and SW reset bit (RES) set in the CONF register.

When the RES bit is set, the only instructions allowed are the one that disable this bit and the REACOM instruction: all other instructions are ignored. It is not possible to disable the RES bit and write the other bits of the CONF register with the same instruction.

Of course, RESET mode can be programmed also by writing the RES bit of the CONF register.

See *Appendix C: Power sequences* for the power up sequence.

During RESET condition all the I/On and CSn pins are set as inputs, DX is in high impedance and all VFROn are set to AGND. After the reset all registers are loaded with the reset value.

It means that the PCM interface and all the VFRO outputs are configured as described in the power down state, while no transmit or receive time slot are set.

Then, filters and gain blocks are configured with the coefficient defined in the default state.

4.2 Power down state

Each of the four channel may be put into power down mode by setting the appropriate bit in the CONF register. In this mode the eventual programmed DX channel is set in high impedance while the VFRO outputs are forced to AGND. When all the channels are set in power down mode the device enters the power down state: all the blocks related to the data processing are turned off, while the RAM is On or Off according to the PDR bit value in the COMEN register.

Figure 3.   Block diagram of a single channel
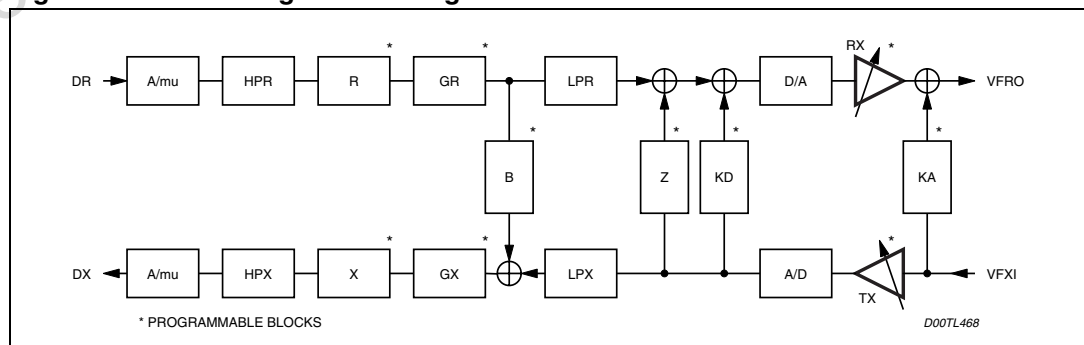
4.3 Ringing state

This state can be used during the ringing phase in order to transmit a low frequency ringing signal (25-50 Hz). In order to obtain a 1 Vrms ringing signal at VFRO output a digital signal DR equal to -0.78 dBm0 must be provided.

This state means B, Z, X, KD and KA blocks equal to open circuits and the R block configured in order to obtain the maximum gain at the frequency of 25-50 Hz. During the ringing state if the TX time slot is enabled the idle PCM code is forced to DX.

To switch to this state, a bit (FR0..3) in the COEFST register must be set for every channel.

The programmed values for the previous blocks become active only when the FR and FD bits are reset.

If both FR and FD bits of a channel are set, the selected coefficient will be those of the ringing state.

4.4 Impedance synthesis

The impedance synthesis is performed by fully digital filters (Z and KD) and by an analog path (KA).

The Z, KD and KA filters report to the receive path the feedback signal coming from the transmit path. The coefficients of the Z, KD and KA filters are programmed via the ZFC, KD and AFE_CFF commands respectively.

4.5 Echo canceling

The trans-hybrid balance is performed by the digital programmable filter B.

The B filter reports to the transmit path the signal coming from the receive path. The coefficient of the B filter are programmed via the BFC command.

Figure 4.   Transmit path
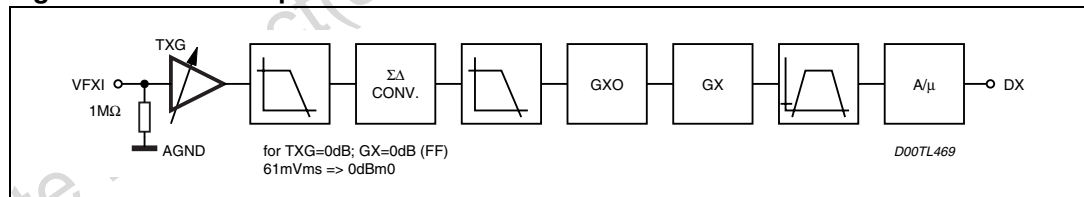
4.6 Transmit path

The transmit section input consist of the input amplifier, the A/D converter, the equalization filter X, the gain block GX, the encoder and the channel filters (LPX and HPX).

The input amplifier is provided of a programmable gain with a typical input impedance of 1MΩ The amplifier gain can be programmed with two different values (0 dB, +3.52dB) by means of the TXG register.

VFXI input must be AC coupled to the signal; the voltage swing allowed is 1.4 Vpp when the preamplifier gain is set to 0 dB and 0.93 Vpp when the gain is 3.52 dB; higher levels must be reduced through proper dividers.

Following the input amplifier the signal is converted into digital domain and a X filter block is programmed to equalize together with the HPX and LPX filters the frequency response. The coefficients of the X filter are programmed via the XFC command.

A gain block (GX) allows to set the transmit level in a 30 dB range, with steps <0.01 dB. This block can be programmed via the GTX command.

The needed TX gain can be set by proper programming of the GX block in combination with the TX amplifier.

Setting GTX=00h, the transmitted signal is muted and an idle PCM signal is generated on DX.

Concerning the CODING function, A/m law can be selected writing the CONF register (bit 5 AMU). In addition, via the CONF register (bit 6 LIN) the coding law can be set to linear mode (16 bits). In this case the signal sent on the DX will take two adjacent PCM channels, proper care has to be taken in the time slot selection programming (DXTS register).

The intrinsic non-programmable gain GX0 set the TX path gain to 22.07 dB. The absolute gain level (see *Chapter 9: Electrical characteristics*) refers to this intrinsic gain.

4.7   Receive path

The receive path of the STLC5048 consists of the decoder section, the gain block GR, the R filter, the channel filters (LPR, HPR) the D/A converter and the output amplifier.

Concerning the DECODING function, A/m law can be selected writing the CONF register (bit 5 AMU). In addition via the CONF register (bit 6 LIN) the coding law can be set to linear mode (16 bits).

In this case the signal received on the DR input will take two adjacent PCM channels, proper care has to be taken in the time slot selection programming (DRTS register).

The gain block GR is controlled by the GRX command allowing 30 dB gain range in 0.01 dB steps.

The R filter together the channel filters (LPR and HPR) performs the line equalization. The coefficients of the R filter are programmed via the RFC command.

The signal is converted in the analog domain and amplified by the RX amplifier that can be programmed with four different values (mute, 0 dB, -6 dB and -12 dB) by means of RXG register.

Figure 5.   Receive path
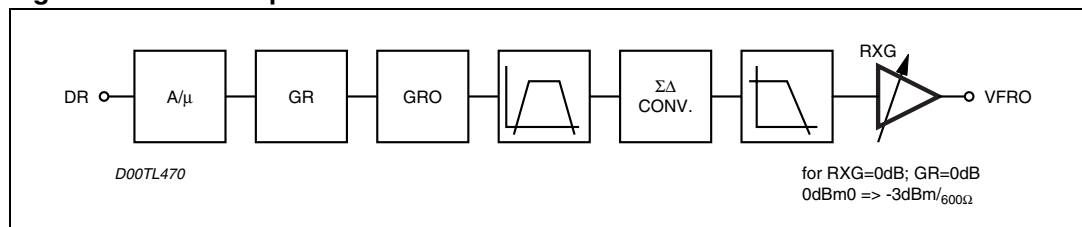
VFRO output, referred to AGND must be AC coupled to the load, referred to VSS, to prevent a DC current flow.

In order to get the best noise performances it is recommended to keep GRX value as close as possible to the maximum (FFh) setting properly the additional attenuation by means of RXG.

The intrinsic non programmable gain GR0 set the RX path gain to -3.15dB. The absolute gain level (see *Chapter 9: Electrical characteristics*) refers to this intrinsic gain.

4.8   PCM interface

The STLC5048 dedicates eight pins to the interface with the PCM highways.

MCLK represents the bit clock and is also used by the device as a source for the clock of the internal PLL.

Five possible frequencies can be used: 1.536/1.544 MHz (24-channel PCM frame); 2048 MHz (32-channel PCM frame); 4.096 MHz (64-channel PCM frame); 8.192 MHz (128 channels PCM frame). The operating frequency is automatically detected by the device the first time both MCLK and FS are applied and becomes active after the second FS period. MCLK synchronizes both the transmit data (DXA/B) and the receive data (DRA/B).

The Frame Synchronization signal FS is the common time base for all the four channels.

Transmit and receive programmable time-slots are framed by an internal synchronization signal that can be coincident with FS or delayed of 1 or 7 MCLK cycles depending on the programming of PCMSH register.

Two PCM ports are available: every channel can be connected to a different PCM port by means of PCMCOM register.

DXA/B represents the transmit PCM interface. It remains in high impedance state except during the assigned time slots during which the PCM data byte is shifted out on the rising/falling edge of MCLK according to the TE bit of PCMCOM register. The four channels can be shifted out in any possible time slot as defined by the DXTS registers. The assigned time slot (transmit and receive) takes place in the 8 MCLK cycles following the rising edge of FS.

The data can be shifted out on port A and/or B according to PCMCOM register.

If one codec is set in power down by software programming, the corresponding time slot is set in high impedance. When linear coding mode is selected by CONF register programming, the output channel will need two consecutive time slots (see *Chapter 5: Register description*).

DRA/B represents the receive PCM interface. It remains inactive except during the assigned time slots during which the PCM data byte is shifted in on the falling edge of MCLK. The four channels are shifted in any possible time slot as defined by the DRTS registers.

If one codec is set in power down by software programming, the corresponding time slot is not loaded and the VFRO output is kept at steady AGND level.

Table 6. **Instruction byte structure**

First byte (address or command ID)								Following bytes (data)							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
R/W	I6	I5	I4	I3	I2	I1	I0	D7	D6	D5	D4	D3	D2	D1	D0

R/$\overline{W}$=0: Write operation

R/$\overline{W}$=1: Read operation

I6..I0: Instruction identifier: it can be a register address or a command identifier.

The number of data bytes depends on the instruction type. The first bit of a byte is the MSB, the first byte of an instruction is the LSByte.

When linear coding mode is selected by CONF register programming the input channel will need two consecutive time slots (see *Chapter 5: Register description*).

The data can be shifted in from port A or B according to the PCMCOM register.

TSXA/B represents the transmit time slot (open drain output, 3.2 mA). Normally it is floating in high impedance state except when a time slot is active on the DXA/B output. In this case TSXA/B output pulls low to enable the backplane line driver. Should be strapped to VSS when not used.

Finally by means of the LOOPB register it is possible to implement a digital or analog loopback on any of the selected channels.

4.9 MCU control interface

The MCU serial control interface consists of the following four pins:

● CCLK: control clock
● CI: serial data in
● CO: serial data out
● CS: chip select input

Control instructions require at least two bytes: however two single byte instructions are also provided.

In the multiple byte instructions the first one specifies the command or the register address and the access type (read or write).

The following bytes contain the data to be loaded into the internal RAM (on CI wire) or carry out the RAM content (on CO wire) depending on the R/W bit of the first byte. CO wire is normally in high impedance and goes to low impedance only after the first byte in case of read operation. This allows to use a common wire for both CI/CO.

CS, normally high, is set low during the transmission/reception of a byte, lasting 8 CCLK pulses. Between two consecutive access, the CS must be set high.

The CCLK can be a continuous or a gated clock.

The result of any instruction (read/write operation), if negative, can generate an interrupt (maskable). The interrupt register (INT) contains the cause information of the generated interrupt and it is cleared every time that it is read.

Depending on the instruction specified in the first byte, the STLC5048 waits a defined number of data bytes. If the STLC5048 doesn't receive the data byte within a predefined

period specified by means of T_OUT command, an internal time out rejects the instruction. The time-out time is verified between two consecutive MCU interface access (between the falling edge of the CS and the following rising edge).

This feature is used to verify the synchronization of the MCU interface: however it can be disabled if not desired (see T_OUT register description). To check this synchronization is provided a specific register (SYNCK) that returns always a predefined value: if the returned value is different the MCU interface is in out of sync state (the device is waiting a data byte while the MCU is writing an address or vice versa). In this case, it is possible to realign it by means of the execution of a specific single byte instruction (REACOM) from 1 to 53 times, depending on the instructions.

Every time an illegal operation (access to not allowed address, time-out violation or clock pulse different than 8 inside a CS active) is performed the MCU interface is put on an error state: to resume it from this state a single REACOM instruction can be used.

Anyway after a REACOM instruction a successful SYNC instruction guarantees the correct synchronization.

One additional wire provided to the control interface is an open drain interrupt output (INT) that goes low when a change of status is detected on the I/O pins or other interrupt source are active (see *Section 5.7: Interrupt register (INT)*). INT is automatically reset after reading of the register corresponding the cause that has generated the interrupt (see INT register description).

A particular register (COMEN) allows to enable a command on different channel at the same time. Every time a command operation is performed at least one channel must be enabled in this register.

This feature is useful when all channels must be configured in the same condition. When a command is used to perform a read operation only one channel can be enabled at the same time.

To check the configuration of the device a checksum value is provided. This value is calculated on all coefficient parameters entered (coefficients of KD, AFE_CFF, GRX, GTX, RFC, XFC, BFC, ZFC blocks; see the CKSUM register description). Two commands are required to get this value: the first one (CKSTART) starts the internal checksum calculation, the second one (CKSUM) returns the calculated value. Between this two commands no other operation are allowed. The checksum value is available within 400us the CKSTART command.

Coefficient checksum is defined by the following algorithm: $X^{16} + X^{12} + X^5 + 1$

This algorithm guarantees a fault coverage of $1 - 2^{-16}$.

4.10 Programming the device

After the power up, the filters and gain blocks can be programmed also with all the channels set in power down. in this case the PDR bit of the COMEN register must be set to 0.

With the proper setting of the COMEN register, the commands can be applied to more than one channel at the same time.

To read the coefficient values loaded in the RAM, only one channel per time must be enabled in the COMEN register.

4.11 SLIC control interface

The device provides 12 I/O pins and 4 CS signals. The interface can work in dynamic or static mode. This can be selected by means of STA bit of the CONF register:

● Dynamic mode: the I/O pins are configured as input or output by means of DIR register. The CS signals are used to select the different SLIC interface. In this case the I/O pin can be multiplexed. The data loaded from SLIC #n via I/O pins configured as input can be read in the DATAn register. The data written in a DATAn register will be loaded on the I/O pins configured as output when the CSn signal will be active.

● Static mode: The CS signal can be used as I/O pins. They can be configured as input or output I/O by means of DATA1 register. The data corresponding to the CS signal can be read or written by means of DATA2 register. All data related to the other I/O pins can be read or written by means of DATA0 register.

4.12 DC SLIC programmability

Three additional pins are used to select the on-hook/off-hook detection threshold and the line card limitation of the STLC3080 SLIC. This two values are programmed by ILIM and ITH registers. The programming of these two registers must be done before the filter coefficients download.

The VBG input pin must be connected to the IREF pin of the STLC3080.

When the L3235N is used in kit with STLC5048 the ILIM, ITH and VBG pin must be not connected.

4.13 Built-in test

By means of TONEG register it is possible to inject a tone of variable frequency (25 Hz, 1 and 3 kHz) and 0 dBm0 amplitude into the receive path, replacing any signal coming from the PCM interface. This test can be performed on every channel.

Setting the proper bit of the PCMCOM register is also possible to read/write the PCM data coming from the transmit path via the MCU interface (PCMRD/PCMWD registers). This feature can be enabled only on one channel per time.

These two features can be used to test the line interface operation.

Table 7.   Register addresses

Addr	Name	Description
00h	DIR-L	I/O direction (bit 7-0)
01h	DIR-H	I/O direction (bit 11-8)
02h	DATA0-L	I/O data ch#0 (bit 7-0)
03h	DATA0-H	I/O data ch #0 (bit 11-8)
04h	DATA1-L	I/O data ch#1 (bit 7-0)
05h	DATA1-H	I/O data ch #1 (bit 11-8)
06h	DATA2-L	I/O data ch#2 (bit 7-0)
07h	DATA2-H	I/O data ch #2 (bit 11-8)

Table 7. **Register addresses (continued)**

Addr	Name	Description
08h	DATA3-L	I/O data ch#3 (bit 7-0)
09h	DATA3-H	I/O data ch #3 (bit 11-8)
0Ah	PCHK-A	Persistency check time for input A
0Bh	PCHK-B	Persistency check time for input B
10h	INT	Interrupt register
11h	DMASK-L	Int. mask I/O port (03h)
12h	DMASK-H	Int. mask I/O port (04h)
13h	IMASK	Interrupt mask reg.
14h	ALARM	Alarm register
20h	CONF	Configuration register
21h	COMEN	Command enable reg.
23h	SYNCCK	Synchronous check reg.
25h	CTRLACK	DSP status register
26h	CKSUM-L	Checksum register L
27h	CKSUM-H	Checksum register H
2Ah	LOOPB	Loopback register
2Bh	TXG	Transmit preamp. gain
2Ch	RXG	Receive preamp. gain
2Dh	ILIM	SLIC line current lim.
2Eh	ITH	SLIC off-hook threshold
50h	PCMSH	PCM shift register
51h	PCMCOM	PCMCOM register
52h	DXTS0	Transmit time slot ch #0
53h	DXTS1	Transmit time slot ch #1
54h	DXTS2	Transmit time slot ch #2
55h	DXTS3	Transmit time slot ch #3
56h	DRTS0	Receive time slot ch #0
57h	DRTS1	Receive time slot ch #1
58h	DRTS2	Receive time slot ch #2
59h	DRTS3	Receive time slot ch #3
5Ah	PCMWD-L	PCMW data register
5Bh	PCMWD-H	PCMW data register
5Ch	PCMRD-L	PCMR data register
5Dh	PCMRD-H	PCMR data register
5Eh	PCMCTRL	PCM control register

Table 7.   Register addresses (continued)

Addr	Name	Description
60h	TONEG	Tone generation reg.
61h	COEFST	Coefficient state reg.
70h	SWRID	Software rev. ID code
71h	HWRID	Silicon revision ID code

5 Register description

5.1 I/O direction register (DIR)

Addr=00h; reset value=00h
Addr=01h; reset value=X0h

Table 8. I/O direction register (DIR) bits

Blt7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	0	0	0
IO_7	IO_6	IO_5	IO_4	IO_3	IO_2	IO_1	IO_0

Table 9. I/O direction register (DIR) bits

Blt7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	0	0	1
				IO_{11}	$IO_{10}0$	IO_9	IO_8

$IO11..0=0$ I/O pin 11..0 is an input, data on the I/O input is written in DATAn register bit 11..0.
$IO11..0=1$ I/O pin 11..0 is an output, data contained in DATAn register bit 11..0 is transferred to the I/O output.

5.2 I/O data register channel #0 (DATA0)

Addr=02h; reset value=00h
Addr=03h; reset value=X0h
If bit 4 of CONF register (STA)=0 dynamic I/O mode:

Table 10. Dynamic I/O data register channel #0 (DATA0) bits

Blt7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	0	1	0
$D0_7$	$D0_6$	$D0_5$	$D0_4$	$D0_3$	$D0_2$	$D0_1$	$D0_0$

Table 11. Dynamic I/O data register channel #0 (DATA0) bits

Blt7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	0	1	1
				$D0_{11}$	$D0_{10}$	$D0_9$	$D0_8$

When CS0 is active D011..0 are transferred to the corresponding I/O pins configured as outputs (see DIR register). For the I/O pins configured as inputs the corresponding D011..0 will be written by the values applied to those pins while CS0 is low.

If bit 4 of CONF register (STA)=1 static I/O mode:

Table 12.   Static I/O data register channel #0 (DATA0) bits

BIt7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	0	1	0
DS_7	DS_6	DS_5	DS_4	DS_3	DS_2	DS_1	DS_0

Table 13.   Static I/O data register channel #0 (DATA0) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	0	1	1
				DS_{11}	DS_{10}	DS_9	DS_8

DS11..0 are transferred to the corresponding I/O pins configured as outputs (see DIR register). For the I/O pins configured as inputs the corresponding DS11..0 will be written by the values applied to those pins.

5.3   I/O data register channel #1 (DATA1)

Addr=04h; reset value=00h
Addr=05h; reset value=X0h

If bit 4 of CONF register (STA)=0 dynamic I/O mode:

Table 14.   Dynamic I/O data register channel #1 (DATA1) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	1	0	0
$D1_7$	$D1_6$	$D1_5$	$D1_4$	$D1_3$	$D1_2$	$D1_1$	$D1_0$

Table 15.   Dynamic I/O data register channel #1 (DATA1) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	1	0	1
				$D1_{11}$	$D1_{10}$	$D1_9$	$D1_8$

When $\overline{CS1}$ is active D111..0 are transferred to the corresponding I/O pins configured as outputs (see DIR register). For the I/O pins configured as inputs the corresponding D111..0 will be written by the values applied to those pins while $\overline{CS1}$ is low.

If bit 4 of CONF register (STA)=1 static I/O mode:

In static mode CS pins are used as additional I/O pins. The CIO0..3 bits are used to define the direction of these pins.

Table 16.   Static I/O data register channel #1 (DATA1) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	1	0	0
				CIO_3	CIO_2	CIO_1	CIO_0

CIO0..3=0 The $\overline{CS0..3}$ is a static input, DATA is written in DATA2 register bits 0..3.
CIO0..3=1 The $\overline{CS0..3}$ is a static output, DATA is taken from DATA2 register bits 0..3.

5.4 I/O data register channel #2 (DATA2)

Addr=06h; reset value=00h
Addr=07h; reset value=X0h

If bit 4 of CONF register (STA)=0 dynamic I/O mode:

Table 17. Dynamic I/O data register channel #2 (DATA2) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	1	1	0
$D2_7$	$D2_6$	$D2_5$	$D2_4$	$D2_3$	$D2_2$	$D2_1$	$D2_0$

Table 18. Dynamic I/O data register channel #2 (DATA2) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	1	1	1
				$D2_{11}$	$D2_{10}$	$D2_9$	$D2_8$

When $\overline{CS2}$ is active D211..0 are transferred to the corresponding I/O pins configured as outputs (see DIR register). For the I/O pins configured as inputs the corresponding D211..0 will be written by the values applied to those pins while $\overline{CS2}$ is low.

If bit 4 of CONF register (STA)=1 static I/O mode:

Table 19. Static I/O data register channel #2 (DATA2) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	0	1	1	0
				CD_3	CD_2	CD_1	CD_0

CD0..3 are transferred to the corresponding CS pin if configured as static output (see DATA1 register). For the CS pins configured as static inputs the corresponding CD0..3 will be written by the values applied to those pins.

5.5 I/O data register channel #3 (data3)

Addr=08h; reset value=00h
Addr=09h; reset value=X0h

Used only if bit 4 of CONF register (STA)=0; dynamic I/O mode:

Table 20. Dynamic I/O data register channel #3 (data3) bits

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	0	0	0	1	0	0	0
$D3_7$	$D3_6$	$D3_5$	$D3_4$	$D3_3$	$D3_2$	$D3_1$	$D3_0$