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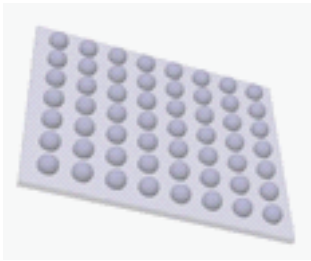
STLED524

Intelligent matrix LED display driver

Datasheet - preliminary data



CSP 56 bumps 0.4 mm pitch 3.4x3.0 mm

Features

- Operating input voltage range from 2.7 V to 5.5 V
- 5x24 LED matrix driver
- Adjustable luminance separately for each LED thanks to internal registers in 255 steps
- Internal registers store 2 patterns
- 4-way scroll function with the possibility to lock column data
- PWM dimming in 255 steps
- Adjustable blanking time
- Automatic slope function
- Cycle time and slope time adjustable for each dot separately
- SPI interface
- Integrated step-up converter with adjustable output voltage
- Integrated LDO with 3.1 V output @ 80 mA
- Boost efficiency 92% at 350 mA
- 2.4 MHz switching frequency
- CSP 56 bumps 0.4 mm pitch 3.4x3.0 mm

Applications

- Appliance user interfaces
- Display driver for handheld units

Description

The STLED524 is a 5x24 dot matrix LED display driver. It can drive each dot with a current up to 20 mA. Rows of the matrix are multiplexed. Each LED in a row is driven by a separate low-side current mirror. Current regulators are supplied by an integrated boost DC-DC converter. Its output voltage can be adjusted by the internal register to optimize efficiency according to the type of LEDs (their forward voltage). This reduces current mirror power dissipation and improves overall efficiency. The STLED524 also includes an internal LDO regulator, which can provide a supply voltage for an additional circuitry. Maximum current, provided by each current mirror, is adjusted by R_{SET} resistor. Current of each LED (dot) can be dimmed in 255 steps due to settings of internal registers.

The STLED524 features PWM dimming in 255 steps. Automatic slope function is also supported. Cycle time and slope time can be adjusted for each LED (dot) separately.

Two patterns can be stored in internal registers. The automatic scrolling of the display content is possible in 4 ways.

Table 1. Device summary

Order code	Package	Packaging
STLED524	CSP	Tape and reel

Contents

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1 Application schematic

Figure 1. Application schematic

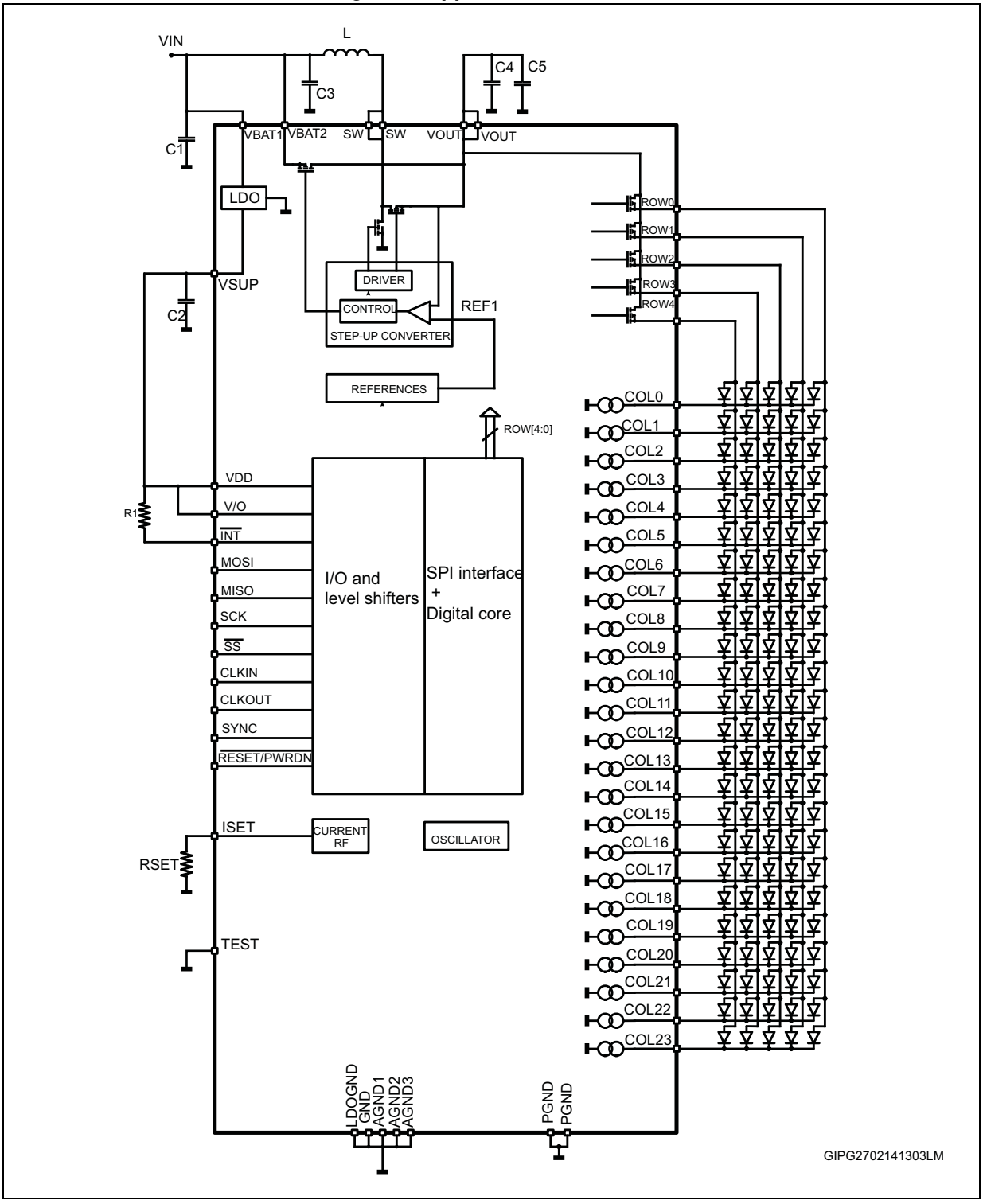


Table 2. Typical external components

Component	Manufacturer	Part number	Value	Size
C1	Murata	GRM188R60J106ME84D	10 µF	0603
C2	Murata	GRM188R60J106ME84D	10 µF	0603
C3	Murata	GRM188R60J106ME84D	10 µF	0603
C4	Murata	GRM21AR60J226ME47L	22 µF	0805
C5	Murata	GRM21AR60J226ME47L	22 µF	0805
L	Murata	LQM2HPN1R0MJC	1.0 µH	2.0x1.6x0.9 mm
R_{SET}			25 k	0402
R1			15 k	0402

Note: All above components refer to a typical application. The device operation is not limited to the choice of these external components.

Figure 2. Pin configuration (top view)

	1	2	3	4	5	6	7
A	GND	VDD	RESET	VSUP	VBAT1	PGND	PGND
B	CLKOUT	CLKIN	SCK	ISET	LDOGND	SW	SW
C	MISO	MOSI	INT	TEST	VBAT2	VOUT	VOUT
D	VIO	SYNC	SS	COL23	COL0	AGND1	ROW0
E	COL21	COL20	COL19	COL22	COL8	COL1	ROW1
F	COL18	COL17	COL15	COL9	COL3	COL2	ROW2
G	COL16	COL13	COL11	AGND2	COL6	COL4	ROW3
H	COL14	COL12	COL10	AGND2	COL7	COL5	ROW4

GIPG2702141312LM

Table 3. Pin description

Name	Pin	Description
VBAT1	A5	LDO supply voltage connection(1)
VBAT2	C5	Supply voltage connection(1)
SW	B6, B7	Coil connection
VOUT	C6, C7	Step-up converter output voltage
VSUP	A4	LDO output voltage
ROW 0-4	D7, E7, F7, G7, H7	Matrix row connections
COL 0-23	D4,D5 E1-E6, F1-F6, G1-G3, G5-G6, H1-H3, H5-H6	Matrix column connections
PGND	A6, A7	Power ground
AGND1	D6	Analog ground 1
AGND2	G4, H4	Analog ground 2
GND	A1	Ground
VDD	A2	Logic supply voltage
VIO	D1	I/O pin supply voltage
RESET/PWRDN	A3	Reset input, active low. When low, the device is in shutdown mode
MISO	C1	Master IN slave OUT (SPI bus)
MOSI	C2	Master OUT slave IN (SPI bus)
SS	D3	Slave select (SPI bus)
SCK	B3	SPU bus clock
CLKIN	B2	Clock input
CLKOUT	B1	Clock output
SYNC	D2	Synchronization input
INT	C3	Interrupt open drain output
LDOGND	B5	Boost output voltage setup resistor connection
ISET	B4	Reference current adjustment resistor connection
TEST	C4	Test input. It has to be connected to GND

1. Both VBAT1 and VBAT2 have to be supplied, even though LDO is not used to supply other devices.

2 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VBAT1, VBAT2	Supply voltage	-0.3 to +6	V
SW	Switching node	-0.3 to +6	V
VOUT	Output voltage	-0.3 to +6	V
VSUP	LDO output voltage	-0.3 to 3.6	V
VDD	Logic supply voltage	-0.3 to 3.6	V
VIO	I/O pin supply voltage	-0.3 to 3.6	V
ROW 0-4	Row switches	-0.3 to VOUT +0.3	V
COL 0-23	Column current mirrors	-0.3 to +6	V
MISO, MOSI, SCK, SS, INT, THA, CLKIN, CLKOUT, SYNC, RESET	Signal pins	-0.3 to +6	V
ISET	Current setting	-0.3 to 2	V
ESD	Machine model	±200	V
	Human body model	±2000	
	Charged device model	±250	
T_{AMB}	Operating ambient temperature	-30 to 85	°C
T_J	Maximum operating junction temperature	+125	°C
T_{STG}	Storage temperature	-40 to 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 5. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	62	°C/W

Note: This parameter corresponds to the PCB board, 8 layers with 1 inch^2 of cooling area.

3 Electrical characteristics

- 30 °C < T_A < 85 °C, V_{IN} = 2.7 V; V_{OUT} = 4.0 V; typical values are at T_A = 25 °C, unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
General section						
V_{IN}	Operating power input voltage range		2.7	3.7	5.5	V
V_{IO}	Supply voltage of I/O pins		1.8		3.6	V
V_{DD}	Digital supply voltage(1)			3.1		V
I_{SHDN}	Shutdown mode			2	10	µA
V_{UVLO}	Undervoltage lockout threshold (when reset is high)	V_{UVLOR} (V_{IN} rising)		2.5	2.6	V
		V_{UVLOF} (V_{IN} falling)	2.3	2.4		
Boost						
f_{SW}	Switching frequency		2.16	2.4	2.64	MHz
I_{OUT}	Continuous output current	V_{IN} = 3.5 V		480		mA
V_{OUT}	Boost output voltage	V_{IN} = 3.0 V	2.8		4.6	V
I_{PK}	Inductor peak current			1.5		A
η	Boost efficiency (V_{IN} = 3.7 V; V_{OUT} = 4.0 V)	I_{OUT} = 350 mA (PS mode)		92		%
V_{OVP}	Overvoltage protection			5.8	6	V
$V_{OVPHYST}$	Overvoltage protection hysteresis			200		mV
$V_{BSTOKHYST}$	Hysteresis of BST_OK comparator			250		mV
LDO						
V_{SUP}	LDO output voltage	V_{IN} = 3.3 V		3.1		V
ΔV_{SUP}	LDO output accuracy	V_{IN} = 3.3 V I_{OUT} = 1 mA		2	3	%
I_{LDO}	LDO output current	V_{IN} = 3.3 V		80	100	mA
I_Q	LDO quiescent current	V_{IN} = 3.3 V I_{OUT} = 80 mA		1.4		µA
Thermal protection						

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{SHDN1}	Thermal shutdown (boost and CM)			150		°C
$T_{SHDN1HYST}$	Hysteresis			20		
T_{SHDN2}	Thermal shutdown (LDO)			170		
$T_{SHDN2HYST}$	Hysteresis			20		
LED current						
$I_{LED0-LED23}$	Current matching	I_{COLx} = 20 mA, V_{OUT} > $V_{LED}+V_{CSH}$			5	%
ΔI_{LEDx}	Absolute channel accuracy	I_{COLx} = 20 mA, V_{OUT} > $V_{LED}+V_{CSH}$	-7.5		+7.5	%
V_{SET}	Voltage reference	R_{SET} = 25 k	1.225	1.25	1.275	V
	Current mirror ratio	I_{LED}/ I_{SET}		400		A/A
V_{CSH}	Current source headroom voltage (COLx to GND)		200			mV
I_{RIPPLE}	LED peak-to-peak current ripple(2)	V_{IN} = 3.0 V; I_{LED} = 20 mA in all channels	-15		+15	%
I_{LED_MAX}	Current mirror max. current	R_{SET} = 20 kΩ	22	25		mA
t_{SET}	LED current settling time (current reaches 90% of the target value)	I_{COLx} = 20 mA		1		µs
		I_{COLx} = 1 mA		10		
Logic inputs: MOSI, SCK, SS						
V_{IL}	Low-level input voltage	V_{IO} = 1.8 V to 3.6 V			0.3 V_{IO}	V
V_{IH}	High-level input voltage	V_{IO} = 1.8 V to 3.6 V	0.7 V_{IO}			V
I_{LK-H}	Input leakage current in high-level	V_{IO} = 3.6 V			2	µA
I_{LK-L}	Input leakage current in low-level	V_{IO} = 3.6 V			2	µA
Logic inputs: CLKIN, SYNK, RESET						
V_{IL}	Low-level input voltage	V_{IO} = 1.8 V to 3.6 V			0.3 V_{IO}	V
V_{IH}	High-level input voltage	V_{IO} = 1.8 V to 3.6 V	0.7 V_{IO}			V
I_{LK-H}	Input leakage current in high-level	V_{IO} = 3.6 V			2	µA
I_{LK-L}	Input leakage current in low-level	V_{IO} = 3.6 V			2	µA
Logic outputs						
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
V_{OH}	High-level output voltage	I_{OH} = 2 mA, V_{IO} = 3.0 V	V_{IO} -0.4			V
Clocks						
f_{OSC}	Internal oscillator frequency	V_{IN} = 2.7 V to 5.5 V	540	600	660	kHz

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
d_{CLKOUT}	Duty cycle of the clock out signal			60		
f_{EXT_MAX}	Maximum frequency of the external clock signal	V_{IN} = 2.7 V to 5.5 V			1.25	MHz
d_{CLKIN}	Duty cycle of the external clock signal	V_{IN} = 2.7 V to 5.5 V	30		70	%
$T_{INTTOEXTCLK}$	Transition time from internal to external clock		10			T_{CLKEX}
Power switches						
$R_{DS(on)}$	P-channel on-resistance (boost)			230		mΩ
	N-channel on-resistance (boost)			130		mΩ
$R_{DS(on)}$	P-channel on-resistance (ROW 0 to ROW 4)			500		mΩ
	N-channel on-resistance (ROW 0 to ROW 4)			200		mΩ
$R_{DS(on)}$	Bypass switch on-resistance					mΩ
I_{LKG-LX}	Coil leakage current	V_{IN} = V_{SW2} = 4.0 V			1	µA
Time and delay						
T_{CLK}	Clock period			1.667		µs
T_{RTCR}	Delay between row rising edge and column rising edge		1		8	T_{CLK}
T_{RTCF}	Delay between column falling edge and row falling edge		1		8	
T_{ONMIN}	PWM minimum on-time			2		
T_{ONMAX}	PWM maximum on-time			510		
T_{FRAME}	Frame period			2560		
T_{ROW}	Row duration			512		
Reset						
T_{RST}	Minimum pulse width on RESET pin		100			µs

1. It is strongly recommended to connect VDD pin to VSUP pin directly.
2. It is valid only if LED matrix is not farther than 10 cm from the driver, otherwise ceramic capacitors should be connected between COLx pin and ground to improve ripple.

4 Detailed description

The STLED524 is a 5x24 LED dot matrix display driver. It includes 24 low-side current mirrors (for each LED in a row). Rows are multiplexed by 5 internal PMOS transistors. Current mirrors are supplied by the integrated boost converter. Its output voltage is adjustable so it can be adapted to the forward voltage of LEDs. It reduces power dissipation and improves efficiency.

4.1 Boost converter

The step-up bridge with current mode control regulation provides output voltage according to the value of VOUT[3:0] register. This voltage should be adjusted to be high enough to provide sufficient headroom to regulate current sources connected to COL 0-23 pins. On the other hand, keeping boost output voltage unnecessarily high, increases power dissipation and degrades efficiency.

Boost incorporates a zero current comparator. When the input voltage is close to the output voltage, pulse-skipping is applied to keep the output voltage regulated.

If the input voltage is higher than desired output voltage, boost switches to bypass mode automatically. In this mode, the output voltage is equal to the input voltage lowered by voltage drop on the PMOS transistor.

Boost converter is enabled only when BSTEN bit in the boost control register is set to 1. VOUT setting shouldn't be changed when boost is on (BSTEN=1).

Table 7. Boost control register bits

Boost control	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 16h	BSTEN	-	-	-	VOUT3	VOUT2	VOUT1	VOUT0
Default	0	0	0	0	1	0	1	0

BSTEN = 0, boost is disabled

BSTEN = 1, boost is enabled

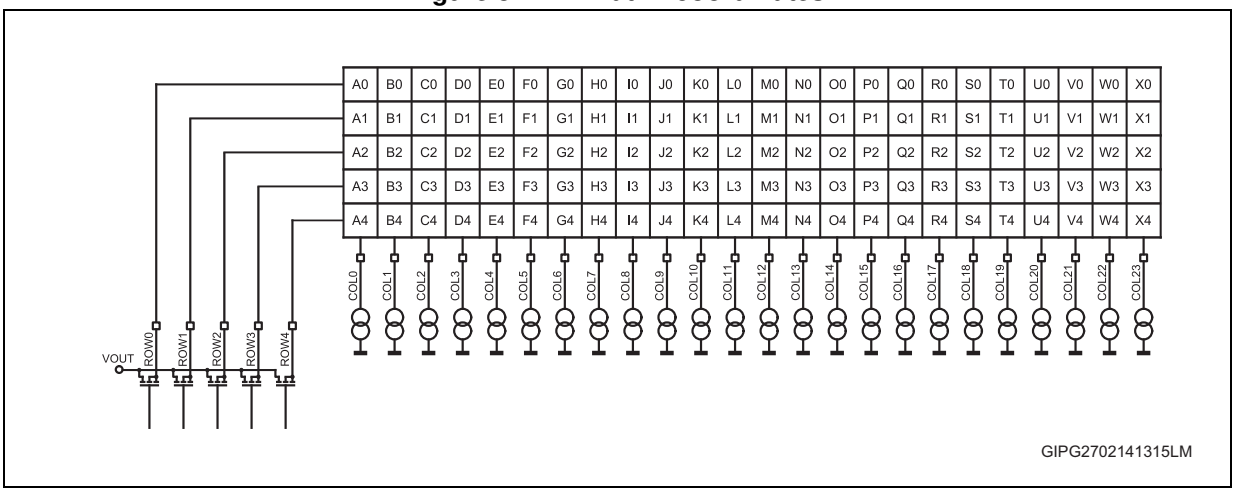
Table 8. Boost output voltage

VOUT[3:0]	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
V_{OUT}[V]	2.80	2.92	3.04	3.16	3.28	3.40	3.52	3.64	3.76	3.88	4.00	4.12	4.24	4.36	4.48	4.60

One step = 120 mV

4.2 LED matrix

Figure 3. LED matrix coordinates

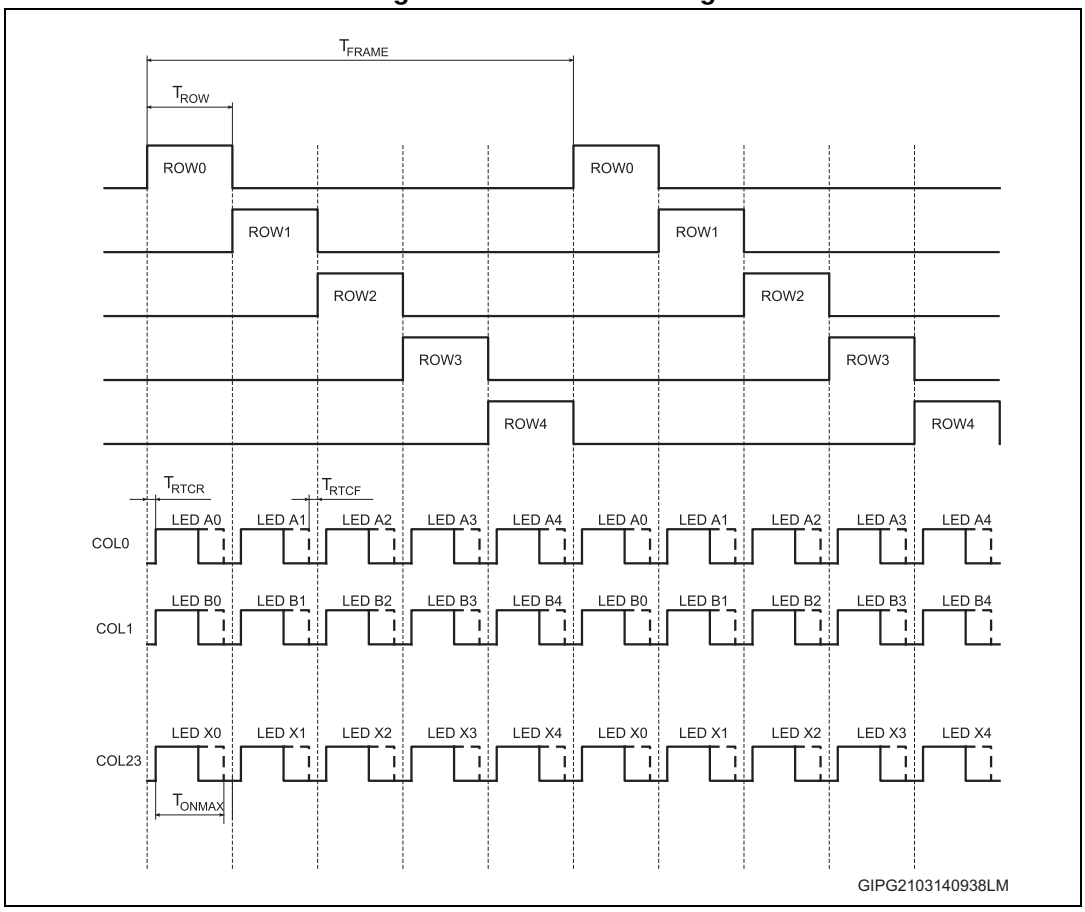


LED matrix rows are connected to ROW 0-4 pins. Columns are connected to COL 0-23 pins.

4.2.1 Blanking time

Rows are multiplexed by T_{ROW} period according to *Figure 4*. The duration of one row is given by $T_{ROW} = T_{FRAME} / 5$, but the maximum dot on-time is $T_{ONMAX} = T_{ROW} - (T_{RTCR} + T_{RTCF})$ only.

Figure 4. LED matrix timing



T_{RTCR} and T_{RTCF} are adjustable due to the blanking time register. If a blanking time is set longer than 2 T_{CLK}, maximum PWM duty cycle is limited according to *Table 10*.

Table 9. Blanking time register

Blanking time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 15h	-	-	-	-	-	BLK[2:0]		
Default	-	-	-	-	-	0	0	0

Table 10. Impact of blanking time on the maximum PWM duty cycle

Blanking time register value	Blanking time [T_{CLK}]	T_{RTCR} [T_{CLK}]	T_{RTCF} [T_{CLK}]	Max. PWM duty cycle
000	2	1	1	255/255
001	4	2	2	254/255
010	6	3	3	253/255
011	8	4	4	252/255
100	10	5	5	251/255
101	12	6	6	250/255
110	14	7	7	249/255
111	16	8	8	248/255

4.3 LED current setting

Although each current mirror can sink up to ~35 mA (that is more than test conditions), the following conditions have to be met:

- The sum of all current mirrors should not exceed 600 mA in bypass mode.
- The sum of all current mirrors should not exceed 480 mA in boost mode.
- If sum of all current mirrors exceeds test conditions, it may exceed the related specifications. The device is not guaranteed to sink current greater than test conditions.

Maximum current of all current mirrors can be adjusted by R_{SET} resistor value according to the following formula:

Equation 1

$$I_{LEDMAX} = \frac{V_{SET}}{R_{SET}} \times 400$$

where: V_{SET} = 1.25 V typically.

Current of each dot can be adjusted in its register, so each LED may have an independent setting of current.

Current can be adjusted in 255 steps; 1 step represents approximately 0.392% of I_{LEDMAX}. Current settings are carried out by Dn_xx registers, where n is the pattern number and xx are the coordinates of a dot in the matrix.

To avoid false activation of the short or open ISET pin protection, the minimum value of R_{SET} should be higher than 14 kΩ and lower than 270 kΩ.

4.4 Patterns

The STLED524 includes the memory for 2 patterns of 5x24 dots. Each dot in a pattern has 2 registers for its setting.

One 8-bit register stores dimming settings. The other one is 4-bit only and stores information about slope and delay.

Table 11. Dimming, slope and delay registers of one dot

Dimming	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = nnh	Dn_xx[7:0]							
Default value	Not defined							
Slope and delay (S&D)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = (nn+1)h	-	-	-	-	PnCYC*xx*[1:0]		PnDLY*xx*[1:0]	
Default value	-	-	-	-	Not defined		Not defined	

where:

n: is a number of pattern

xx: are coordinates of a dot in the matrix xx = {A0, A1, A2, A3, A4, B0, B1, …, B4, C0…, X0, X1, X2, X3, X4}.

Pattern 1 and pattern 2 memories are not initialized after the reset. They can contain random data. Their content should be reset by CLR1/CLR2 bits.

4.4.1 Pattern register organization

A pair of 8-bit registers is used to set properties of each dot in the matrix.

Table 12. Dimming, slope and delay registers of one dot (memory organization)

Address 0xnnh								Address 0x(nn+1)h							
Dimming register								Slope and delay register							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Dn_xx[7:0]								-	-	-	-	PnCYCxx[1:0]		PnDLYxx[1:0]	

Table 13. Register addresses in pattern 1

Address	Dimming register	Address	Slope and delay register	
00h	D1_A0[7:0]	01h	P1CYCA0[1:0]	P1DLYA0[1:0]
02hh	D1_A1[7:0]	03h	P1CYCA1[1:0]	P1DLYA1[1:0]
…	…	…	…	…
EEh	D1_X4[7:0]	EFh	P1CYCX4[1:0]	P1DLYX4[1:0]

Table 14. Register addresses in pattern 2

Address	Dimming register	Address	Slope and delay register	
00h	D2_A0[7:0]	01h	P2CYCA0[1:0]	P2DLYA0[1:0]
02h	D2_A1[7:0]	03h	P2CYCA1[1:0]	P2DLYA1[1:0]
…	…	…	…	…
EEh	D2_X4[7:0]	EFh	P2CYCX4[1:0]	P2DLYX4[1:0]

4.4.2 Display size

If DISPSIZE bit is set to 1, the content of columns 20-23 is always linked to pattern 1 regardless of the value of DISP bits. Columns 0-19 can still be used as a display, while columns 20-23 can be used for other functions.

If DISPSIZE bit is set to 1, the content of pattern 2 is also limited to columns 0-19 only. Columns 20-23 are not displayed during scrolling.

The minimum number of scroll steps in horizontal direction is reduced to 20, if DISPSIZE = 1.

Table 15. Content of columns 20-23

DISP	DISPSIZE	COL 0-19	COL 20-23
00	0	Blank	Blank
01	0	Pattern 1	Pattern 1
10	0	Pattern 2	Pattern 2
00	1	Blank	Pattern 1
01	1	Pattern 1	Pattern 1
10	1	Pattern 2	Pattern 1

4.5 Description of registers

4.5.1 Software control register

Table 16. Software control register

Software control	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 00h	SWRST	-	-	-	-	CLR2	CLR1	EN
Default	0	0	0	0	0	0	0	0

When CLR1 is set to 1, pattern 1 is cleared, (dimming, slope and delay of all dots are set to 0) then it is set to 0 automatically.

When CLR2 is set to 1, pattern 2 is cleared, (dimming, slope and delay of all dots are set to 0) then it is set to 0 automatically.

If SWRST bit is set to 1, content of all registers is set to default values and SWRST bit is cleared automatically.

If EN = 0, display is off

If EN = 1, display is on

4.5.2 Display control register

Table 17. Display control register

Display control	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 01h	-	-	-	-	-	-	DISP2	DISP1
Default	0	0	0	0	0	0	0	0

DISP1 and DISP2 bits define which pattern is displayed, see *Table 18*.

Table 18. DISP bits

DISP2	DISP1	Displayed pattern
0	0	No pattern is displayed (blank screen)
0	1	Pattern 1 is displayed
1	0	Pattern 2 is displayed
1	1	No pattern is displayed (blank screen)

DISP bits can be written by SPI anytime, but the display change (from pattern 1 to pattern 2 or vice versa) is performed according to the following rules:

- On next frame, if the display is on and scroll features are disabled (EN=1, SCRLEN=0).
- If SCRLEN=1 and EN=1, scroll operation starts according to the scroll setup.

4.5.3 Clock register

This register is used to set up clock signals.

Table 19. Clock register

Clock	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 10h	-	-	-	REFSEL	SYNCSEL	SYNCEN	CLKIN	CLKOUT
Default	0	0	0	0	1	0	0	0

CLKOUT = 0, CLKOUT pin does not provide any clock signal. It is permanently low

CLKOUT = 1, CLKOUT pin provides CLK signal

CLKIN = 0, clock signal from the internal oscillator is used for display timings

CLKIN = 1, clock signal from CLKIN pin is used for display timings

SYNCEN = 0, driver operation synchronization is disabled by an external signal connected to SYNC pin

SYNCEN = 1, driver operation synchronization is enabled by an external signal connected to SYNC pin

SYNCSEL = 0, driver operation is enabled when SYNC signal is low

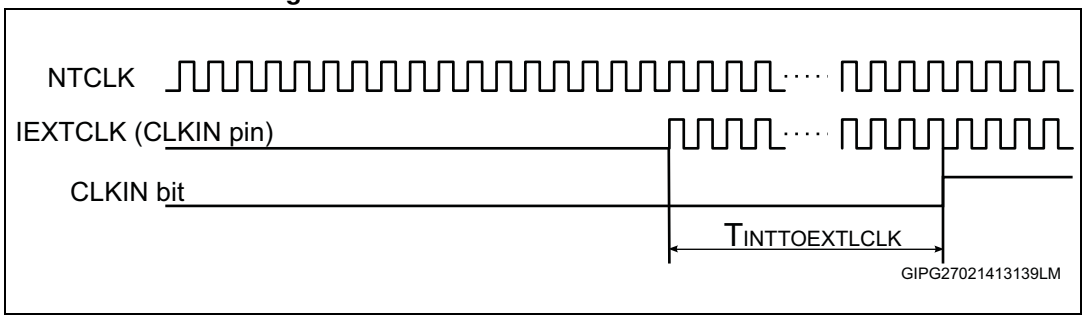
SYNCSEL = 1, driver operation is enabled when SYNC signal is high

REFSEL = 0, external reference defined by R_{SET} value is used for current mirrors

REFSEL = 1, internal reference is used for current mirrors

If the clock signal changes from internal to external, the external clock has to be provided, at least $T_{INTTOEXTCLK}$ before than CLKIN bit is set to 1.

Figure 5. Internal to external clock transition



SYNC pin behavior

If the synchronization is enabled (SYNCEN = 1), SYNC pin is in inactive state (defined by SYNCSEL bit) and the micro writes EN, DISP or SLPEN bits, but the corresponding operation is delayed, until SYNC pin gets to the active state.

If the synchronization is disabled (SYNCEN = 0), the micro writes EN, DISP or SLPEN bits, and the corresponding operation starts immediately.

Table 20. SYNC pin behavior

SYNCEN bit	SYNCSEL bit	SYNC pin	Operation
0	0	0	Not synchronized
0	0	1	Not synchronized
0	1	0	Not synchronized
0	1	1	Not synchronized
1	0	0	Synchronized, but the bit change has immediate effect
1	0	1	Synchronized, the operation is delayed, until SYNC pin is 0
1	1	0	Synchronized, the operation is delayed, until SYNC pin is 1
1	1	1	Synchronized, but bit change has immediate effect

4.5.4 Column control register

These registers are used to enable/disable columns of the matrix.

Table 21. Column control 1 register

Column control 1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 11h	COL7EN	COL6EN	COL5EN	COL4EN	COL3EN	COL2EN	COL1EN	COL0EN
Default	1	1	1	1	1	1	1	1

Table 22. Column control 2 register

Column control 2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 12h	COL15EN	COL14EN	COL13EN	COL12EN	COL11EN	COL10EN	COL9EN	COL8EN
Default	1	1	1	1	1	1	1	1

Table 23. Column control 3 register

Column control 3	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 13h	COL23EN	COL22EN	COL21EN	COL20EN	COL19EN	COL18EN	COL17EN	COL16EN
Default	1	1	1	1	1	1	1	1

COL<i>EN = 0, column <i> is disabled

COL<i>EN = 1, column <i> is enabled

These bits can be read or written in any configuration, but these registers should be changed when EN=0.

4.5.5 Row control register

This register is used to enable/disable rows of the matrix.

Table 24. Row control register

Row control	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 14h	-	-	-	ROW4EN	ROW3EN	ROW2EN	ROW1EN	ROW0EN
Default	0	0	0	1	1	1	1	1

ROW<i>EN = 0, row <i> is disabled

ROW<i>EN = 1, row <i> is enabled

These bits can be read or written in any configuration, but these registers should be registerd when EN=0.

4.5.6 Blanking time register

This register sets the blanking time duration.

Table 25. Blanking time duration

Blanking time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 16h	-	-	-	-	-	BLK[2:0]		
Default	0	0	0	0	0	0	0	0

BLK[2:0] - blanking time duration

000: 2 clock periods

001: 4 clock periods

010: 6 clock periods

011: 8 clock periods

100: 10 clock periods

101: 12 clock periods

110: 14 clock periods

111: 16 clock periods

These bits can be read or written in any configuration, these registers should be changed when EN=0. See *Section 4.2.1* for details.

4.5.7 Boost control register

This register is described in *Section 4.1*.

4.5.8 Display visual control register

This register enables/disables the driver visual features.

Table 26. Display visual control register

Display visual control	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 20h	-	-	BRCEN	WAITEN	SLPEN	SCRLEN	PWMEN	DISPSIZE
Default	0	0	0	0	0	0	0	0

PWMEN = 0, PWM duty cycle is fixed to maximum available

PWMEN = 1, PWM duty cycle can be customized by PWM control register

SCRLEN = 0, scrolling is disabled

SCRLEN = 1, scrolling is enabled

SLPEN = 0, slope operation is disabled

SLPEN = 1, slope operation is enabled

WAITEN = 0, wait time at the end of scroll operation is disabled

WAITEN = 1, wait time at the end of scroll operation is enabled

BRCEN = 0, insertion of blank rows/columns during scroll operation is disabled

BRCEN = 1, insertion of blank rows/columns during scroll operation is enabled

DISPSIZE = 0, full number of columns is used to display content of patterns 1 and 2

DISPSIZE = 1, content of columns 20-23 is always linked to pattern 1 regardless of the value of DISP bits. If content of pattern 2 is displayed, then columns 0-19 are visible. The rest is "hidden behind" in the columns 20-23 that display content of pattern 1 permanently.