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# RM0380
# Reference manual

## STLUX and STNRG digital controllers designed for lighting and power conversion

## Introduction

This reference manual provides complete information for application developers on how to use the STLUX and STNRG family of digital controllers.

The STLUX™ family of controllers is a part of the STMicroelectronics® digital devices tailored for lighting applications. The STLUX controllers have been successfully integrated in a wide range of architectures and applications, starting from simple buck converters for driving multiple LED strings, boost for power factor corrections, half-bridge resonant converters for high power dimmable LED strings and up to full bridge controllers for HID lamp ballasts. STLUX natively supports the DALI via the internal DALI communication module (DCM). DALI is a serial communication standard used in the lighting industry.

STNRG devices are a part of the STNRG family of STMicroelectronics digital devices designed for advanced power conversion applications. The STNRG improves the design of the STLUX™ family to support industrial power conversion applications such as PFC+LLC, interleaved LC DC-DC, interleaved PFC for smart power supplies as well as the full bridge for pilot line drivers for electric vehicles.

The heart of the STLUX (and consequently STNRG where not differently specified) is the SMED (“State Machine, Event Driven”) technology which allows the device to operate several independently configurable PWM clocks with an up to 1.3 ns resolution. An SMED is a powerful autonomous state machine which is programmed to react to both external and internal events and may evolve without any software intervention. The SMED even reaction time can be as low as 10 ns, giving the STLUX the ability of operating in time critical applications.

The SMEDs are configured and programmed via the STLUX internal low-power microcontroller (STM8). The STM8 controller extends the STLUX reliability and guarantees more than 15 years of both operating lifetime and memory data retention to the program and data memory after cycling. The STM8 device also provides powerful processing while maintaining the advantages of the CISC architecture, a 24-bit linear addressing mode, an 8-bit data bus and an optimized architecture for low power applications.

The STLUX controller 1.8 V core voltage is provided by an internal power supply DC regulator in order to simplify and reduce the application design and cost.

The STLUX device has an embedded low power, low voltage, single voltage Flash program memory designed for reliability. The same technology provides an embedded true RWW data EEPROM dedicated area and dedicated 128 byte data used for the IC configuration.

This manual describes how to program the SMED and the STM8 companion controller.

Refer to the product datasheets for ordering information, pin description, mechanical and electrical device characteristics, and for specific peripherals and implementation details.

# Contents

# List of tables

# List of figures

# 1 Reference documents

- For hardware information on the STLUX controller and product specific SMED configuration, please refer to the STLUX product datasheets for STLUX385A, STLUX383A, STLUX325A and STLUX285A.
- For hardware information of the STNRG controller and product specific SMED configuration, please refer to the STNRG product datasheets for STNRG388A, STNRG328A and STNRG288A.
- For information on programming, erasing and protection of the internal Flash memory please refer to the programming manual PM0051 - “How to program STM8S and STM8A Flash program memory and data EEPROM”.
- For information about the debug module and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core and assembler instruction please refer to the STM8 CPU programming manual (PM0044).
- For information on the development tools please refer to the UM1792.

# 2 Acronyms

The following is a list of acronyms used in this document:

**Table 1. Acronym descriptions**

| Acronym | Description |
|---|---|
| ACU | Analog comparator unit |
| ADC | Analog-to-digital converter |
| AWU | Auto-wakeup unit |
| BL | Bootloader - used to load the user program without the emulator |
| CKC | Clock control unit |
| CPU | Central processing unit |
| CSS | Clock security system |
| DAC | Digital-to-analog converter |
| DALI | Digital addressable lighting interface |
| ECC | Error Correction Code |
| FSM | Finite state machine |
| FW | Firmware loaded and running on the CPU |
| GPIO | General purpose input/output |
| HSE | High-speed external crystal - ceramic resonator |
| HSI | High-speed internal RC oscillator |

**Table 1. Acronym descriptions (continued)**

| Acronym | Description |
|---|---|
| $I^2C$ | Inter-integrated circuit interface |
| IAP | In-application programming |
| ICP | In-circuit programming |
| ITC | Interrupt controller |
| IWDG | Independent watchdog |
| LSI | Low-speed internal RC oscillator |
| MCU | Microprocessor central unit |
| MSC | Miscellaneous |
| PM | Power management |
| RFU | Reserved for future use |
| ROP | Read-out protection |
| RST | Reset control unit |
| RTC | Real-time clock |
| SMED | State machine, event driven |
| STMR | System timer |
| SW | Software is the firmware loaded and running on the CPU (synonymous of FW) |
| SWIM | Single wire interface module |
| UART | Universal asynchronous receiver transmitter |
| WWDG | Window watchdog |

# 3 Register model

*Table 2* shows an outline picture of the register abbreviations used in this document.

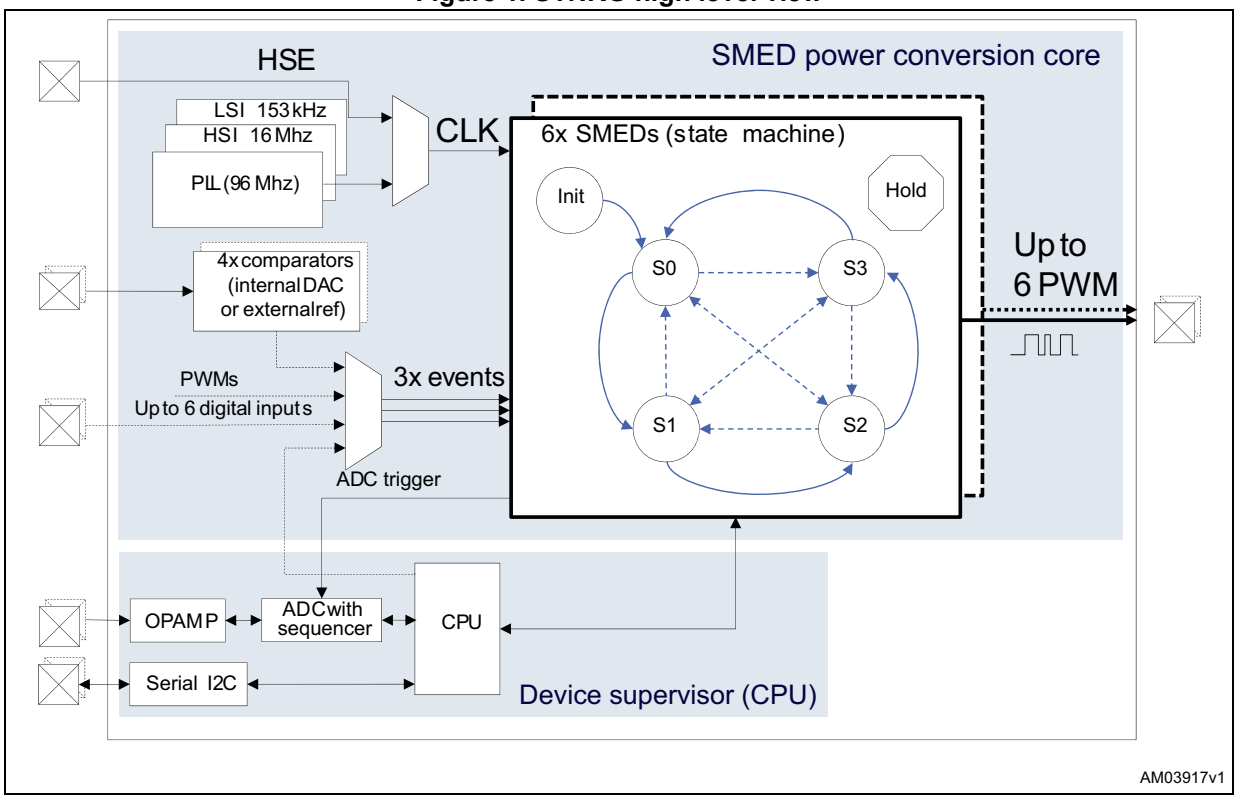
**Table 2. Register abbreviations**

| Abbreviation | Description |
|---|---|
| read/write (rw) or (r/w) | Software can read and write to these bits. |
| read only (r, ro) | Software can only read these bits. |
| write only (w, wo) | Software can only write to this bit. Reading the bit returns a meaningless value. |
| read/write clear (r/wc) | SW reads and writes clear. |
| read/write clear (r/w0) | SW reads and writes clear when writing-bit 0. |
| read/write clear (r/w1) | SW reads and writes clear when writing-bit 1. |
| read/write once (rwo) | Software can only write once to this bit and can also read it at any time. Only a reset can return the bit to its reset value. |
| read/clear (rc/w1) | Software can read as well as clear this bit by writing 1. Writing ‘0’ has no effect on the bit value. |
| read/clear (rc/w0) | Software can read as well as clear this bit by writing 0. Writing ‘1’ has no effect on the bit value. |
| read/set (rs) | Software can read as well as set this bit. Writing ‘0’ has no effect on the bit value. |
| read/write0 (r/w0) | Software can read and writing '0'. Writing '1' has to be avoiding for future product compatibility. |

# 4 Description

The STLUX and STNRG device families generate and control PWM signals by means of a state machine, called SMED (state machine event driven). *Figure 1* gives an overview of the internal architecture.

**Figure 1. STNRG high level view**




The core of the device is the SMED unit: a hardware state machine driven by system events. The SMED includes 4 states (S0, S1, S2 and S3) available during running operations. A special HOLD state is provided as well.

The SMED allows the user to configure, for every state, which system events will trigger a transaction to a new state.

During a transaction from one state to the other, the PWM output signal level can be updated.

Once a SMED is configured and running, it becomes an autonomous unit, so no interaction is required since the SMED automatically reacts to system events.

Thanks to the SMED's 96 MHz operating frequency and their automatic dithering function, the PWM maximum resolution is 1.3 ns.

The device has 6 SMEDs available. Multiple SMEDs can operate independently from each other or they can be grouped together to form a more powerful state machine.

## 4.1 STLUX/STNRG feature comparison

The following table summarizes the differences between the STLUX and STNRG family of products

**Table 3. STLUX/STNRG feature comparison**

| Feature | | Device | |
|---|---|---|---|
| | | STLUX | STNRG |
| Max. pin count | | 38 | |
| SMED available | | 6 | |
| Max. SMED PWM output pins | | 6 | |
| Max. fast digital inputs pins | | 6 | |
| Max. positive comparator input pin | | 4 | |
| Max. negative comparator input pins | | 1 | 3 |
| Comparator hysteresis | | No | Yes |
| Internal DACs | | 4 | |
| Max. ADC input pins | | 8 | |
| Max. ADC gain | | x1 – x4 | |
| ADC hardware trigger | | No | Yes |
| Max. GPIO port 0 pins | | 6 | |
| Communication | UART peripheral | Yes | |
| | DALI peripheral | Yes | No |
| | I2C peripheral | Yes | |
| HSE function | | Yes | |
| Timers | System timer | 1 | |
| | Auxiliary timer | 1 | |
| | Basic timer | No | 2 |
| Auto-wakeup timer | | 1 | |
| Watchdog | Window watchdog timer | 1 | |
| | Independent watchdog timer | 1 | |
| Flash program memory | | 32 Kb | |
| EEPROM data memory | | 1 Kb | |
| RAM | | 2 Kb | 6 Kb |