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STM1403

3 V FIPS-140 security supervisor with battery switchover

Features

- STM1403 supports FIPS-140 security level 3+
  - Four high-impedance physical tamper inputs
  - Over/under operating voltage detector
  - Security alarm ($\overline{SAL}$) on tamper detection
- Supervisory functions
  - Automatic battery switchover
  - $\overline{RST}$ output (open drain)
  - Manual (push-button) reset input ($\overline{MR}$)
  - Power-fail comparator (PFI/$\overline{PFO}$)
- $\overline{Vccsw}$ (V_{CC} switch output)
  - Low when switched to V_{CC}
  - High when switched to V_{BAT} (BATT ON indicator)
- Battery low voltage detector (power-up)
- Optional V_{REF} (1.237 V)
  - (Available for STM1403A only)
- Low battery supply current (2.8 µA, typ)
- Secure low profile 16-pin, 3 x 3 mm, QFN package

QFN16, 3 mm x 3 mm (Q)

Table 1. Device summary

Device	Standard supervisory functions(1)	Physical tamper inputs	Over/under voltage alarms	V_{REF} (1.237 V) option	V_{OUT} status, during alarm	$\overline{Vccsw}$ status, during alarm
STM1403A	✔	✔	✔	✔	ON	Normal mode(2)
STM1403B(3)	✔	✔	✔	Note(4)	High-Z	High
STM1403C	✔	✔	✔	Note(4)	Ground	High

1. Reset output, power-fail comparator, battery low detection ($\overline{SAL}$, $\overline{RST}$, $\overline{PFO}$, and $\overline{BLD}$ are open drain).
2. Normal mode: low when V_{OUT} is internally switched to V_{CC} and high when V_{OUT} is internally switched to battery.
3. Contact local ST sales office for availability.
4. Pin 9 is the V_{REF} pin for STM1403A. It is the V_{TPU} pin for STM1403B/C.

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1 Description

The STM1403 family of security supervisors are a low-power family of intrusion (tamper) detection chips targeted at manufacturers of POS terminals and other systems, to enable them to meet **physical and/or environmental** intrusion monitoring requirements as mandated by various standards, such as Federal Information Processing Standards (FIPS) Pub 140 entitled “Security Requirements for Cryptographic Modules,” published by the National Institute of Standards and Technology, U.S. Department of Commerce), EMVCo, ISO, ZKA, and VISA PED. STM1403 supports target levels 3 and lower.

The STM1403 includes automatic battery switchover, $\overline{RST}$ output (open drain), manual (push-button) reset input ($\overline{MR}$), power-fail comparator (PFI/$\overline{PFO}$), physical and/or environmental tamper detect/security alarm, and battery low voltage detect features.

The STM1403A also offers a V_{REF} (1.237 V) as an option on pin 9. On the STM1403B/C, this pin is V_{TPU} (internally switched V_{CC} or V_{BAT}).

1.1 V_{OUT} pin modes

The STM1403 is available in three versions, corresponding to three modes of the V_{OUT} pin (supply voltage out), when the $\overline{SAL}$ (security alarm) is asserted (active-low) upon tamper detection:

1.1.1 STM1403A

V_{OUT} stays ON (at V_{CC} or V_{BAT}) when $\overline{SAL}$ is driven low (activated).

1.1.2 STM1403B

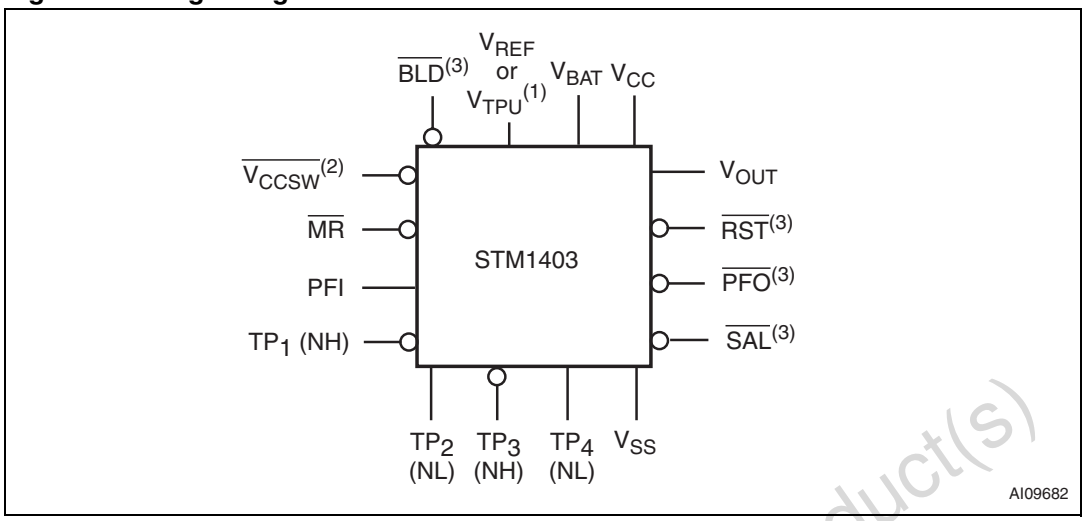
V_{OUT} is set to High-Z when $\overline{SAL}$ is driven low (activated).

1.1.3 STM1403C

V_{OUT} is driven to ground when $\overline{SAL}$ is activated (may be used when V_{OUT} is connected directly to the V_{CC} pin of the external SRAM that holds the cryptographic codes).

All variants (see *Table 1: Device summary*) are pin-compatible and available in a security-friendly, low profile, 16-pin QFN package.

Figure 1. Logic diagram



1. V_{REF} only for STM1403A; V_{TPU} for STM1403B/C.
2. Normal mode: low when V_{OUT} is internally switched to V_{CC} and high when V_{OUT} is internally switched to battery.
3. $\overline{SAL}$, $\overline{RST}$, $\overline{PFO}$, and $\overline{BLD}$ are open drain.

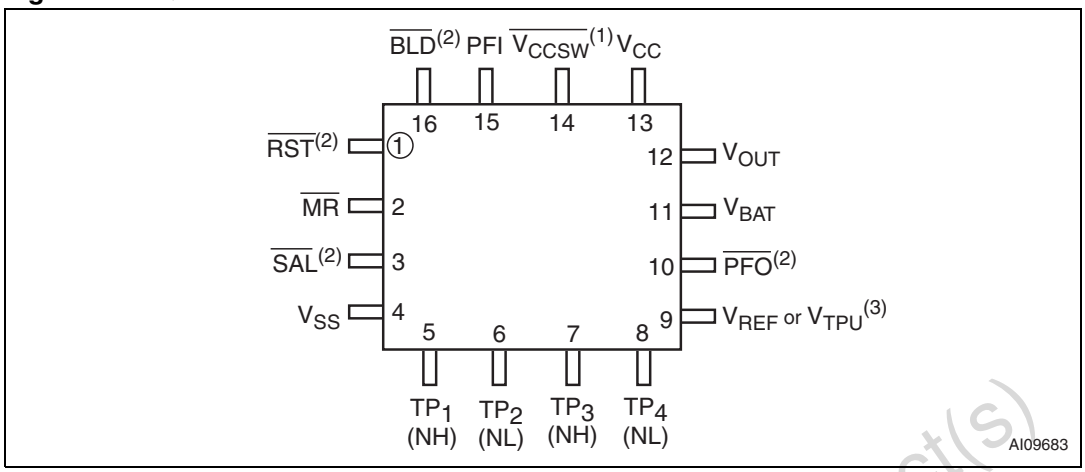
Table 2. Signal names

$\overline{Vccsw}$(1)	V_{CC} switch output
$\overline{MR}$	Manual (push-button) reset input
PFI	Power-fail Input
TP_1 - TP_4	Independent physical tamper detect pins 1 through 4
V_{OUT}	Supply voltage output
$\overline{RST}$(2)	Active-low reset output
$\overline{PFO}$(2)	Power-fail output
$\overline{SAL}$(2)	Security alarm output
$\overline{BLD}$(2)	Battery low voltage detect
V_{REF}(3)	1.237 V reference voltage
V_{TPU}(3)	Tamper pull-up (V_{CC} or V_{BAT})
V_{BAT}	Backup supply voltage
V_{CC}	Supply voltage
V_{SS}	Ground

1. Normal mode: low when V_{OUT} is internally switched to V_{CC} and high when V_{OUT} is internally switched to battery.
2. $\overline{SAL}$, $\overline{RST}$, $\overline{PFO}$, and $\overline{BLD}$ are open drain.
3. V_{REF} only for STM1403A; V_{TPU} for STM1403B/C.

Note: See Section 2: Pin descriptions on page 11 for details.

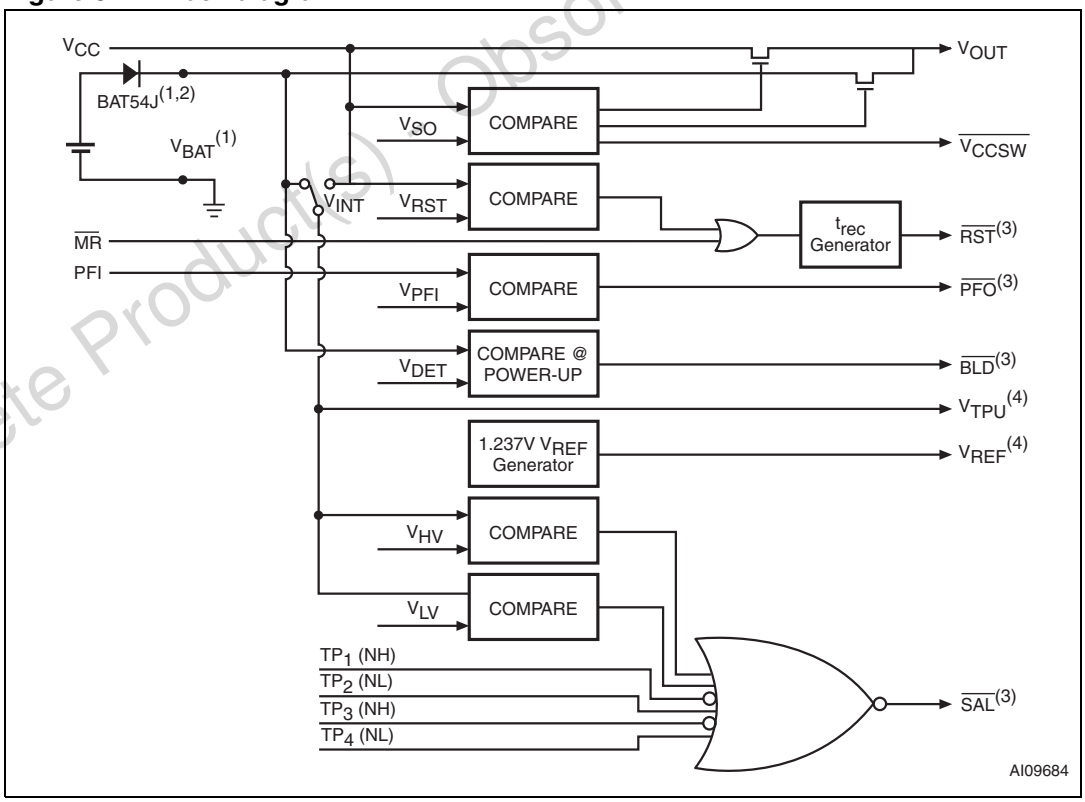
Figure 2. QFN16 connections



Note: See Section 2: Pin descriptions on page 11 for details.

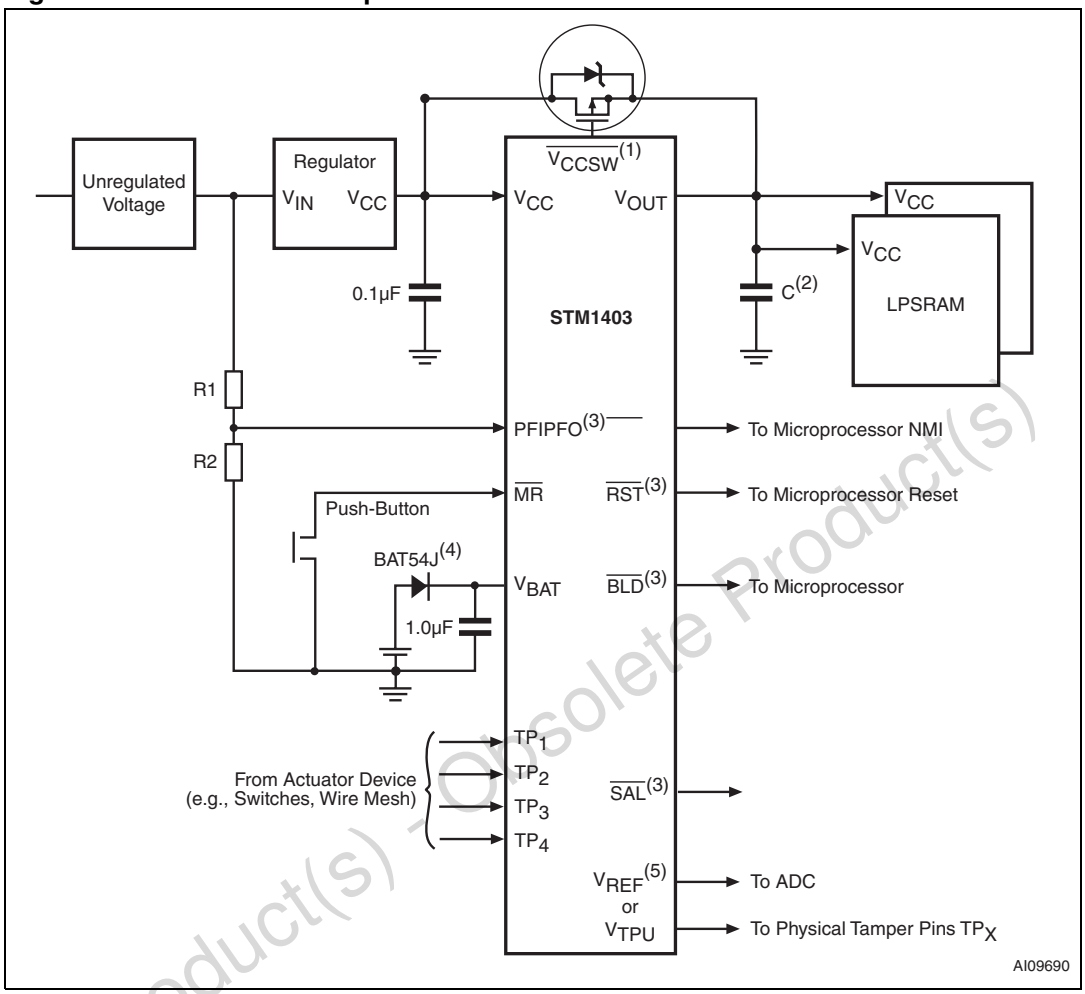
1. Normal mode: low when V_{OUT} is internally switched to V_{CC} and high when V_{OUT} is internally switched to battery.
2. $\overline{SAL}$, $\overline{RST}$, $\overline{PFO}$, and $\overline{BLD}$ are open drain.
3. V_{REF} only for STM1403A; V_{TPU} for STM1403B/C

Figure 3. Block diagram



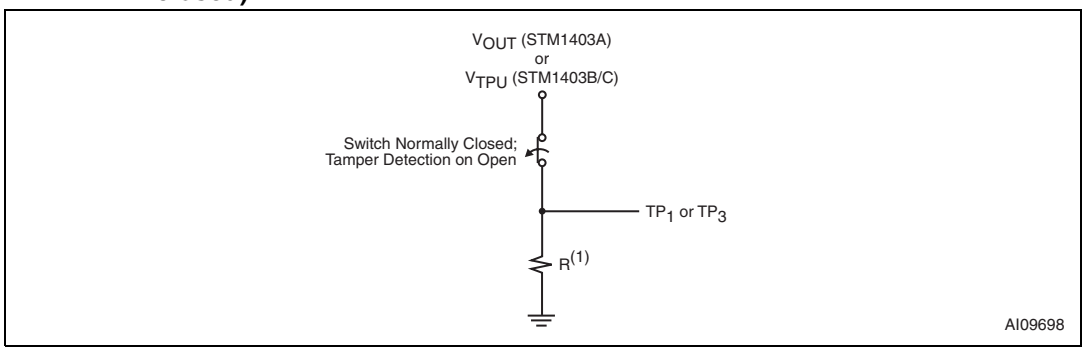
1. BAT54J (from STMicroelectronics) recommended
2. Required for battery-reverse charging protection
3. Open drain
4. V_{REF} only for STM1403; V_{TPU} for STM1403B/C

Figure 4. Hardware hookup



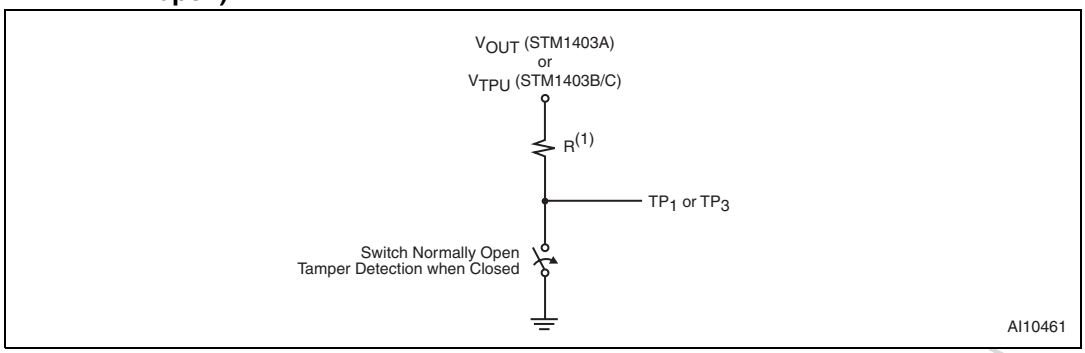
1. Normal mode: low when V_{OUT} is internally switched to V_{CC} and high when V_{OUT} is internally switched to battery.
2. Capacitor (C) is typically ≥ 10 µF.
3. Open drain
4. Diode is required for battery reverse charge protection.
5. V_{REF} only for STM1403; V_{TPU} for STM1403B/C.

Figure 5. Tamper pin (TP_1 or TP_3) normally high (NH) external hookup (switch closed)



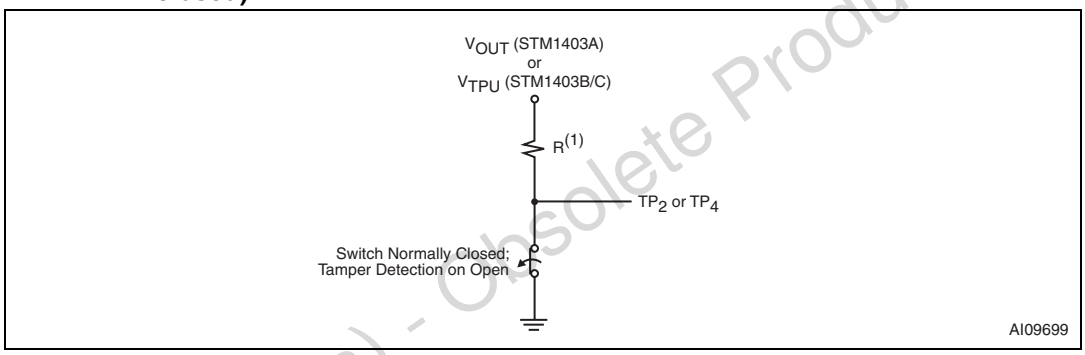
1. R typical is 10 MΩ. Resistors must be protected against conductive materials.

Figure 6. Tamper pin (TP_1 or TP_3) normally high (NH) external hookup (switch open)



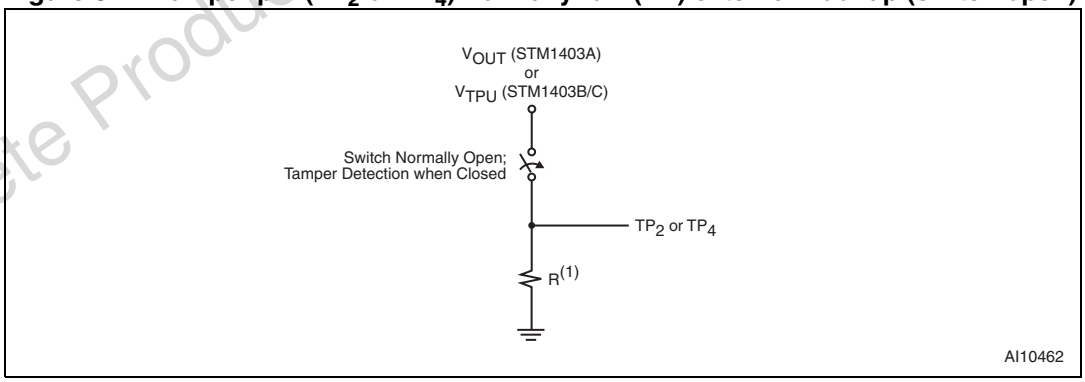
1. R typical is 10MΩ. Resistors must be protected against conductive materials.

Figure 7. Tamper pin (TP_2 or TP_4) normally low (NL) external hookup (switch closed)



1. R typical is 10 MΩ. Resistors must be protected against conductive materials.

Figure 8. Tamper pin (TP_2 or TP_4) normally low (NL) external hookup (switch open)



1. R typical is 10 MΩ. Resistors must be protected against conductive materials.

2 Pin descriptions

See *Figure 1: Logic diagram* and *Table 2: Signal names* for a brief overview of the signals connected to this device.

2.1 $\overline{SAL}$, security alarm output (open drain)

This signal can be generated when ANY of the following conditions occur:

- $V_{INT} > V_{HV}$, where V_{HV} = upper voltage trip limit (4.2 V typ); and where $V_{INT} = V_{CC}$ or V_{BAT};
- $V_{INT} < V_{LV}$, where V_{LV} = lower voltage trip limit (2.0 V typ); and where $V_{INT} = V_{CC}$ or V_{BAT}; or
- When any of the physical tamper inputs, TP_1 to TP_4, change from their normal states to the opposite (i.e., intrusion of a physical enclosure).

Note: 1 The default state of the $\overline{SAL}$ output during initial power-up is undetermined.

2 The alarm function will operate either with V_{CC} on or when the part is internally switched from V_{CC} to V_{BAT}.

2.1.1 TP_1, TP_3

Physical tamper detect pin set normally to high (NH). They are connected externally through a closed switch or a high-impedance resistor to V_{OUT} (in the case of STM1403A) or V_{TPU} (in the case of STM1403B/C. A tamper condition will be detected when the input pin is pulled low (see *Figure 5* and *Figure 6*). If not used, tie the pin to V_{OUT} (for STM1403A) or V_{TPU} (for STM1403B/C).

2.1.2 TP_2, TP_4

Physical tamper detect pin set normally to low (NL). They are connected externally through a high-impedance resistor or a closed switch to V_{SS}. A tamper condition will be detected when the input pin is pulled high (see *Figure 7* and *Figure 8*). If not used, tie the pin to V_{SS}.

2.1.3 $\overline{Vccsw}$, V_{CC} switch output

This output is low when V_{OUT} (see *Section 2.1.10: V_{OUT} on page 13*) is internally switched to V_{CC}; in this mode it may be used to turn on an external p-channel MOSFET switch which can source an external device directly from V_{CC} for currents greater than 80 mA (bypassing the STM1403).

This pin goes high when V_{OUT} is internally switched to V_{BAT} and may be used as a “BATT ON” indicator.

If a security alarm ($\overline{SAL}$) is issued on tamper, then the state of the $\overline{Vccsw}$ pin is as follows:

1. STM1403A (V_{OUT} remains ON when $\overline{SAL}$ is active-low): $\overline{Vccsw}$ pin will continue to operate in normal mode;
2. STM1403B (V_{OUT} is taken to High-Z when $\overline{SAL}$ is active-low): $\overline{Vccsw}$ pin will be set to high when this occurs; and
3. STM1403C (V_{OUT} is driven to ground when $\overline{SAL}$ is active-low): $\overline{Vccsw}$ pin will be set to high when this occurs.

2.1.4 $\overline{BLD}$, V_{BAT} low voltage detect output (open drain)

This is an internally loaded test of the battery, activated only during a power-up sequence to insure that the battery is good either prior to or after encapsulation of the module. There are three customer options for V_{DET}:

- 2.3 V (2.5 V – external diode drop of about 0.2 V) for a 3 V lithium cell
- 2.5 V (2.7 V – 0.2 V) for a 3 V lithium cell or
- 3.2 V (3.4 V – 0.2 V) for a 3.68 V lithium “AA” battery

This output pin will go active-low when it detects a voltage on the V_{BAT} pin below V_{DET}. $\overline{BLD}$ will be released when V_{CC} drops below V_{RST}.

2.1.5 Active-low $\overline{RST}$ output (open drain)

Goes low and stays low when V_{CC} drops below V_{RST} (reset threshold selected by the customer), or when $\overline{MR}$ is logic low. It remains low for t_{rec} (200ms, typical) AFTER V_{CC} rises above V_{RST} and $\overline{MR}$ goes from low to high.

2.1.6 $\overline{MR}$, manual reset input

A logic low on $\overline{MR}$ asserts the $\overline{RST}$ output. The $\overline{RST}$ output remains asserted as long as $\overline{MR}$ is low and for t_{rec} after $\overline{MR}$ returns to high. This active low input has an internal 40 kΩ (typical) pull-up resistor. It can be driven from a TTL or CMOS logic line or shorted to ground with a switch. Leave it open if unused.

2.1.7 $\overline{PFO}$, power-fail output (open drain)

When PFI is less than V_{PFI} (power-fail input threshold voltage) or V_{CC} falls below V_{SW} (battery switchover threshold ~ 2.4 V), $\overline{PFO}$ goes low, otherwise, $\overline{PFO}$ remains high. Leave this pin open if unused.

2.1.8 PFI, power-fail input

When PFI is less than V_{PFI}, or when V_{CC} falls below V_{SW} (see $\overline{PFO}$, above), $\overline{PFO}$ goes active-low. If this function is unused, connect this pin to V_{SS}.

2.1.9 V_{REF}, reference voltage output (1.237, typ)

This is valid only when V_{CC} is between 2.4 V and 3.6 V. When V_{CC} falls below 2.4 V (V_{SW}), V_{REF} is pulled to ground with an internal 100 kΩ resistor. This is an optional feature available on the STM1403A. On the STM1403B/C, this pin is V_{TPU} (internally switched V_{CC} or V_{BAT}). If unused, this pin should float.

2.1.10 V_{OUT}

This is the supply voltage output. When V_{CC} rises above V_{SO} (battery backup switchover voltage), V_{OUT} is supplied from V_{CC}. In this condition, V_{OUT} may be connected externally to V_{CC} through a p-channel MOSFET switch. When V_{CC} falls below the lower value of V_{SW} (~2.4 V), or V_{BAT}, V_{OUT} is supplied from V_{BAT}. It is recommended that the V_{OUT} pin be connected externally to a capacitor that will retain a charge for a period of time, in case an intruder forces V_{CC} or V_{BAT} to ground. The rectifying diode connected from the positive terminal of the battery to the V_{BAT} pin of the STM1403 will prevent discharge of the capacitor.

Three variations of parts will be offered with the following options:

1. STM1403A: V_{OUT} remains ON when $\overline{SAL}$ is active-low; $\overline{Vccsw}$ pin will continue to operate in normal mode (see *Section 2.1.3: Vccsw, V_{CC} switch output on page 11*);
2. STM1403B: V_{OUT} is taken to High-Z when $\overline{SAL}$ is active-low; $\overline{Vccsw}$ pin will be set to high when this occurs; and
3. STM1403C: V_{OUT} is driven to ground when $\overline{SAL}$ is active-low; $\overline{Vccsw}$ pin will be set to high when this occurs.

2.1.11 V_{TPU}

For STM1403B and STM1403C, this pin provides pull-up voltage for the physical tamper pins (TP1-4). This pin is not to be used as voltage supply source for any other purpose.

Note: V_{TPU} is the internally switched supply voltage from either the V_{CC} pin or the V_{BAT} pin.

2.1.12 V_{CC}

This is the supply voltage (2.2 V to 3.6 V).

2.1.13 V_{BAT}

This is the secondary (backup battery) supply voltage. The pin is connected to the positive terminal of the battery with a rectifying diode like the BAT54J from STMicroelectronics for reverse charge protection. Voltage at this pin, after diode rectification, will be approximately 0.2 V less than the battery voltage, and will depend on the type of battery used as well as the I_{BAT} being drawn. (A capacitor of at least 1.0 µF connected between the V_{BAT} pin and V_{SS} is required.) If no battery is used, connect the V_{BAT} pin to the V_{CC} pin.

2.1.14 V_{SS}

Ground, V_{SS}, is the reference for the power supply. It must be connected to system ground.

3 Operation

3.1 Reset input

The STM1403 security supervisor asserts a reset signal to the MCU whenever V_{CC} goes below the reset threshold (V_{RST}), or when the push-button reset input ($\overline{MR}$) is taken low. $\overline{RST}$ is guaranteed to be a logic low for 0 V < V_{CC} < V_{RST} if V_{BAT} is greater than 1 V. Without a backup battery, $\overline{RST}$ is guaranteed valid down to V_{CC} =1 V.

During power-up, once V_{CC} exceeds the reset threshold an internal timer keeps $\overline{RST}$ low for the reset time-out period, t_{rec}. After this interval $\overline{RST}$ returns high.

If V_{CC} drops below the reset threshold, $\overline{RST}$ goes low. Each time $\overline{RST}$ is asserted, it stays low for at least the reset time-out period (t_{rec}). Any time V_{CC} goes below the reset threshold the internal timer clears. The reset timer starts when V_{CC} returns above the reset threshold.

3.2 Push-button reset input

A logic low on $\overline{MR}$ asserts reset. Reset remains asserted while $\overline{MR}$ is low, and for t_{rec} (see *Figure 25 on page 24*) after it returns high. The $\overline{MR}$ input has an internal 40 kΩ pull-up resistor, allowing it to be left open if not used. This input can be driven with TTL/CMOS-logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to ground to create a manual reset function; external debounce circuitry is not required. If $\overline{MR}$ is driven from long cables or the device is used in a noisy environment, connect a 0.1 µF capacitor from $\overline{MR}$ to V_{SS} to provide additional noise immunity. $\overline{MR}$ may float, or be tied to V_{CC} when not used.

3.3 Backup battery switchover

In the event of a power failure, it may be necessary to preserve the contents of external SRAM through V_{OUT}. With a backup battery installed with voltage V_{BAT}, the devices automatically switch the SRAM to the backup supply when V_{CC} falls.

Note: If backup battery is not used, connect both V_{BAT} and V_{OUT} to V_{CC}.

This family of security supervisors does not always connect V_{BAT} to V_{OUT} when V_{BAT} is greater than V_{CC}. V_{BAT} connects to V_{OUT} (through a 100 Ω switch) when V_{CC} is below V_{SW} (~2.4 V) or V_{BAT} (whichever is lower). This is done to allow the backup battery (e.g., a 3.6 V battery) to have a higher voltage than V_{CC}.

Assuming that V_{BAT} > 2.0 V, switchover at V_{SO} ensures that battery backup mode is entered before V_{OUT} gets too close to the 2.0 V minimum required to reliably retain data in most external SRAMs. When V_{CC} recovers, hysteresis is used to avoid oscillation around the V_{SO} point. V_{OUT} is connected to V_{CC} through a 3 Ω PMOS power switch.

Note: The backup battery may be removed while V_{CC} is valid, assuming V_{BAT} is adequately decoupled (0.1 µF typ), without danger of triggering a reset.

Table 3. I/O status in battery backup

Pin	Status
V_{OUT}	Connected to V_{BAT} through internal switch
V_{CC}	Disconnected from V_{OUT}
PFI	Disabled
$\overline{PFO}$	Logic low
$\overline{MR}$	Disabled
$\overline{RST}$	Logic low
V_{BAT}	Connected to V_{OUT}
$\overline{Vccsw}$	Logic high
V_{REF}	Pulled to V_{SS} below 2.4 V (V_{SW})
$\overline{BLD}$	Logic high
V_{TPU}	Connected to V_{BAT} through an internal switch

3.4 Power-fail input/output

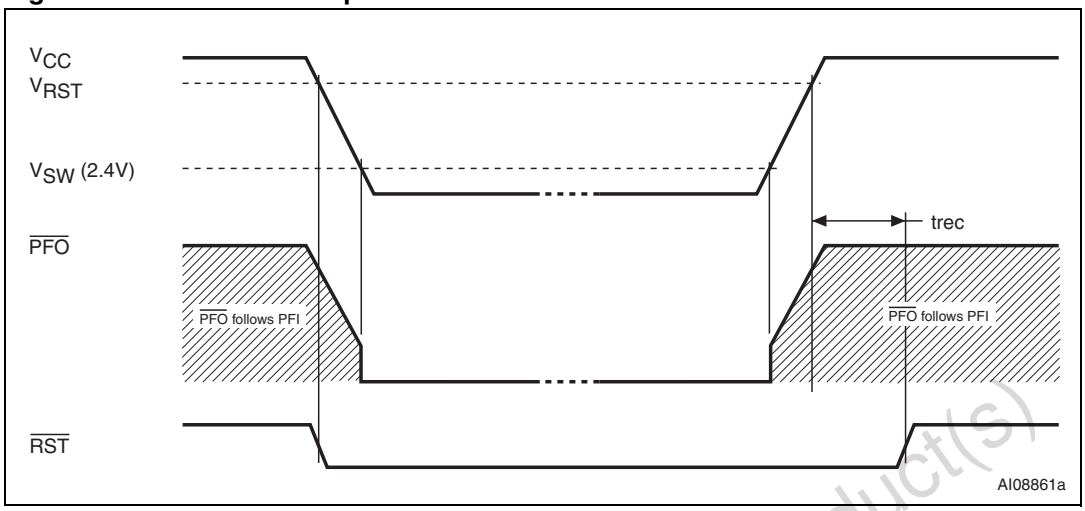
The power-fail input (PFI) is compared to an internal reference voltage (independent from the V_{RST} comparator). If PFI is less than the power-fail threshold (V_{PFI}), the power-fail output ($\overline{PFO}$) will go low. This function is intended for use as an undervoltage detector to signal a failing power supply. Typically PFI is connected through an external voltage divider (see *Figure 4 on page 9*) to either the unregulated DC input (if it is available) or the regulated output of the V_{CC} regulator. The voltage divider can be set up such that the voltage at PFI falls below V_{PFI} several milliseconds before the regulated V_{CC} input to the STM1403 or the microprocessor drops below the minimum operating voltage.

During battery backup, the power-fail comparator is turned off and $\overline{PFO}$ goes (or remains) low (see *Figure 9 on page 16*). This occurs after V_{CC} drops below V_{SW} (~2.4V). When power returns, the power-fail comparator is enabled and $\overline{PFO}$ follows PFI. If the comparator is unused, PFI should be connected to V_{SS} and $\overline{PFO}$ left unconnected. $\overline{PFO}$ may be connected to $\overline{MR}$ so that a low voltage on PFI will generate a reset output.

3.5 Applications information

These supervisor circuits are not short-circuit protected. Shorting V_{OUT} to ground - excluding power-up transients such as charging a decoupling capacitor - destroys the device. Decouple both V_{CC} and V_{BAT} pins to ground by placing 0.1 µF capacitors as close to the device as possible.

Figure 9. Power-fail comparator waveform

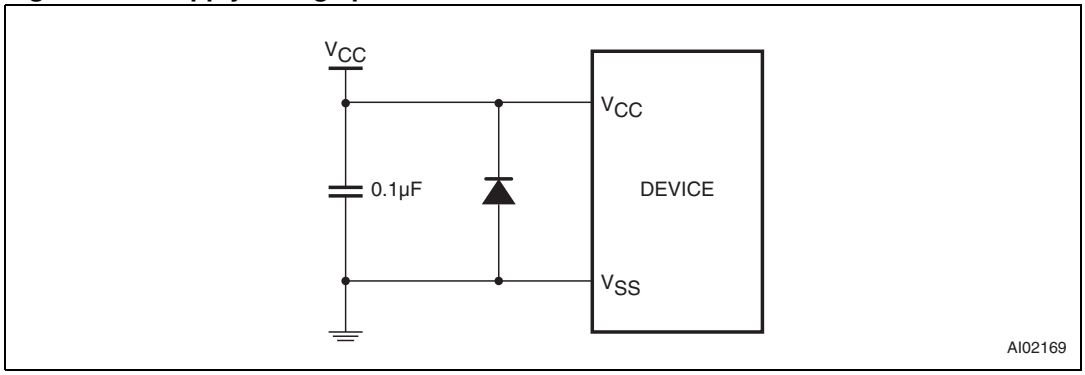


3.6 Negative-going V_{CC} transients and undershoot

The STM1403 devices are relatively immune to negative-going V_{CC} transients (glitches). *Figure 23 on page 22* was generated using a negative pulse applied to V_{CC}, starting at V_{RST} + 0.3 V and ending below the reset threshold by the magnitude indicated (comparator overdrive). The graph indicates the maximum pulse width a negative V_{CC} transient can have without causing a reset pulse. As the magnitude of the transient increases (further below the threshold), the maximum allowable pulse width decreases. Any combination of duration and overdrive which lies under the curve will NOT generate a reset signal. Typically, a V_{CC} transient that goes 100 mV below the reset threshold and lasts 40 µs or less will not cause a reset pulse. A 0.1 µF bypass capacitor mounted as close as possible to the V_{CC} pin provides additional transient immunity (see *Figure 10*).

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, STMicroelectronics recommends connecting a Schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

Figure 10. Supply voltage protection



4 Tamper detection

4.1 Physical

There are four (4) high-impedance physical tamper detect input pins, 2 normally set to high (NH) and 2 normally set to low (NL). Each input is designed with a glitch immunity (see *Table 7 on page 28*). These inputs can be connected externally to several types of actuator devices (e.g., switches, wire mesh). A tamper on any one of the four inputs that causes its state to change will trigger the security alarm ($\overline{SAL}$) and drive it to active-low. Once the tamper condition no longer exists, the $\overline{SAL}$ will return to its normal high state.

TP_1 and TP_3 are set normally to high (NH). They are connected externally through a closed switch or a high-impedance resistor to V_{OUT} (in the case of STM1403A) or V_{TPU} (in the case of STM1403B/C), A tamper condition will be detected when the input pin is pulled low (see *Figure 5* and *Figure 6*). If not used, tie the pin to V_{OUT} or V_{TPU}.

TP_2 and TP_4 are set normally to low (NL). They are connected externally through a high-impedance resistor or a closed switch to V_{SS}. A tamper condition will be detected when the input pin is pulled high (see *Figure 7* and *Figure 8*). If not used, tie the pin to V_{SS}.

4.2 Supply voltage

The internally switched supply voltage, V_{INT} (either V_{CC} input or V_{BAT} input) is continuously monitored. If V_{INT} should exceed the over voltage trip point, V_{HV} (set at 4.2V, typical), or should go below the under voltage trip point, V_{LV} (set at 2.0 V, typical). $\overline{SAL}$ will be driven active-low. Once the tamper condition no longer exists, the $\overline{SAL}$ pin will return to its normal high state.

When no tamper condition exists, $\overline{SAL}$ is normally high (see *Section 2: Pin descriptions on page 11*).

When a tamper is detected, the $\overline{SAL}$ is activated (driven low), independent of the part type. V_{OUT} can be driven to one of three states, depending on which variant of STM1403 is being used (see *Table 1: Device summary on page 1*):

- ON
- High-Z or
- Ground (V_{SS})

Note: The STM1403 must be initially powered above V_{RST} to enable the tamper detection alarms. For example, if the battery is on while V_{CC} = 0 V, no alarm condition can be detected until V_{CC} rises above V_{RST} (and t_{rec} expires). From this point on, alarms can be detected either on battery or V_{CC}. This is done to avoid false alarms when the device goes from no power to its operational state.

5 Typical operating characteristics

Note: Typical values are at T_A = 25 °C.

Figure 11. V_{BAT} -to-V_{OUT} on-resistance vs. temperature

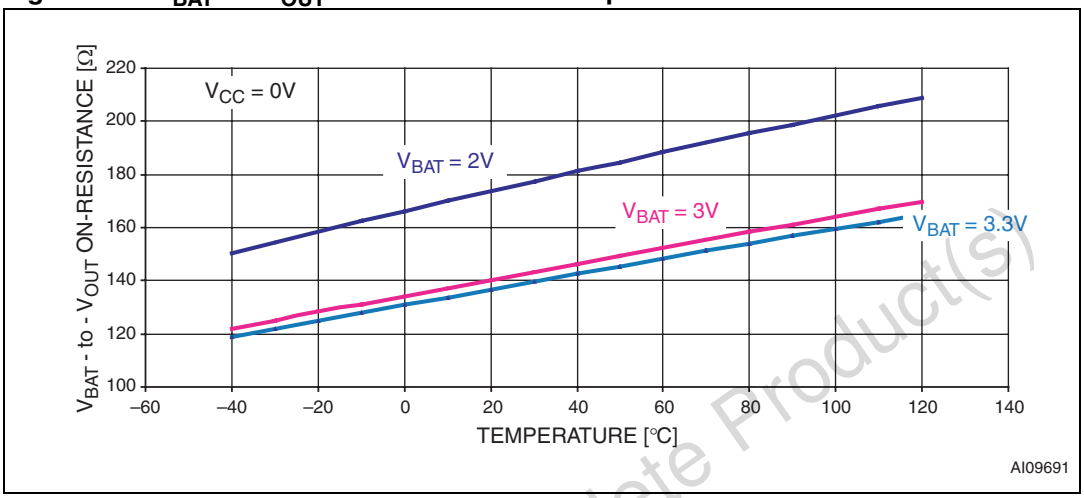


Figure 12. Supply current vs. temperature (no load)

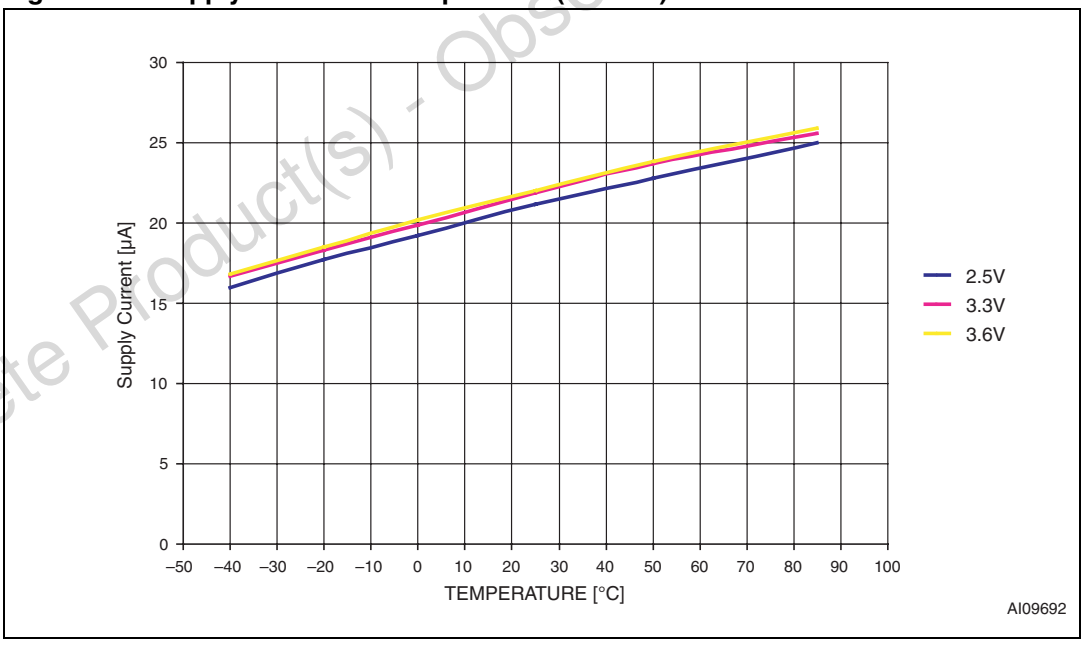


Figure 13. V_{PFI} threshold vs. temperature

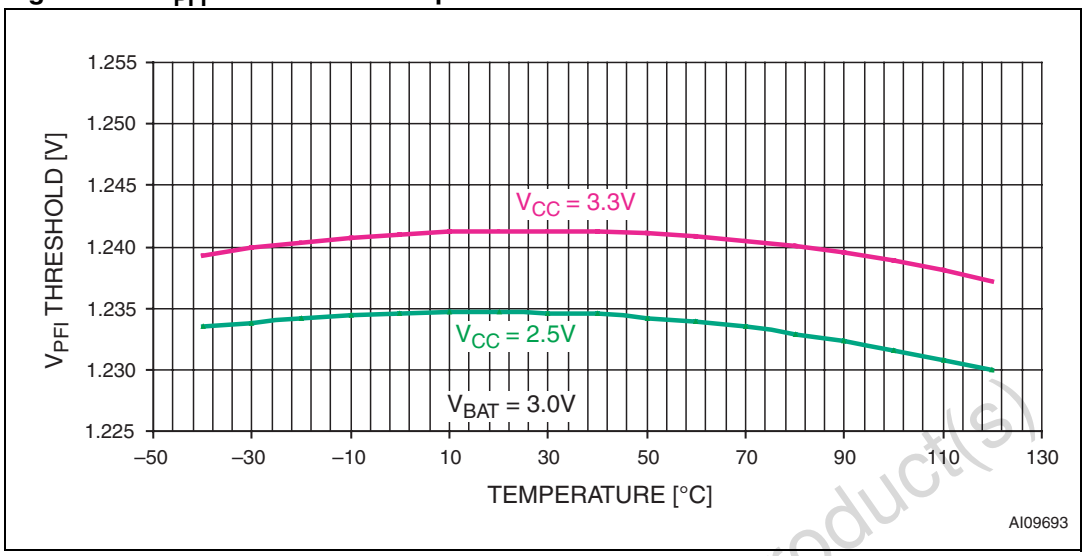


Figure 14. Reset comparator propagation delay vs. temperature

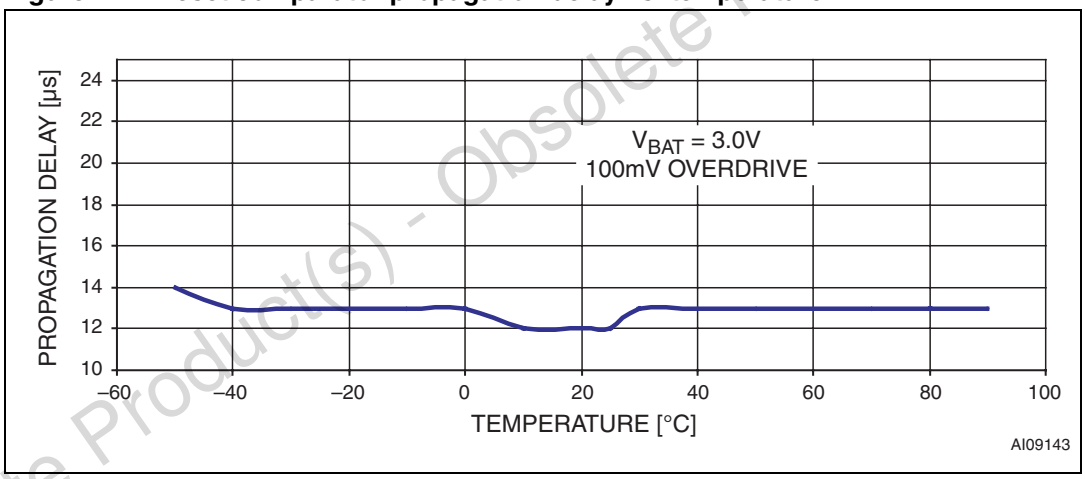


Figure 15. Power-up t_{rec} vs. temperature

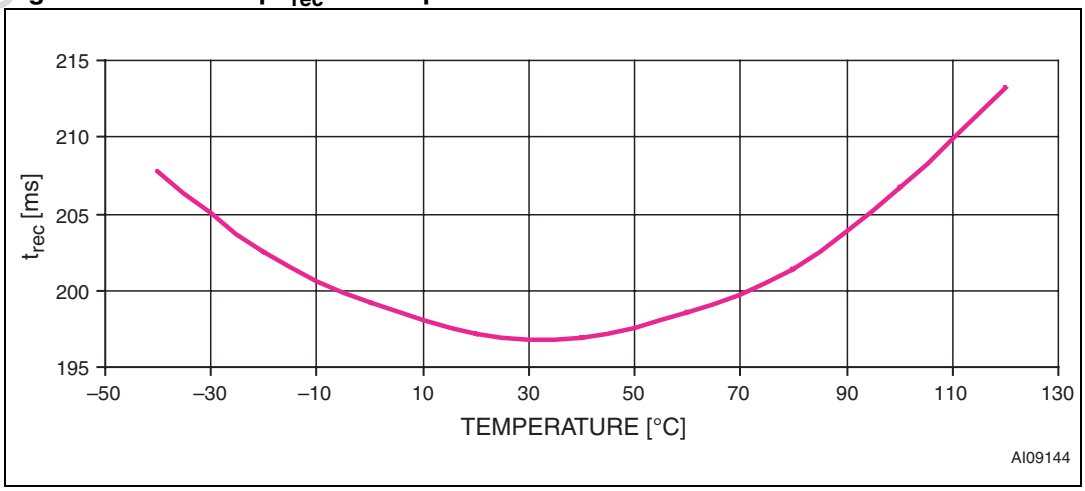


Figure 16. Normalized reset threshold vs. temperature

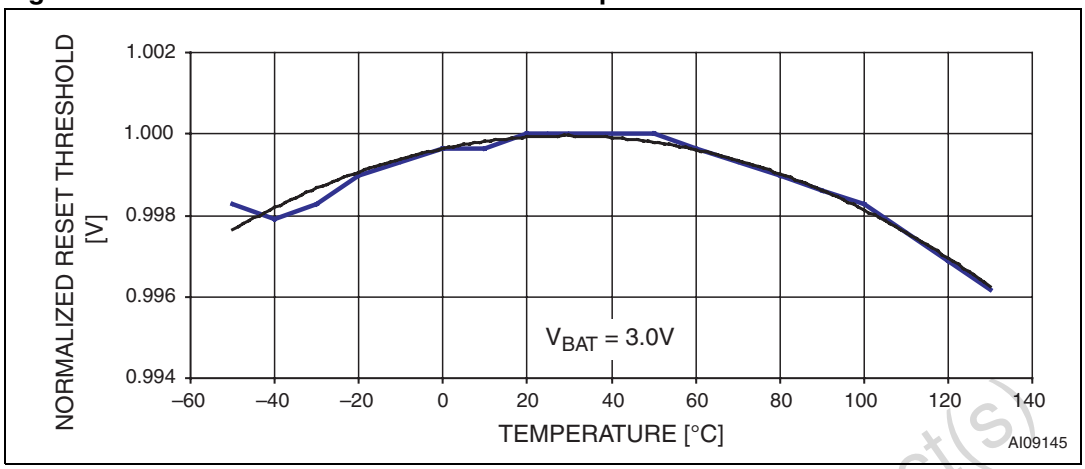


Figure 17. PFI to $\overline{PFO}$ propagation delay vs. temperature

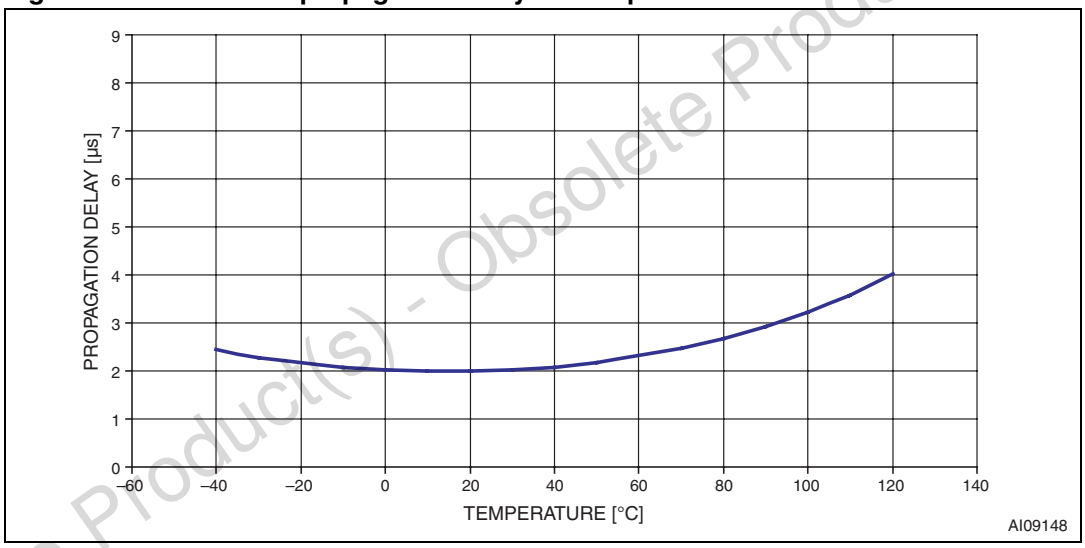


Figure 18. $\overline{RST}$ output voltage vs. supply voltage

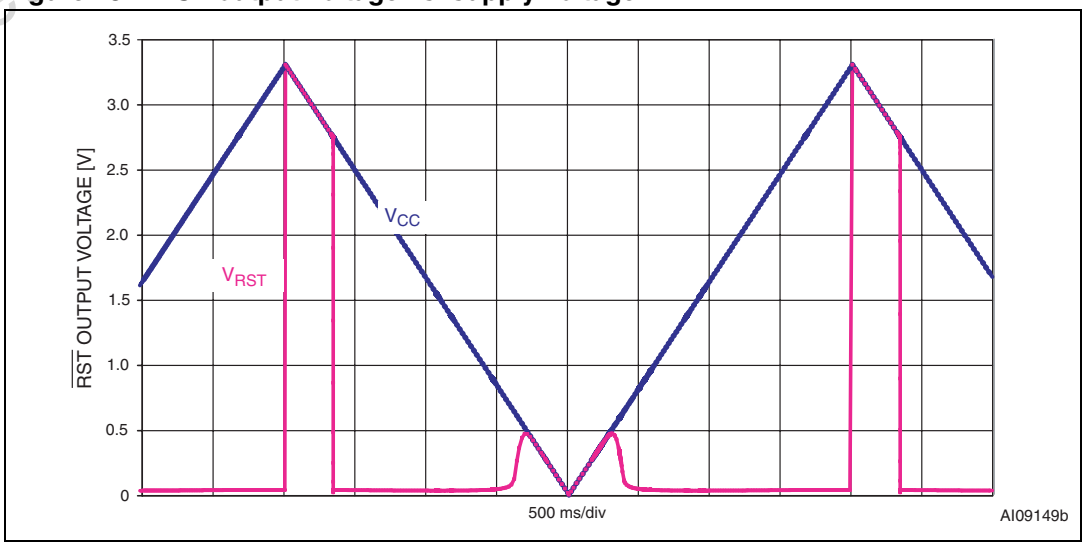


Figure 19. $\overline{RST}$ response time (assertion)

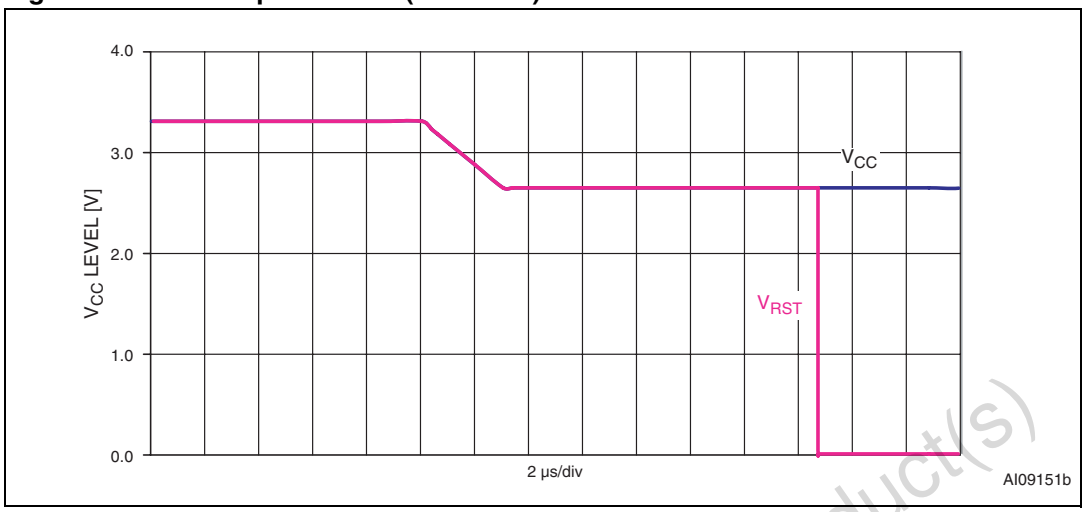


Figure 20. Power-fail comparator response time (assertion)

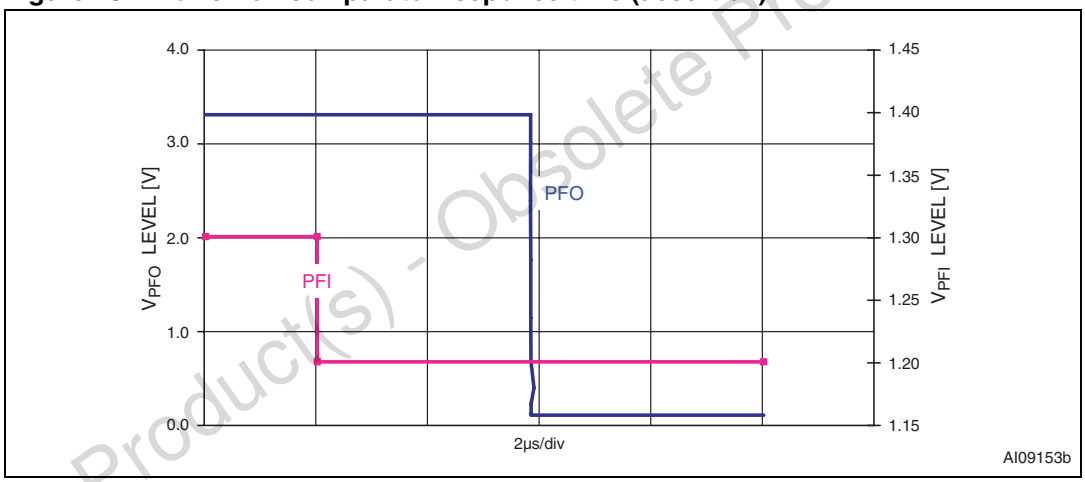


Figure 21. Power-fail comparator response time (de-assertion)

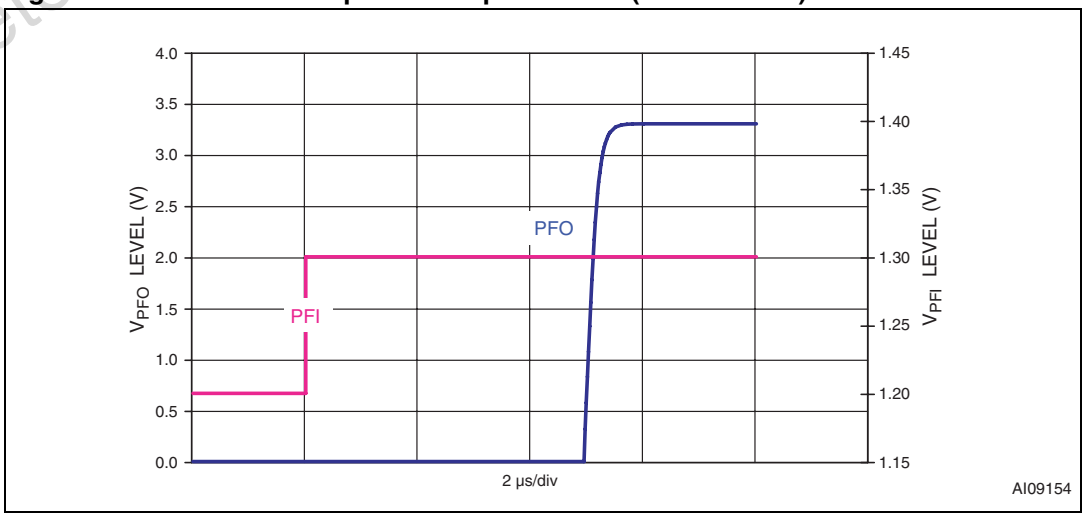


Figure 22. V_{CC} to reset propagation delay vs. temperature

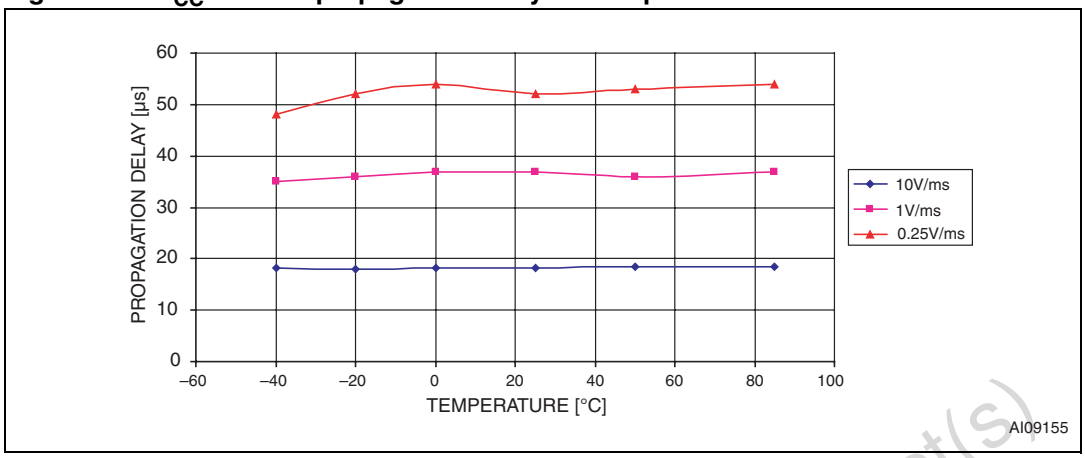
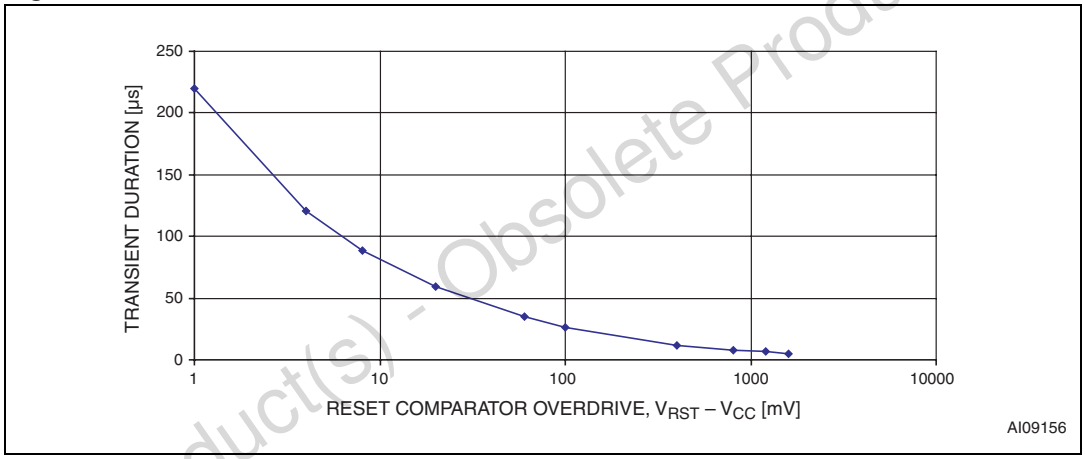


Figure 23. Maximum transient duration vs. reset threshold overdrive



6 Maximum ratings

Stressing the device above the ratings listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature (V_{CC} off, V_{BAT} off)	–55 to 150	°C
T_{SLD}(1)	Lead solder temperature for 10 seconds	260	°C
V_{IO}	Input or output voltage	–0.3 to V_{CC} +0.3	V
V_{CC}/V_{BAT}	Supply voltage	–0.3 to 4.5	V
I_O	Output current	20	mA
P_D	Power dissipation	320	mW

1. Reflow at peak temperature of 255 °C to 260 °C for < 30 seconds (total thermal budget not to exceed 180 °C for between 90 to 150 seconds).

7 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in *Table 5: Operating and AC measurement condition*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 5. Operating and AC measurement condition

Parameter	STM1403	Unit
V_{CC}/V_{BAT} supply voltage	2.2 to 3.6	V
Ambient operating temperature (T_A)	–40 to 85	°C
Input rise and fall times	≤ 5	ns
Input pulse voltages	0.2 to $0.8V_{CC}$	V
Input and output timing ref. voltages	0.3 to $0.7V_{CC}$	V

Figure 24. AC testing input/output waveforms

Figure 25. $\overline{MR}$ timing waveform

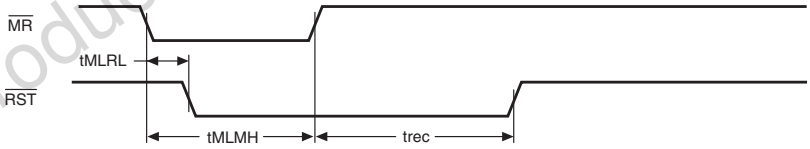


Figure 26. STM1403 switchover diagram, condition A ($V_{BAT} < V_{SW}$)

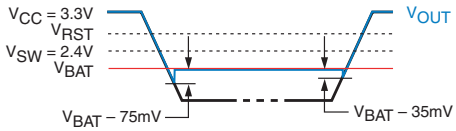


Figure 27. STM1403 switchover diagram, condition B ($V_{BAT} > V_{SW}$)

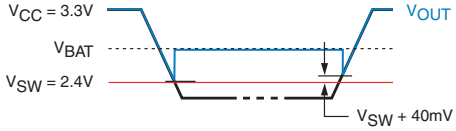


Table 6. DC and AC characteristics

Sym	Alter-native	Description	Test condition(1)	Min	Typ	Max	Unit
V_{CC}, V_{BAT}(2)		Operating voltage	T_A = –40 to +85 °C	2.2		3.6	V
I_{CC}		V_{CC} supply current (STM1403A)	Typ @ 3.3 V, 25 °C		45	60	µA
		V_{CC} supply current (STM1403B,C)			30	45	µA
		V_{CC} supply current in battery backup mode	Excluding I_{OUT} (V_{BAT} = 2.3 V, V_{CC} = 2.0 V, $\overline{MR}$ = V_{CC})		25	35	µA
I_{BAT}(3)		V_{BAT} supply current in battery backup mode	Excluding I_{OUT} (V_{BAT} = 3.6 V)		2.8	4.0	µA
V_{OUT1}		V_{OUT} voltage (active)	I_{OUT1} = 5 mA(4) (V_{CC} > V_{SW})	V_{CC} – 0.03	V_{CC} – 0.015		V
			I_{OUT1} = 80 mA (V_{CC} > V_{SW})	V_{CC} – 0.3	V_{CC} – 0.15		V
			I_{OUT1} = 250 µA, V_{CC} > V_{SW}(4)	V_{CC} – 0.0015	V_{CC} – 0.0006		V
V_{OUT2}		V_{OUT} voltage (battery backup)	I_{OUT2} = 250 µA, V_{BAT} = 2.2 V	V_{BAT} – 0.1	V_{BAT} – 0.04		V
			I_{OUT2} = 1 mA, V_{BAT} = 2.2 V		V_{BAT} – 0.16		V
V_{TPU1}		Internal switched supply voltage (active)	I_{SOURCE} = 500 µA (V_{CC} > V_{SW})	V_{CC} – 0.3			V
V_{TPU2}		Internal switched supply voltage (battery backup)	I_{SOURCE} = 100 µA (V_{BAT} = 2.2 V)		V_{BAT} – 0.10		V
I_{LI}		Input leakage current ($\overline{MR}$)	$\overline{MR}$ = 0 V; V_{CC} = 3 V	20	75	350	µA
		Input leakage current (PFI)	0 V = V_{IN} = V_{CC}	–25	2	+25	nA
		Input leakage current (TP1-TP4)	0 V = V_{IN} = V_{CC}	–1		+1	µA
I_{LO}		Output leakage current	0 V = V_{IN} = V_{CC}(5)	–1		+1	µA
V_{IH}		Input high voltage ($\overline{MR}$)	V_{RST} (max) < V_{CC} < 3.6 V	0.7V_{CC}			V
V_{IL}		Input low voltage ($\overline{MR}$)				0.3V_{CC}	V
V_{OL}		Output low voltage ($\overline{PFO}$, $\overline{RST}$, Vccsw, $\overline{SAL}$, $\overline{BLD}$)	V_{CC} = V_{RST} (max), I_{SINK} = 3.2 mA			0.3	V
V_{OL}		Output low voltage ($\overline{RST}$)	I_{OL} = 40 µA; V_{CC} = 1.0 V; V_{BAT} = V_{CC}; T_A = 0 °C to 85 °C			0.3	V
			I_{OL} = 200 µA; V_{CC} = 1.2 V; V_{BAT} = V_{CC}			0.3	V