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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

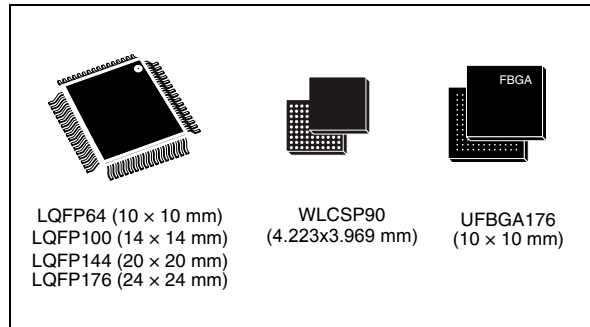


ARM Cortex-M4 32b MCU+FPU, 210DMIPS, up to 1MB Flash/192+4KB RAM, USB OTG HS/FS, Ethernet, 17 TIMs, 3 ADCs, 15 comm. interfaces & camera

Datasheet - production data

Features

- Core: ARM® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution from Flash memory, frequency up to 168 MHz, memory protection unit, 210 DMIPS/1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Memories
 - Up to 1 Mbyte of Flash memory
 - Up to 192+4 Kbytes of SRAM including 64-Kbyte of CCM (core coupled memory) data RAM
 - Flexible static memory controller supporting Compact Flash, SRAM, PSRAM, NOR and NAND memories
 - LCD parallel interface, 8080/6800 modes
 - Clock, reset and supply management
 - 1.8 V to 3.6 V application supply and I/Os
 - POR, PDR, PVD and BOR
 - 4-to-26 MHz crystal oscillator
 - Internal 16 MHz factory-trimmed RC (1% accuracy)
 - 32 kHz oscillator for RTC with calibration
 - Internal 32 kHz RC with calibration
 - Low-power operation
 - Sleep, Stop and Standby modes
 - V_{BAT} supply for RTC, 20×32 bit backup registers + optional 4 KB backup SRAM
 - 3×12-bit, 2.4 MSPS A/D converters: up to 24 channels and 7.2 MSPS in triple interleaved mode
 - 2×12-bit D/A converters
 - General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Up to 17 timers: up to twelve 16-bit and two 32-bit timers up to 168 MHz, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
- Debug mode
 - Serial wire debug (SWD) & JTAG interfaces
 - Cortex-M4 Embedded Trace Macrocell™
- Up to 140 I/O ports with interrupt capability
 - Up to 136 fast I/Os up to 84 MHz
 - Up to 138 5 V-tolerant I/Os
- Up to 15 communication interfaces
 - Up to 3 × I²C interfaces (SMBus/PMBus)
 - Up to 4 USARTs/2 UARTs (10.5 Mbit/s, ISO 7816 interface, LIN, IrDA, modem control)
 - Up to 3 SPIs (42 Mbits/s), 2 with muxed full-duplex I²S to achieve audio class accuracy via internal audio PLL or external clock
 - 2 × CAN interfaces (2.0B Active)
 - SDIO interface
- Advanced connectivity
 - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
 - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
 - 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII



- 8- to 14-bit parallel camera interface up to 54 Mbytes/s
- True random number generator
- CRC calculation unit
- 96-bit unique ID
- RTC: subsecond accuracy, hardware calendar

Table 1. Device summary

| Reference | Part number |
|-------------|--|
| STM32F405xx | STM32F405RG, STM32F405VG, STM32F405ZG, STM32F405OG, STM32F405OE |
| STM32F407xx | STM32F407VG, STM32F407IG, STM32F407ZG, STM32F407VE, STM32F407ZE, STM32F407IE |

Contents

| | | |
|----------|--|-----------|
| 1 | Introduction | 12 |
| 2 | Description | 13 |
| 2.1 | Full compatibility throughout the family | 16 |
| 2.2 | Device overview | 19 |
| 2.2.1 | ARM® Cortex®-M4 core with FPU and embedded Flash and SRAM | 20 |
| 2.2.2 | Adaptive real-time memory accelerator (ART Accelerator™) | 20 |
| 2.2.3 | Memory protection unit | 20 |
| 2.2.4 | Embedded Flash memory | 20 |
| 2.2.5 | CRC (cyclic redundancy check) calculation unit | 21 |
| 2.2.6 | Embedded SRAM | 21 |
| 2.2.7 | Multi-AHB bus matrix | 21 |
| 2.2.8 | DMA controller (DMA) | 22 |
| 2.2.9 | Flexible static memory controller (FSMC) | 23 |
| 2.2.10 | Nested vectored interrupt controller (NVIC) | 23 |
| 2.2.11 | External interrupt/event controller (EXTI) | 23 |
| 2.2.12 | Clocks and startup | 23 |
| 2.2.13 | Boot modes | 24 |
| 2.2.14 | Power supply schemes | 24 |
| 2.2.15 | Power supply supervisor | 24 |
| 2.2.16 | Voltage regulator | 26 |
| 2.2.17 | Regulator ON/OFF and internal reset ON/OFF availability | 29 |
| 2.2.18 | Real-time clock (RTC), backup SRAM and backup registers | 29 |
| 2.2.19 | Low-power modes | 30 |
| 2.2.20 | V _{BAT} operation | 31 |
| 2.2.21 | Timers and watchdogs | 31 |
| 2.2.22 | Inter-integrated circuit interface (I ² C) | 34 |
| 2.2.23 | Universal synchronous/asynchronous receiver transmitters (USART) | 34 |
| 2.2.24 | Serial peripheral interface (SPI) | 35 |
| 2.2.25 | Inter-integrated sound (I2S) | 35 |
| 2.2.26 | Audio PLL (PLLI2S) | 36 |
| 2.2.27 | Secure digital input/output interface (SDIO) | 36 |
| 2.2.28 | Ethernet MAC interface with dedicated DMA and IEEE 1588 support | 36 |
| 2.2.29 | Controller area network (bxCAN) | 37 |

| | | |
|----------|---|-----------|
| 2.2.30 | Universal serial bus on-the-go full-speed (OTG_FS) | 37 |
| 2.2.31 | Universal serial bus on-the-go high-speed (OTG_HS) | 38 |
| 2.2.32 | Digital camera interface (DCMI) | 38 |
| 2.2.33 | Random number generator (RNG) | 38 |
| 2.2.34 | General-purpose input/outputs (GPIOs) | 38 |
| 2.2.35 | Analog-to-digital converters (ADCs) | 39 |
| 2.2.36 | Temperature sensor | 39 |
| 2.2.37 | Digital-to-analog converter (DAC) | 39 |
| 2.2.38 | Serial wire JTAG debug port (SWJ-DP) | 40 |
| 2.2.39 | Embedded Trace Macrocell™ | 40 |
| 3 | Pinouts and pin description | 41 |
| 4 | Memory mapping | 71 |
| 5 | Electrical characteristics | 76 |
| 5.1 | Parameter conditions | 76 |
| 5.1.1 | Minimum and maximum values | 76 |
| 5.1.2 | Typical values | 76 |
| 5.1.3 | Typical curves | 76 |
| 5.1.4 | Loading capacitor | 76 |
| 5.1.5 | Pin input voltage | 76 |
| 5.1.6 | Power supply scheme | 77 |
| 5.1.7 | Current consumption measurement | 78 |
| 5.2 | Absolute maximum ratings | 78 |
| 5.3 | Operating conditions | 79 |
| 5.3.1 | General operating conditions | 79 |
| 5.3.2 | VCAP_1/VCAP_2 external capacitor | 82 |
| 5.3.3 | Operating conditions at power-up / power-down (regulator ON) | 82 |
| 5.3.4 | Operating conditions at power-up / power-down (regulator OFF) | 82 |
| 5.3.5 | Embedded reset and power control block characteristics | 83 |
| 5.3.6 | Supply current characteristics | 84 |
| 5.3.7 | Wakeup time from low-power mode | 98 |
| 5.3.8 | External clock source characteristics | 99 |
| 5.3.9 | Internal clock source characteristics | 103 |
| 5.3.10 | PLL characteristics | 104 |
| 5.3.11 | PLL spread spectrum clock generation (SSCG) characteristics | 106 |

| | | |
|-------------------|--|------------|
| 5.3.12 | Memory characteristics | 108 |
| 5.3.13 | EMC characteristics | 110 |
| 5.3.14 | Absolute maximum ratings (electrical sensitivity) | 112 |
| 5.3.15 | I/O current injection characteristics | 113 |
| 5.3.16 | I/O port characteristics | 114 |
| 5.3.17 | NRST pin characteristics | 118 |
| 5.3.18 | TIM timer characteristics | 119 |
| 5.3.19 | Communications interfaces | 121 |
| 5.3.20 | CAN (controller area network) interface | 133 |
| 5.3.21 | 12-bit ADC characteristics | 133 |
| 5.3.22 | Temperature sensor characteristics | 138 |
| 5.3.23 | V _{BAT} monitoring characteristics | 139 |
| 5.3.24 | Embedded reference voltage | 139 |
| 5.3.25 | DAC electrical characteristics | 139 |
| 5.3.26 | FSMC characteristics | 142 |
| 5.3.27 | Camera interface (DCMI) timing specifications | 161 |
| 5.3.28 | SD/SDIO MMC card host interface (SDIO) characteristics | 162 |
| 5.3.29 | RTC characteristics | 163 |
| 6 | Package information | 164 |
| 6.1 | WLCSP90 package information | 164 |
| 6.2 | LQFP64 package information | 167 |
| 6.3 | LQFP100 package information | 170 |
| 6.4 | LQFP144 package information | 173 |
| 6.5 | UFBGA176+25 package information | 177 |
| 6.6 | LQFP176 package information | 180 |
| 6.7 | Thermal characteristics | 184 |
| 7 | Part numbering | 185 |
| Appendix A | Application block diagrams | 186 |
| A.1 | USB OTG full speed (FS) interface solutions | 186 |
| A.2 | USB OTG high speed (HS) interface solutions | 188 |
| A.3 | Ethernet interface solutions | 189 |
| 8 | Revision history | 191 |

List of tables

| | | |
|-----------|--|-----|
| Table 1. | Device summary | 2 |
| Table 2. | STM32F405xx and STM32F407xx: features and peripheral counts. | 14 |
| Table 3. | Regulator ON/OFF and internal reset ON/OFF availability. | 29 |
| Table 4. | Timer feature comparison. | 31 |
| Table 5. | USART feature comparison | 35 |
| Table 6. | Legend/abbreviations used in the pinout table | 46 |
| Table 7. | STM32F40xxx pin and ball definitions | 47 |
| Table 8. | FSMC pin definition | 59 |
| Table 9. | Alternate function mapping | 62 |
| Table 10. | register boundary addresses | 72 |
| Table 11. | Voltage characteristics | 78 |
| Table 12. | Current characteristics | 79 |
| Table 13. | Thermal characteristics. | 79 |
| Table 14. | General operating conditions | 79 |
| Table 15. | Limitations depending on the operating power supply range | 81 |
| Table 16. | VCAP_1/VCAP_2 operating conditions | 82 |
| Table 17. | Operating conditions at power-up / power-down (regulator ON) | 82 |
| Table 18. | Operating conditions at power-up / power-down (regulator OFF). | 82 |
| Table 19. | Embedded reset and power control block characteristics. | 83 |
| Table 20. | Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM | 85 |
| Table 21. | Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled) | 86 |
| Table 22. | Typical and maximum current consumption in Sleep mode | 89 |
| Table 23. | Typical and maximum current consumptions in Stop mode | 90 |
| Table 24. | Typical and maximum current consumptions in Standby mode | 90 |
| Table 25. | Typical and maximum current consumptions in V _{BAT} mode. | 91 |
| Table 26. | Typical current consumption in Run mode, code with data processing running from Flash memory, regulator ON (ART accelerator enabled except prefetch), V _{DD} = 1.8 V. | 93 |
| Table 27. | Switching output I/O current consumption | 95 |
| Table 28. | Peripheral current consumption | 96 |
| Table 29. | Low-power mode wakeup timings | 99 |
| Table 30. | High-speed external user clock characteristics. | 99 |
| Table 31. | Low-speed external user clock characteristics | 100 |
| Table 32. | HSE 4-26 MHz oscillator characteristics | 101 |
| Table 33. | LSE oscillator characteristics (f _{LSE} = 32.768 kHz) | 102 |
| Table 34. | HSI oscillator characteristics | 103 |
| Table 35. | LSI oscillator characteristics | 103 |
| Table 36. | Main PLL characteristics. | 104 |
| Table 37. | PLLI2S (audio PLL) characteristics | 105 |
| Table 38. | SSCG parameters constraint | 106 |
| Table 39. | Flash memory characteristics | 108 |
| Table 40. | Flash memory programming. | 108 |
| Table 41. | Flash memory programming with VPP | 110 |
| Table 42. | Flash memory endurance and data retention. | 110 |
| Table 43. | EMS characteristics | 111 |
| Table 44. | EMI characteristics | 112 |

| | | |
|-----------|--|-----|
| Table 45. | ESD absolute maximum ratings | 112 |
| Table 46. | Electrical sensitivities | 113 |
| Table 47. | I/O current injection susceptibility | 114 |
| Table 48. | I/O static characteristics | 114 |
| Table 49. | Output voltage characteristics | 116 |
| Table 50. | I/O AC characteristics | 117 |
| Table 51. | NRST pin characteristics | 119 |
| Table 52. | Characteristics of TIMx connected to the APB1 domain | 120 |
| Table 53. | Characteristics of TIMx connected to the APB2 domain | 121 |
| Table 54. | I2C analog filter characteristics | 121 |
| Table 55. | SPI dynamic characteristics | 122 |
| Table 56. | I2S dynamic characteristics | 126 |
| Table 57. | USB OTG FS startup time | 128 |
| Table 58. | USB OTG FS DC electrical characteristics | 128 |
| Table 59. | USB OTG FS electrical characteristics | 129 |
| Table 60. | USB HS DC electrical characteristics | 129 |
| Table 61. | USB HS clock timing parameters | 129 |
| Table 62. | ULPI timing | 130 |
| Table 63. | Ethernet DC electrical characteristics | 131 |
| Table 64. | Dynamic characteristics: Eternity MAC signals for SMI | 131 |
| Table 65. | Dynamic characteristics: Ethernet MAC signals for RMII | 132 |
| Table 66. | Dynamic characteristics: Ethernet MAC signals for MII | 133 |
| Table 67. | ADC characteristics | 133 |
| Table 68. | ADC accuracy at $f_{ADC} = 30$ MHz | 135 |
| Table 69. | Temperature sensor characteristics | 138 |
| Table 70. | Temperature sensor calibration values | 138 |
| Table 71. | V_{BAT} monitoring characteristics | 139 |
| Table 72. | Embedded internal reference voltage | 139 |
| Table 73. | Internal reference voltage calibration values | 139 |
| Table 74. | DAC characteristics | 139 |
| Table 75. | Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings | 143 |
| Table 76. | Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings | 144 |
| Table 77. | Asynchronous multiplexed PSRAM/NOR read timings | 145 |
| Table 78. | Asynchronous multiplexed PSRAM/NOR write timings | 146 |
| Table 79. | Synchronous multiplexed NOR/PSRAM read timings | 148 |
| Table 80. | Synchronous multiplexed PSRAM write timings | 149 |
| Table 81. | Synchronous non-multiplexed NOR/PSRAM read timings | 151 |
| Table 82. | Synchronous non-multiplexed PSRAM write timings | 152 |
| Table 83. | Switching characteristics for PC Card/CF read and write cycles in attribute/common space | 157 |
| Table 84. | Switching characteristics for PC Card/CF read and write cycles in I/O space | 158 |
| Table 85. | Switching characteristics for NAND Flash read cycles | 160 |
| Table 86. | Switching characteristics for NAND Flash write cycles | 161 |
| Table 87. | DCMI characteristics | 161 |
| Table 88. | Dynamic characteristics: SD / MMC characteristics | 163 |
| Table 89. | RTC characteristics | 163 |
| Table 90. | WLCSP90 - 4.223 x 3.969 mm, 0.400 mm pitch wafer level chip scale package mechanical data | 165 |
| Table 91. | WLCSP90 recommended PCB design rules | 166 |
| Table 92. | LQFP64 – 64-pin 10 x 10 mm low-profile quad flat package mechanical data | 167 |

| | | |
|------------|---|-----|
| Table 93. | LQPF100 – 100-pin, 14 x 14 mm low-profile quad flat package mechanical data | 170 |
| Table 94. | LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data | 174 |
| Table 95. | UFBGA176+25 ball, 10 × 10 × 0.65 mm pitch, ultra thin fine pitch ball grid array mechanical data | 177 |
| Table 96. | UFBGA176+2 recommended PCB design rules (0.65 mm pitch BGA) | 178 |
| Table 97. | LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package mechanical data | 180 |
| Table 98. | Package thermal characteristics | 184 |
| Table 99. | Ordering information scheme | 185 |
| Table 100. | Document revision history | 191 |

List of figures

| | | |
|------------|---|-----|
| Figure 1. | Compatible board design between STM32F10xx/STM32F40xxx for LQFP64 | 16 |
| Figure 2. | Compatible board design STM32F10xx/STM32F2/STM32F40xxx for LQFP100 package. | 17 |
| Figure 3. | Compatible board design between STM32F10xx/STM32F2/STM32F40xxx for LQFP144 package. | 17 |
| Figure 4. | Compatible board design between STM32F2 and STM32F40xxx for LQFP176 and BGA176 packages | 18 |
| Figure 5. | STM32F40xxx block diagram | 19 |
| Figure 6. | Multi-AHB matrix | 22 |
| Figure 7. | Power supply supervisor interconnection with internal reset OFF | 25 |
| Figure 8. | PDR_ON and NRST control with internal reset OFF | 26 |
| Figure 9. | Regulator OFF | 27 |
| Figure 10. | Startup in regulator OFF mode: slow V_{DD} slope - power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization | 28 |
| Figure 11. | Startup in regulator OFF mode: fast V_{DD} slope - power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization | 29 |
| Figure 12. | STM32F40xxx LQFP64 pinout | 41 |
| Figure 13. | STM32F40xxx LQFP100 pinout | 42 |
| Figure 14. | STM32F40xxx LQFP144 pinout | 43 |
| Figure 15. | STM32F40xxx LQFP176 pinout | 44 |
| Figure 16. | STM32F40xxx UFBGA176 ballout | 45 |
| Figure 17. | STM32F40xxx WLCSP90 ballout | 46 |
| Figure 18. | STM32F40xxx memory map. | 71 |
| Figure 19. | Pin loading conditions. | 76 |
| Figure 20. | Pin input voltage | 76 |
| Figure 21. | Power supply scheme | 77 |
| Figure 22. | Current consumption measurement scheme | 78 |
| Figure 23. | External capacitor C_{EXT} | 82 |
| Figure 24. | Typical current consumption versus temperature, Run mode, code with data processing running from Flash (ART accelerator ON) or RAM, and peripherals OFF | 87 |
| Figure 25. | Typical current consumption versus temperature, Run mode, code with data processing running from Flash (ART accelerator ON) or RAM, and peripherals ON | 87 |
| Figure 26. | Typical current consumption versus temperature, Run mode, code with data processing running from Flash (ART accelerator OFF) or RAM, and peripherals OFF | 88 |
| Figure 27. | Typical current consumption versus temperature, Run mode, code with data processing running from Flash (ART accelerator OFF) or RAM, and peripherals ON | 88 |
| Figure 28. | Typical V_{BAT} current consumption (LSE and RTC ON/backup RAM OFF) | 91 |
| Figure 29. | Typical V_{BAT} current consumption (LSE and RTC ON/backup RAM ON) | 92 |
| Figure 30. | High-speed external clock source AC timing diagram | 100 |
| Figure 31. | Low-speed external clock source AC timing diagram | 101 |
| Figure 32. | Typical application with an 8 MHz crystal | 102 |
| Figure 33. | Typical application with a 32.768 kHz crystal | 103 |
| Figure 34. | ACC_{LSI} versus temperature | 104 |
| Figure 35. | PLL output clock waveforms in center spread mode | 107 |
| Figure 36. | PLL output clock waveforms in down spread mode | 108 |
| Figure 37. | I/O AC characteristics definition | 118 |
| Figure 38. | Recommended NRST pin protection | 119 |
| Figure 39. | SPI timing diagram - slave mode and CPHA = 0 | 124 |

| | | |
|------------|---|-----|
| Figure 40. | SPI timing diagram - slave mode and CPHA = 1 | 124 |
| Figure 41. | SPI timing diagram - master mode | 125 |
| Figure 42. | I2S slave timing diagram (Philips protocol) | 127 |
| Figure 43. | I2S master timing diagram (Philips protocol) ⁽¹⁾ | 127 |
| Figure 44. | USB OTG FS timings: definition of data signal rise and fall time | 129 |
| Figure 45. | ULPI timing diagram | 130 |
| Figure 46. | Ethernet SMI timing diagram | 131 |
| Figure 47. | Ethernet RMII timing diagram | 132 |
| Figure 48. | Ethernet MII timing diagram | 132 |
| Figure 49. | ADC accuracy characteristics | 136 |
| Figure 50. | Typical connection diagram using the ADC | 136 |
| Figure 51. | Power supply and reference decoupling (V_{REF+} not connected to V_{DDA}) | 137 |
| Figure 52. | Power supply and reference decoupling (V_{REF+} connected to V_{DDA}) | 138 |
| Figure 53. | 12-bit buffered /non-buffered DAC | 142 |
| Figure 54. | Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms | 143 |
| Figure 55. | Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms | 144 |
| Figure 56. | Asynchronous multiplexed PSRAM/NOR read waveforms | 145 |
| Figure 57. | Asynchronous multiplexed PSRAM/NOR write waveforms | 146 |
| Figure 58. | Synchronous multiplexed NOR/PSRAM read timings | 147 |
| Figure 59. | Synchronous multiplexed PSRAM write timings | 149 |
| Figure 60. | Synchronous non-multiplexed NOR/PSRAM read timings | 150 |
| Figure 61. | Synchronous non-multiplexed PSRAM write timings | 152 |
| Figure 62. | PC Card/CompactFlash controller waveforms for common memory read access | 153 |
| Figure 63. | PC Card/CompactFlash controller waveforms for common memory write access | 154 |
| Figure 64. | PC Card/CompactFlash controller waveforms for attribute memory read access | 155 |
| Figure 65. | PC Card/CompactFlash controller waveforms for attribute memory write access | 156 |
| Figure 66. | PC Card/CompactFlash controller waveforms for I/O space read access | 156 |
| Figure 67. | PC Card/CompactFlash controller waveforms for I/O space write access | 157 |
| Figure 68. | NAND controller waveforms for read access | 159 |
| Figure 69. | NAND controller waveforms for write access | 159 |
| Figure 70. | NAND controller waveforms for common memory read access | 160 |
| Figure 71. | NAND controller waveforms for common memory write access | 160 |
| Figure 72. | DCMI timing diagram | 161 |
| Figure 73. | SDIO high-speed mode | 162 |
| Figure 74. | SD default mode | 163 |
| Figure 75. | WLCSP90 - 4.223 x 3.969 mm, 0.400 mm pitch wafer level chip scale package outline | 164 |
| Figure 76. | WLCSP90 - 4.223 x 3.969 mm, 0.400 mm pitch wafer level chip scale recommended footprint | 165 |
| Figure 77. | WLCSP90 marking example (package top view) | 166 |
| Figure 78. | LQFP64 – 64-pin, 10 x 10 mm low-profile quad flat package outline | 167 |
| Figure 79. | LQFP64 – 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint | 168 |
| Figure 80. | LPQF64 marking example (package top view) | 169 |
| Figure 81. | LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline | 170 |
| Figure 82. | LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint | 171 |
| Figure 83. | LQFP100 marking example (package top view) | 172 |
| Figure 84. | LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline | 173 |
| Figure 85. | LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package | |

| | | |
|------------|--|-----|
| | recommended footprint | 175 |
| Figure 86. | LQFP144 marking example (package top view) | 176 |
| Figure 87. | UFBGA176+25 ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline | 177 |
| Figure 88. | UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array recommended footprint | 178 |
| Figure 89. | UFBGA176+25 marking example (package top view) | 179 |
| Figure 90. | LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package outline | 180 |
| Figure 91. | LQFP176 - 176-pin, 24 x 24 mm low profile quad flat recommended footprint. | 182 |
| Figure 92. | LQFP176 marking example (package top view) | 183 |
| Figure 93. | USB controller configured as peripheral-only and used in Full speed mode | 186 |
| Figure 94. | USB controller configured as host-only and used in full speed mode. | 186 |
| Figure 95. | USB controller configured in dual mode and used in full speed mode | 187 |
| Figure 96. | USB controller configured as peripheral, host, or dual-mode and used in high speed mode. | 188 |
| Figure 97. | MII mode using a 25 MHz crystal | 189 |
| Figure 98. | RMII with a 50 MHz oscillator | 189 |
| Figure 99. | RMII with a 25 MHz crystal and PHY with PLL | 190 |

1 Introduction

This datasheet provides the description of the STM32F405xx and STM32F407xx lines of microcontrollers. For more details on the whole STMicroelectronics STM32™ family, please refer to [Section 2.1: Full compatibility throughout the family](#).

The STM32F405xx and STM32F407xx datasheet should be read in conjunction with the STM32F4xx reference manual which is available from the STMicroelectronics website www.st.com.

For information on the Cortex®-M4 core, please refer to the Cortex®-M4 programming manual (PM0214) available from www.st.com.

2 Description

The STM32F405xx and STM32F407xx family is based on the high-performance ARM[®] Cortex[®]-M4 32-bit RISC core operating at a frequency of up to 168 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F405xx and STM32F407xx family incorporates high-speed embedded memories (Flash memory up to 1 Mbyte, up to 192 Kbytes of SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, three AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers, a true random number generator (RNG). They also feature standard and advanced communication interfaces.

- Up to three I²Cs
- Three SPIs, two I²Ss full duplex. To achieve audio class accuracy, the I2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus two UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI),
- Two CANs
- An SDIO/MMC interface
- Ethernet and the camera interface available on STM32F407xx devices only.

New advanced peripherals include an SDIO, an enhanced flexible static memory control (FSMC) interface (for devices offered in packages of 100 pins and more), a camera interface for CMOS sensors. Refer to [Table 2: STM32F405xx and STM32F407xx: features and peripheral counts](#) for the list of peripherals available on each part number.

The STM32F405xx and STM32F407xx family operates in the –40 to +105 °C temperature range from a 1.8 to 3.6 V power supply. The supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor: refer to [Section : Internal reset OFF](#). A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F405xx and STM32F407xx family offers devices in various packages ranging from 64 pins to 176 pins. The set of included peripherals changes with the device chosen.

These features make the STM32F405xx and STM32F407xx microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances



Figure 5 shows the general block diagram of the device family.

Table 2. STM32F405xx and STM32F407xx: features and peripheral counts

| Peripherals | | STM32F405RG | STM32F405OG | STM32F405VG | STM32F405ZG | STM32F405OE | STM32F407Vx | STM32F407Zx | STM32F407Ix | |
|-------------------------|------------------|----------------|--------------------|-------------|-------------|-------------|-------------|-------------|-------------|------|
| Flash memory in Kbytes | | 1024 | | | | 512 | 512 | 1024 | 512 | 1024 |
| SRAM in Kbytes | System | 192(112+16+64) | | | | | | | | |
| | Backup | 4 | | | | | | | | |
| FSMC memory controller | | No | Yes ⁽¹⁾ | | | | | | | |
| Ethernet | | No | | | | | Yes | | | |
| Timers | General-purpose | 10 | | | | | | | | |
| | Advanced-control | 2 | | | | | | | | |
| | Basic | 2 | | | | | | | | |
| | IWDG | Yes | | | | | | | | |
| | WWDG | Yes | | | | | | | | |
| | RTC | Yes | | | | | | | | |
| Random number generator | | Yes | | | | | | | | |



Table 2. STM32F405xx and STM32F407xx: features and peripheral counts (continued)

| Peripherals | | STM32F405RG | STM32F405OG | STM32F405VG | STM32F405ZG | STM32F405OE | STM32F407Vx | STM32F407Zx | STM32F407Ix |
|--------------------------|--|----------------------------------|-------------|-------------|-------------|-------------|-------------|---------------------|-------------|
| Communication interfaces | SPI / I2S | 3/2 (full duplex) ⁽²⁾ | | | | | | | |
| | I ² C | 3 | | | | | | | |
| | USART/ UART | 4/2 | | | | | | | |
| | USB OTG FS | Yes | | | | | | | |
| | USB OTG HS | Yes | | | | | | | |
| | CAN | 2 | | | | | | | |
| | SDIO | Yes | | | | | | | |
| Camera interface | No | | | | | Yes | | | |
| GPIOs | 51 | 72 | 82 | 114 | 72 | 82 | 114 | 140 | |
| 12-bit ADC | 3 | | | | | | | | |
| Number of channels | 16 | 13 | 16 | 24 | 13 | 16 | 24 | 24 | |
| 12-bit DAC | Yes | | | | | | | | |
| Number of channels | 2 | | | | | | | | |
| Maximum CPU frequency | 168 MHz | | | | | | | | |
| Operating voltage | 1.8 to 3.6 V ⁽³⁾ | | | | | | | | |
| Operating temperatures | Ambient temperatures: -40 to +85 °C / -40 to +105 °C | | | | | | | | |
| | Junction temperature: -40 to + 125 °C | | | | | | | | |
| Package | LQFP64 | WLCSP90 | LQFP100 | LQFP144 | WLCSP90 | LQFP100 | LQFP144 | UFBGA176 LQFP176 | |

1. For the LQFP100 and WLCSP90 packages, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I²S audio mode.
3. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to [Section : Internal reset OFF](#)).

2.1 Full compatibility throughout the family

The STM32F405xx and STM32F407xx are part of the STM32F4 family. They are fully pin-to-pin, software and feature compatible with the STM32F2xx devices, allowing the user to try different memory densities, peripherals, and performances (FPU, higher frequency) for a greater degree of freedom during the development cycle.

The STM32F405xx and STM32F407xx devices maintain a close compatibility with the whole STM32F10xxx family. All functional pins are pin-to-pin compatible. The STM32F405xx and STM32F407xx, however, are not drop-in replacements for the STM32F10xxx devices: the two families do not have the same power scheme, and so their power pins are different. Nonetheless, transition from the STM32F10xxx to the STM32F40xxx family remains simple as only a few pins are impacted.

[Figure 4](#), [Figure 3](#), [Figure 2](#), and [Figure 1](#) give compatible board designs between the STM32F40xxx, STM32F2, and STM32F10xxx families.

Figure 1. Compatible board design between STM32F10xx/STM32F40xx for LQFP64

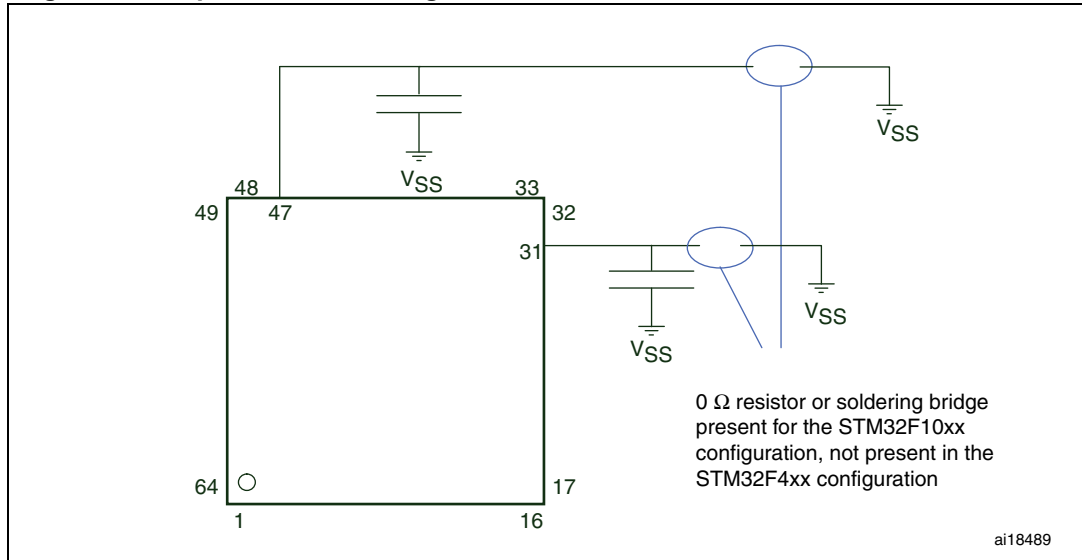


Figure 2. Compatible board design STM32F10xx/STM32F2/STM32F40xxx for LQFP100 package

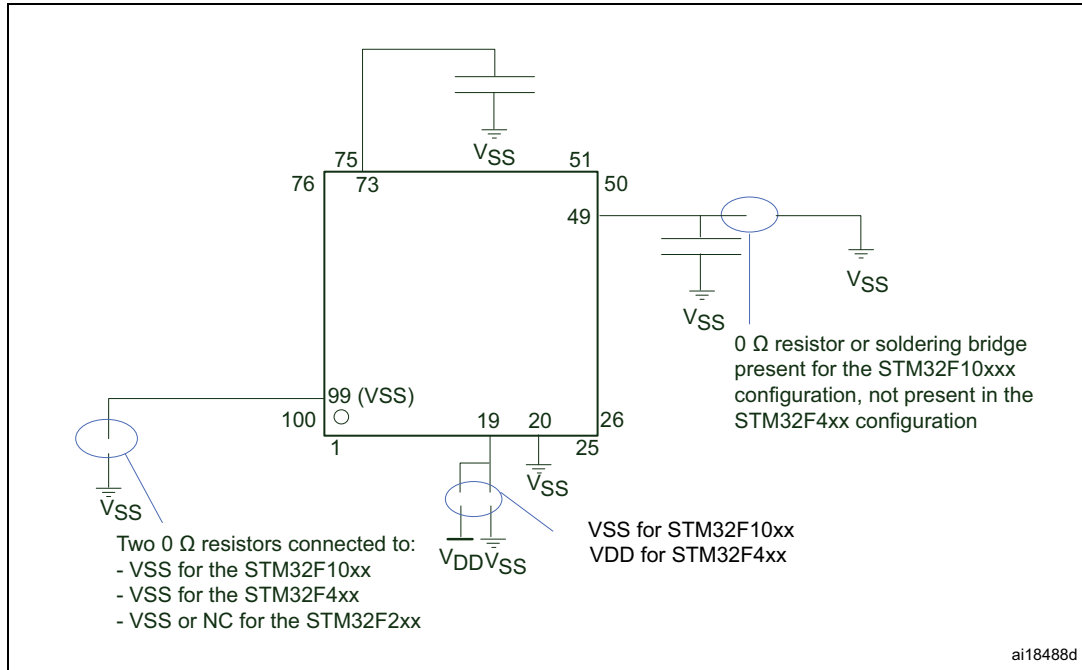


Figure 3. Compatible board design between STM32F10xx/STM32F2/STM32F40xxx for LQFP144 package

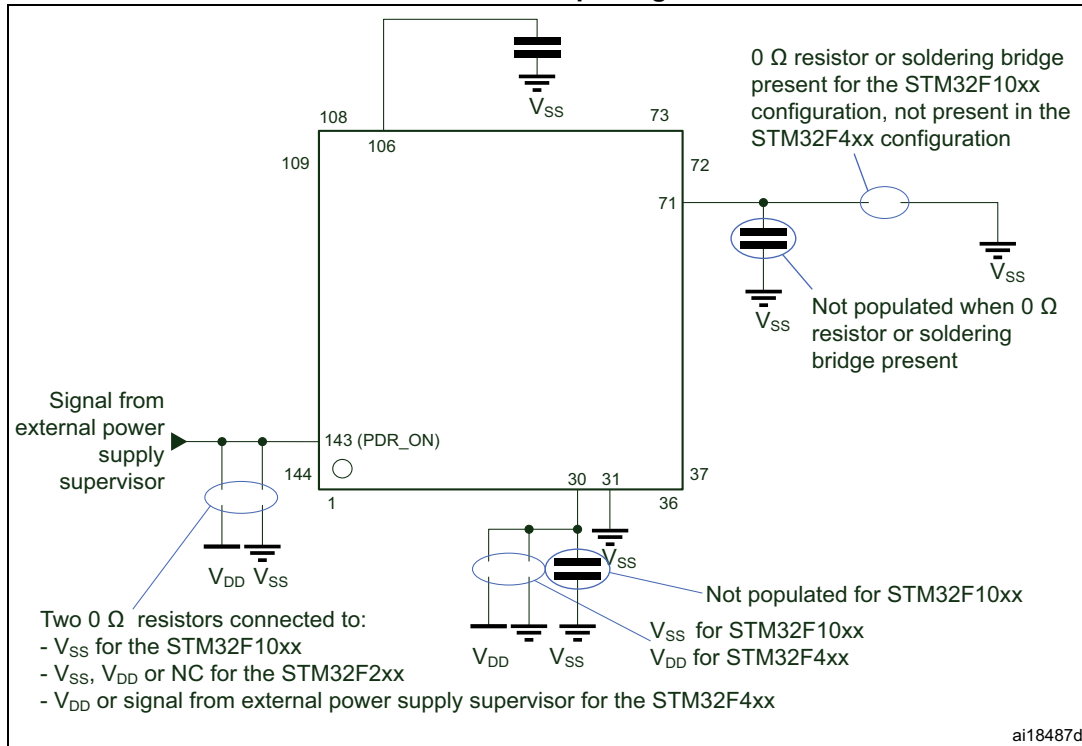
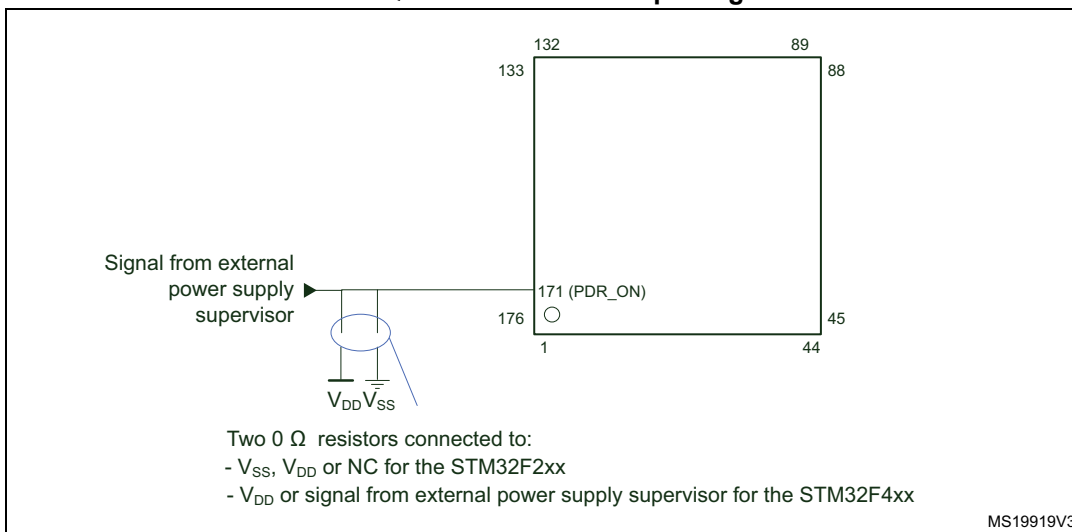
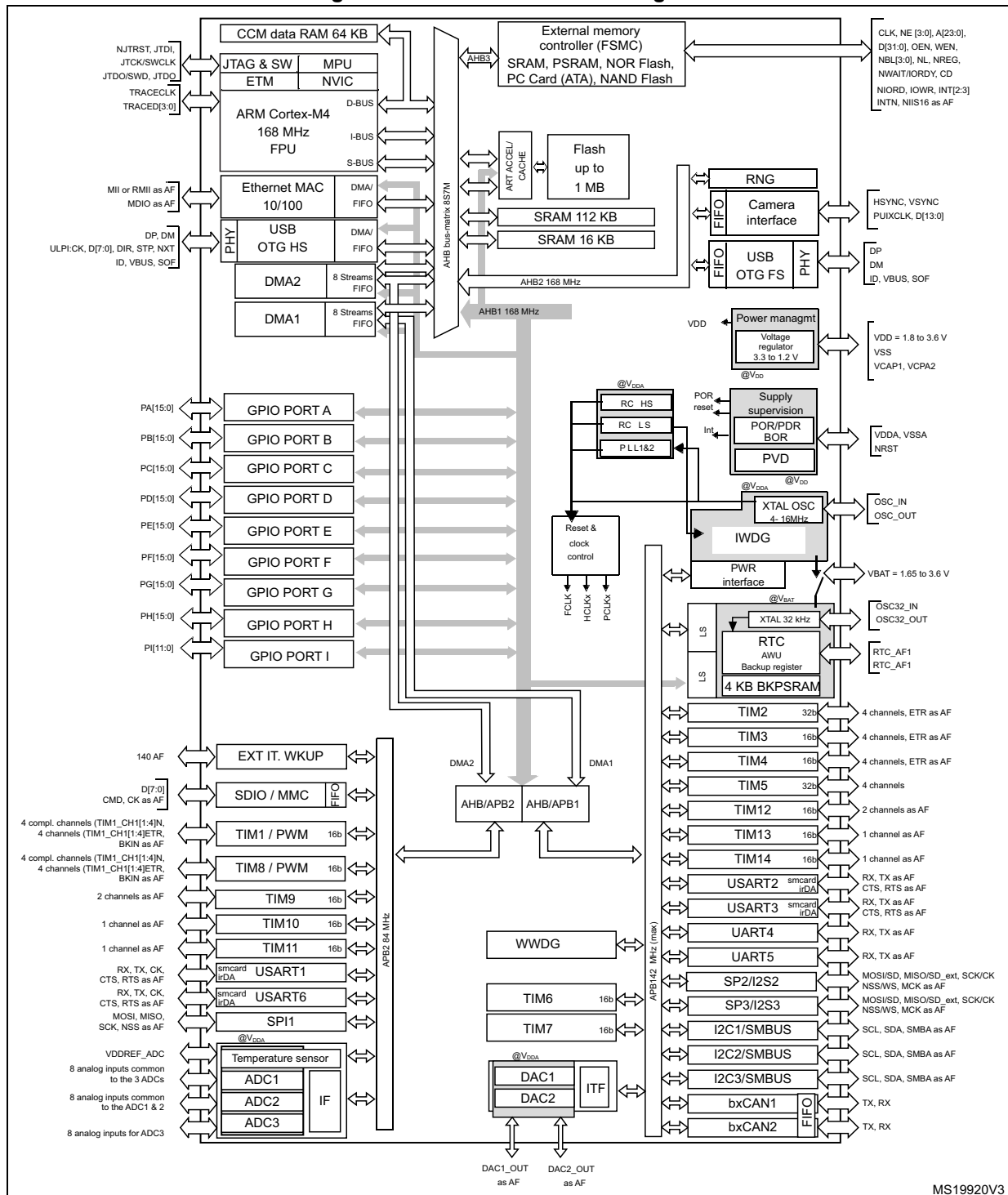


Figure 4. Compatible board design between STM32F2 and STM32F40xxx for LQFP176 and BGA176 packages



2.2 Device overview

Figure 5. STM32F40xxx block diagram



1. The camera interface and ethernet are available only on STM32F407xx devices.



2.2.1 ARM[®] Cortex[®]-M4 core with FPU and embedded Flash and SRAM

The ARM Cortex-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M4 32-bit RISC processor with FPU features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F405xx and STM32F407xx family is compatible with all ARM tools and software.

Figure 5 shows the general block diagram of the STM32F40xxx family.

Note: Cortex-M4 with FPU is binary compatible with Cortex-M3.

2.2.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM[®] Cortex[®]-M4 with FPU processors. It balances the inherent performance advantage of the ARM Cortex-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 210 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 168 MHz.

2.2.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.2.4 Embedded Flash memory

The STM32F40xxx devices embed a Flash memory of 512 Kbytes or 1 Mbytes available for storing programs and data.

2.2.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.2.6 Embedded SRAM

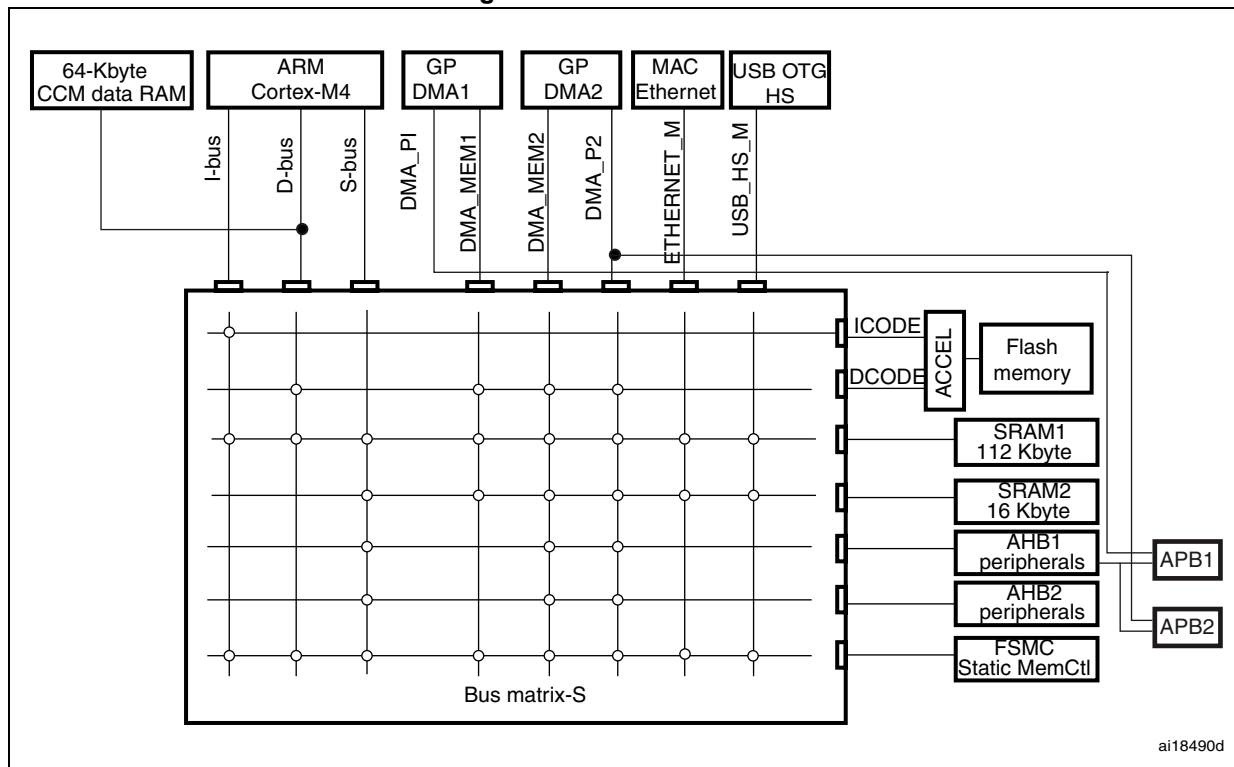
All STM32F40xxx products embed:

- Up to 192 Kbytes of system SRAM including 64 Kbytes of CCM (core coupled memory) data RAM
RAM memory is accessed (read/write) at CPU clock speed with 0 wait states.
- 4 Kbytes of backup SRAM
This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or VBAT mode.

2.2.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS) and the slaves (Flash memory, RAM, FSMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 6. Multi-AHB matrix



2.2.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I²S
- I²C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDIO
- Camera interface (DCMI)
- ADC.

2.2.9 Flexible static memory controller (FSMC)

The FSMC is embedded in the STM32F405xx and STM32F407xx family. It has four Chip Select outputs supporting the following modes: PCCard/Compact Flash, SRAM, PSRAM, NOR Flash and NAND Flash.

Functionality overview:

- Write FIFO
- Maximum FSMC_CLK frequency for synchronous accesses is 60 MHz.

LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

2.2.10 Nested vectored interrupt controller (NVIC)

The STM32F405xx and STM32F407xx embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 82 maskable interrupt channels plus the 16 interrupt lines of the Cortex[®]-M4 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

2.2.11 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 140 GPIOs can be connected to the 16 external interrupt lines.

2.2.12 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy over the full temperature range. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 168 MHz. Similarly, full interrupt management of the PLL

clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the three AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the three AHB buses is 168 MHz while the maximum frequency of the high-speed APB domains is 84 MHz. The maximum allowed frequency of the low-speed APB domain is 42 MHz.

The devices embed a dedicated PLL (PLL12S) which allows to achieve audio class performance. In this case, the I²S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

2.2.13 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART3 (PC10/PC11 or PB10/PB11), CAN2 (PB5/PB13), USB OTG FS in Device mode (PA11/PA12) through DFU (device firmware upgrade).

2.2.14 Power supply schemes

- $V_{DD} = 1.8$ to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins.
- V_{SSA} , $V_{DDA} = 1.8$ to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.
- $V_{BAT} = 1.65$ to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Refer to [Figure 21: Power supply scheme](#) for more details.

Note: V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to [Section : Internal reset OFF](#)).

Refer to [Table 2](#) in order to identify the packages supporting this option.

2.2.15 Power supply supervisor

Internal reset ON

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On all other packages, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default BOR threshold levels, or to disable BOR permanently. Three BOR thresholds are available through option bytes. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for an external reset circuit.

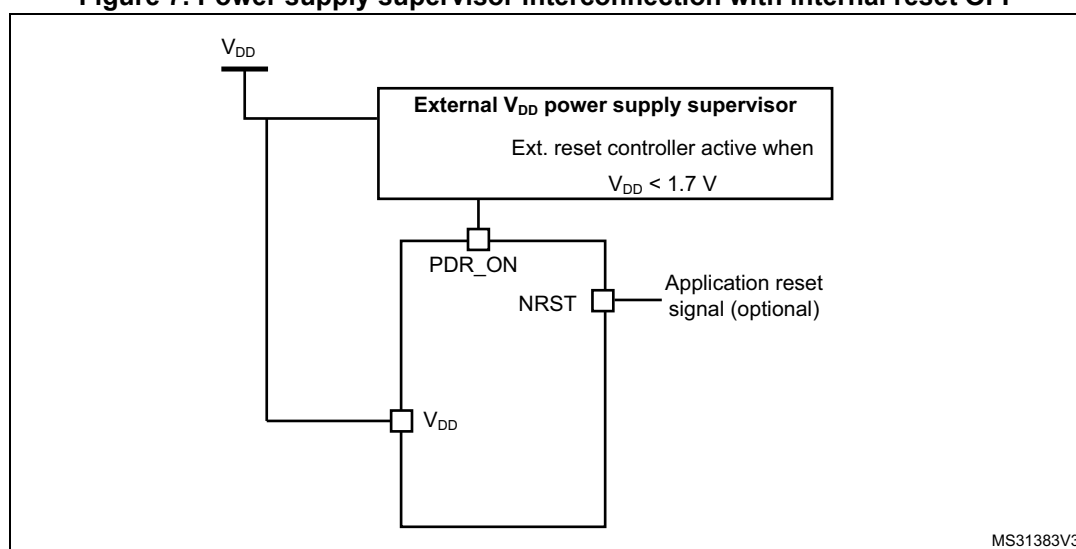
The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled with the PDR_ON pin.

An external power supply supervisor should monitor V_{DD} and should maintain the device in reset mode as long as V_{DD} is below a specified threshold. PDR_ON should be connected to this external power supply supervisor. Refer to [Figure 7: Power supply supervisor interconnection with internal reset OFF](#).

Figure 7. Power supply supervisor interconnection with internal reset OFF



1. PDR = 1.7 V for reduce temperature range; PDR = 1.8 V for all temperature range.

The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.8 V (see [Figure 7](#)). This supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range.

A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry is disabled
- The embedded programmable voltage detector (PVD) is disabled
- V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}

All packages, except for the LQFP64 and LQFP100, allow to disable the internal reset through the PDR_ON signal.