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STM32F070CB STM32F070RB STM32F070C6 STM32F070F6

ARM®-based 32-bit MCU, up to 128 KB Flash, USB FS 2.0, 11 timers, ADC, communication interfaces, 2.4 - 3.6 V

Datasheet - production data

Features

- Core: ARM® 32-bit Cortex®-M0 CPU, frequency up to 48 MHz
- Memories
  - 32 to 128 Kbytes of Flash memory
  - 6 to 16 Kbytes of SRAM with HW parity
- CRC calculation unit
- Reset and power management
  - Digital & I/Os supply: V_{DD} = 2.4 V to 3.6 V
  - Analog supply: V_{DDA} = V_{DD} to 3.6 V
  - Power-on/Power down reset (POR/PDR)
  - Low power modes: Sleep, Stop, Standby
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC with x6 PLL option
  - Internal 40 kHz RC oscillator
- Up to 51 fast I/Os
  - All mappable on external interrupt vectors
  - Up to 51 I/Os with 5V tolerant capability
- 5-channel DMA controller
- One 12-bit, 1.0 µs ADC (up to 16 channels)
  - Conversion range: 0 to 3.6 V
  - Separate analog supply: 2.4 V to 3.6 V
- Calendar RTC with alarm and periodic wakeup from Stop/Standby
- 11 timers
  - One 16-bit advanced-control timer for six-channel PWM output
  - Up to seven 16-bit timers, with up to four IC/OC, OCN, usable for IR control decoding
  - Independent and system watchdog timers
  - SysTick timer

LQFP64 10x10 mm
LQFP48 7x7 mm

TSSOP20

- Communication interfaces
  - Up to two I^2C interfaces
    - Fast Mode Plus (1 Mbit/s) support, with 20 mA current sink
    - SMBus/PMBus support (on single I/F)
  - Up to four USARTs supporting master synchronous SPI and modem control; one with auto baud rate detection
  - Up to two SPIs (18 Mbit/s) with 4 to 16 programmable bit frames
  - USB 2.0 full-speed interface with BCD and LPM support
- Serial wire debug (SWD)
- All packages ECOPACK®2

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F070CB/RB/C6/F6 microcontrollers.

This document should be read in conjunction with the STM32F0x0xx reference manual (RM0360). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M0 core, please refer to the Cortex®-M0 Technical Reference Manual, available from the www.arm.com website.

2 Description

The STM32F070CB/RB/C6/F6 microcontrollers incorporate the high-performance ARM® Cortex®-M0 32-bit RISC core operating at a 48 MHz frequency, high-speed embedded memories (up to 128 Kbytes of Flash memory and up to 16 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (up to two I^2Cs, up to two SPIs and up to four USARTs), one USB Full speed device, one 12-bit ADC, seven general-purpose 16-bit timers and an advanced-control PWM timer.

The STM32F070CB/RB/C6/F6 microcontrollers operate in the -40 to +85 °C temperature range from a 2.4 to 3.6V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

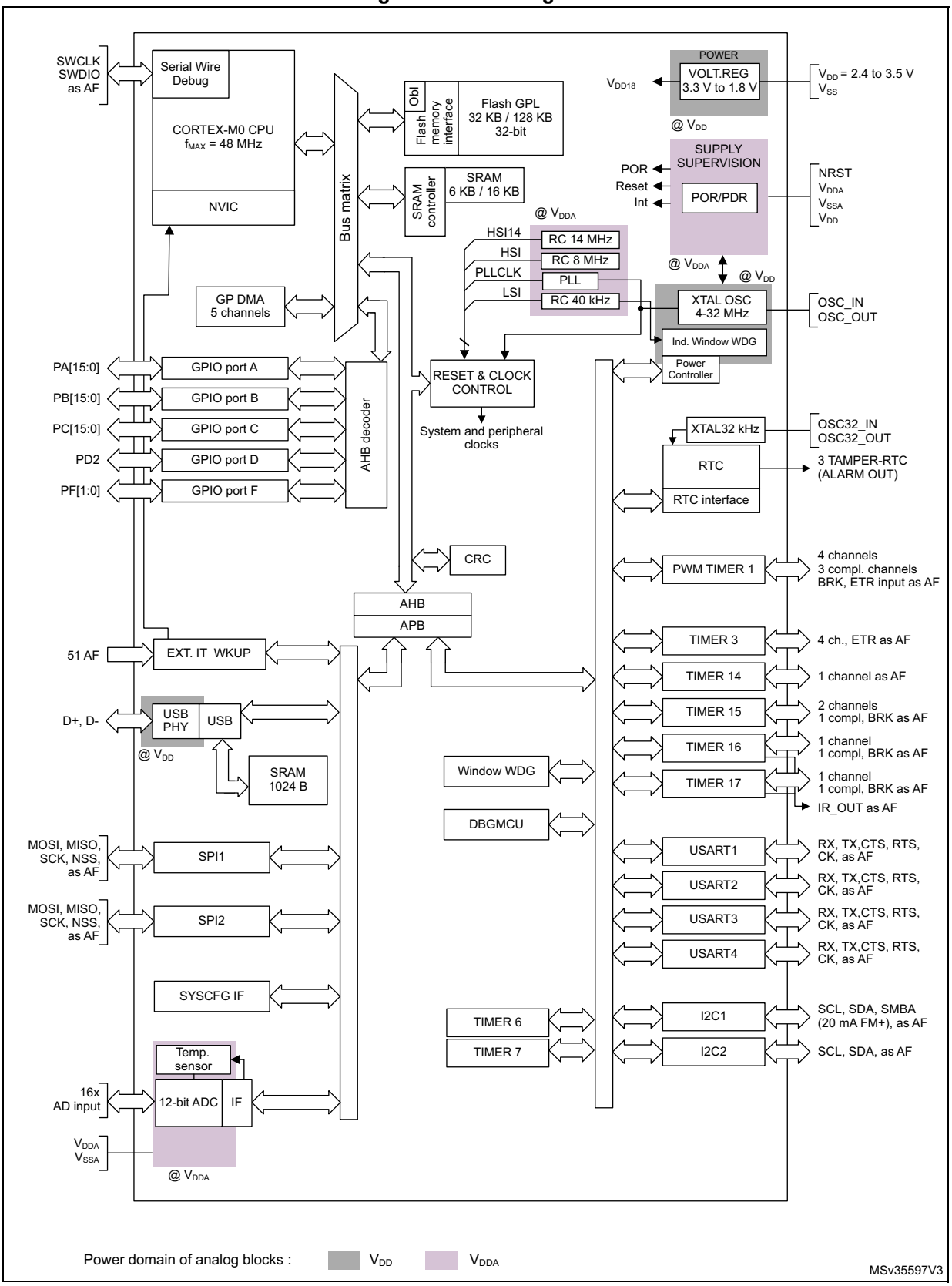
The STM32F070CB/RB/C6/F6 microcontrollers include devices in three different packages ranging from 20 pins to 64 pins. Depending on the device chosen, different sets of peripherals are included. The description below provides an overview of the complete range of STM32F070CB/RB/C6/F6 peripherals proposed.

These features make the STM32F070CB/RB/C6/F6 microcontrollers suitable for a wide range of applications such as application control and user interfaces, handheld equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

Table 1. STM32F070CB/RB/C6/F6 family device features and peripheral counts

Peripheral		STM32F070F6	STM32F070C6	STM32F070CB	STM32F070RB
Flash (Kbytes)		32		128	
SRAM (Kbytes)		6		16	
Timers	Advanced control	1 (16-bit)			
	General purpose	4 (16-bit)		5 (16-bit)	
	Basic	-		2 (16-bit)	
Comm. interfaces	SPI	1		2	
	I^2C	1		2	
	USART	2		4	
	USB	1			
12-bit ADC (number of channels)		1 (9 ext. + 2 int.)	1 (10 ext. + 2 int.)	1 (10 ext. + 2 int.)	1 (16 ext. + 2 int.)
GPIOs		15	37	37	51
Max. CPU frequency		48 MHz			
Operating voltage		2.4 to 3.6 V			
Operating temperature		Ambient operating temperature: -40°C to 85°C Junction temperature: -40°C to 105°C			
Packages		TSSOP20	LQFP48	LQFP48	LQFP64

Figure 1. Block diagram



3 Functional overview

3.1 ARM®-Cortex®-M0 core with embedded Flash and SRAM

The ARM® Cortex®-M0 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M0 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F0xx family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

3.2 Memories

The device has the following features:

- 6 to 16 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
  - 32 to 128 Kbytes of embedded Flash memory for programs and data
  - Option bytes

  The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex®-M0 serial wire) and boot in RAM selection disabled

3.3 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART on pins PA14/PA15 or PA9/PA10.

3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.5 Power management

3.5.1 Power supply schemes

- V_{DD} = 2.4 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through VDD pins.
- V_{DDA} = from V_{DD} to 3.6 V: external analog power supply for ADC, Reset blocks, RCs and PLL. The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be provided first.

For more details on how to connect power pins, refer to *Figure 9: Power supply scheme*.

3.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

3.5.3 Voltage regulator

The regulator has two operating modes and it is always enabled after reset.

- Main (MR) is used in normal operating mode (Run).
- Low power (LPR) can be used in Stop mode where the power demand is reduced.

In Standby mode, it is put in power down mode. In this mode, the regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

3.5.4 Low-power modes

The STM32F070CB/RB/C6/F6 microcontrollers support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

  The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines and RTC.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the RTC domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC event occurs.

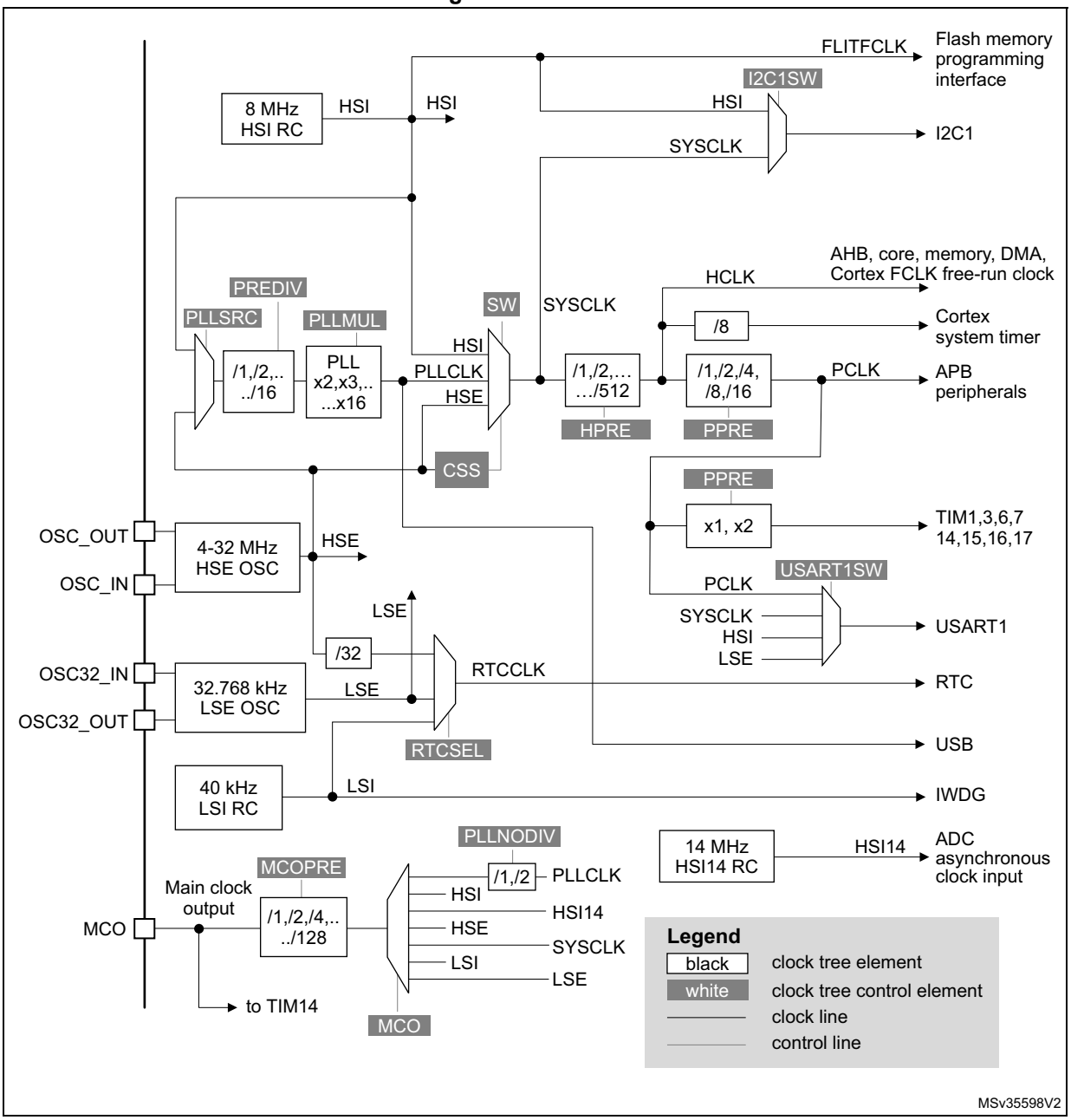
Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

Figure 2. Clock tree



3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.8 Direct memory access controller (DMA)

The 5-channel general-purpose DMA manages memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I2C, USART, all TIMx timers (except TIM14) and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F0xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 32 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 51 GPIOs can be connected to the 16 external interrupt lines.

3.10 Analog to digital converter (ADC)

The 12-bit analog to digital converter has up to 16 external and two internal (temperature sensor, voltage reference measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 2. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), V_{DDA}= 3.3 V (± 10 mV)	0x1FFF F7B8 - 0x1FFF F7B9

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 3. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at a temperature of 30 °C (± 5 °C), V_{DDA}= 3.3 V (± 10 mV)	0x1FFF F7BA - 0x1FFF F7BB

3.11 Timers and watchdogs

The STM32F070CB/RB/C6/F6 devices include up to five general-purpose timers, two basic timers and one advanced control timer.

Table 4 compares the features of the different timers.

Table 4. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	3
General purpose	TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	-
	TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	-
	TIM15(1)	16-bit	Up	Any integer between 1 and 65536	Yes	2	-
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6,(1) TIM7(1)	16-bit	Up	Any integer between 1 and 65536	Yes	0	-

1. Not available on STM32F070x6 devices.

3.11.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

3.11.2 General-purpose timers (TIM3, TIM14..17)

There are five synchronizable general-purpose timers embedded in the STM32F070CB/RB/C6/F6 devices (see *Table 4* for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM3

STM32F070CB/RB/C6/F6 devices feature one synchronizable 4-channel general-purpose timer. TIM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. It features four independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM3 general-purpose timer can work with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM3 has an independent DMA request generation.

This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

The counter can be frozen in debug mode.

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate withTIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16 and TIM17 have a complementary output with dead-time generation and independent DMA request generation.

Their counters can be frozen in debug mode.

3.11.3 Basic timers TIM6 and TIM7

These timers can be used as a generic 16-bit time base.

3.11.4 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It

can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.11.5 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.11.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source (HCLK or HCLK/8)

3.12 Real-time clock (RTC)

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 day of the month.
- Programmable alarm with wake up from Stop and Standby mode capability.
- Periodic wakeup unit with programmable resolution and period.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Tow anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32

3.13 Inter-integrated circuit interfaces (I^2C)

Up to two I2C interfaces (I2C1 and I2C2) can operate in multimaster or slave modes. Both can support Standard mode (up to 100 kbit/s) or Fast mode (up to 400 kbit/s). I2C1 also supports Fast Mode Plus (up to 1 Mbit/s), with 20 mA output drive.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). They also include programmable analog and digital noise filters.

Table 5. Comparison of I2C analog and digital filters

-	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	-

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management.

The I2C interfaces can be served by the DMA controller.

Refer to *Table 6* for the differences between I2C1 and I2C2.

Table 6. STM32F070CB/RB/C6/F6 I^2C implementation(1)

I2C features	I2C1	I2C2(2)
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus (up to 1 Mbit/s), with 20mA output drive I/Os	X	-
Independent clock	X	-
SMBus	X	-
Wakeup from STOP	-	-

1. X = supported.
2. Only available on STM32F070xB devices.

3.14 Universal synchronous/asynchronous receiver/transmitter (USART)

The device embeds up to four universal synchronous/asynchronous receivers/transmitters that communicate at speeds of up to 6 Mbit/s.

Table 7 gives an overview of features as implemented on the available USART interfaces. All USART interfaces can be served by the DMA controller.

Table 7. STM32F70x0 USART implementation(1)

USART modes/ features	STM32F070x6		STM32F070xB		
	USART1	USART2	USART1 USART2	USART3	USART4
Hardware flow control for modem	X	X	X	X	X
Continuous communication using DMA	X	X	X	X	-
Multiprocessor communication	X	X	X	X	X
Synchronous mode	X	X	X	X	X
Smartcard mode	-	-	-	-	-
Single-wire Half-duplex communication	X	X	X	X	X
IrDA SIR ENDEC block	-	-	-	-	-
LIN mode	-	-	-	-	-
Dual clock domain and wakeup from Stop mode	-	-	-	-	-
Receiver timeout interrupt	X	-	X	-	-
Modbus communication	-	-	-	-	-
Auto baud rate detection (supported modes)	4	-	4	-	-
Driver Enable	X	X	X	X	X
USART data length	7, 8 and 9 bits				

1. **X = supported.**

3.15 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

SPI1 and SPI2 are identical and implement the set of features shown in the following table.

Table 8. STM32F070CB/RB/C6/F6 SPI implementation(1)

SPI features	SPI1	SPI2(2)
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
TI mode	X	X

1. X = supported.
2. Available on STM32F070xB only.

3.16 Universal serial bus (USB)

The STM32F070CB/RB/C6/F6 embeds a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 KB and suspend/resume support. It requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use an HSE crystal oscillator).

3.17 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

4 Pinouts and pin descriptions

Figure 3. LQFP64 64-pin package pinout (top view)

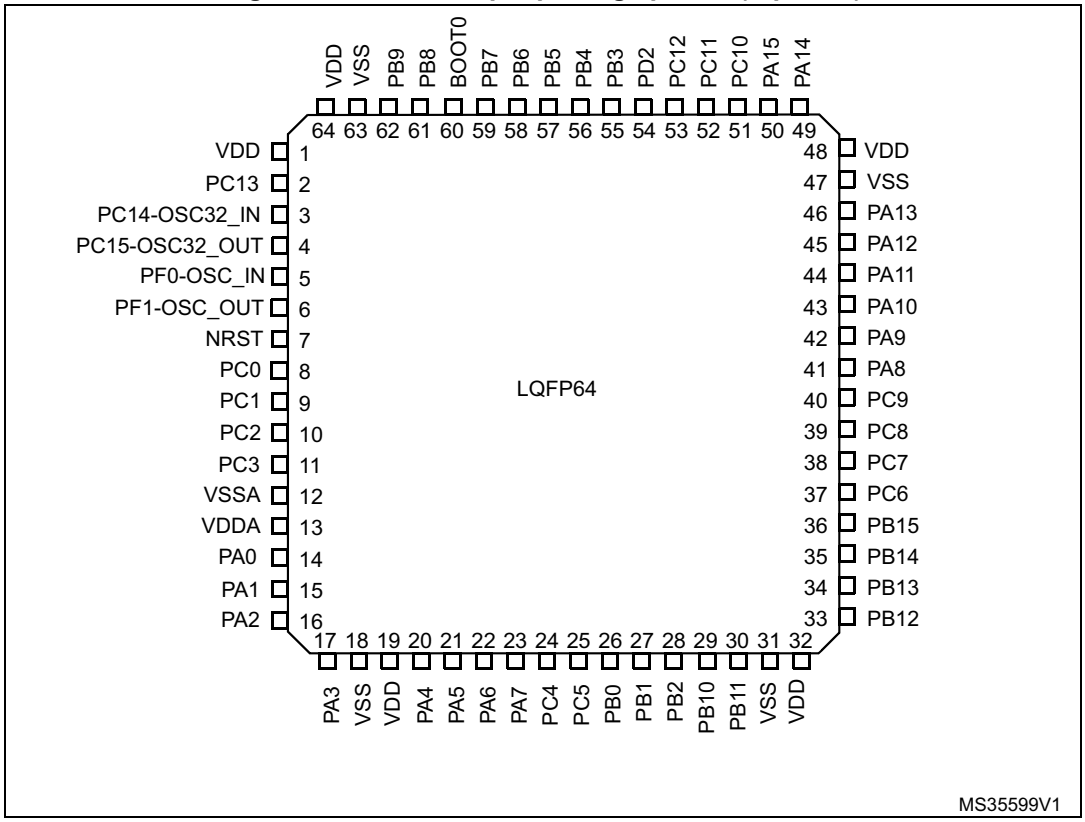


Figure 4. LQFP48 48-pin package pinout (top view)

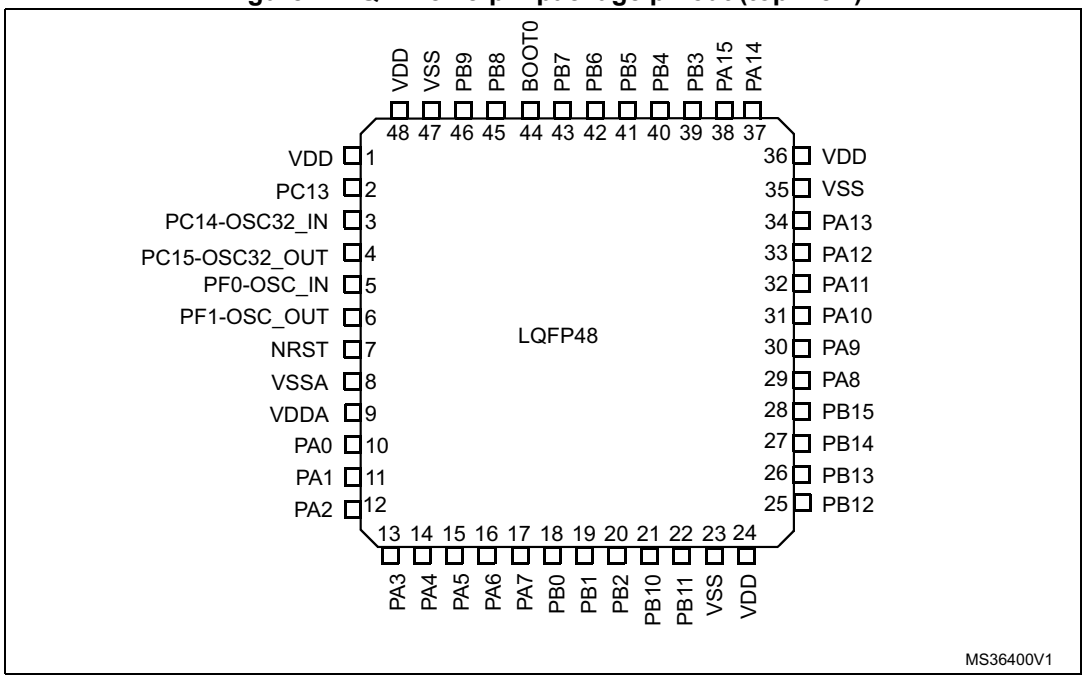


Figure 5. TSSOP20 20-pin package pinout (top view)

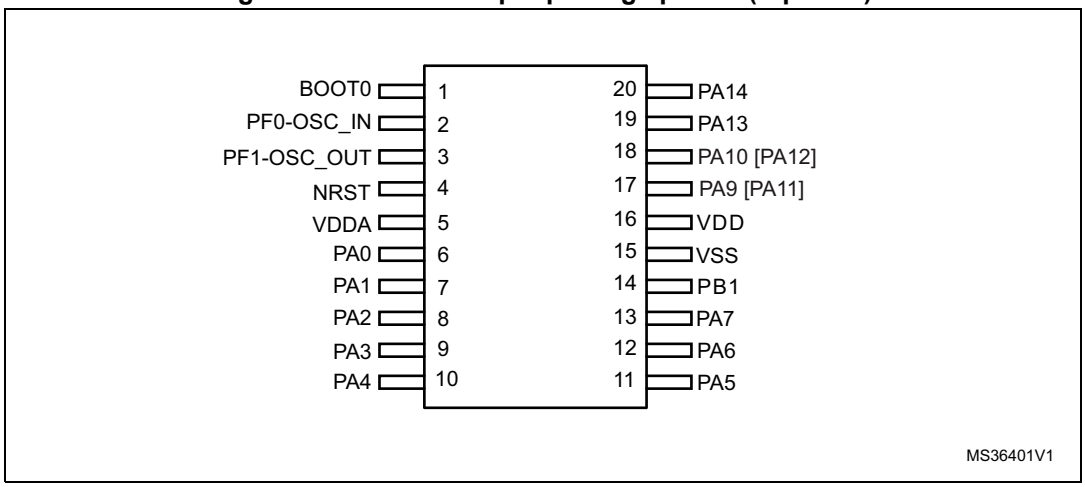


Table 9. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TC	Standard 3.3 V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	