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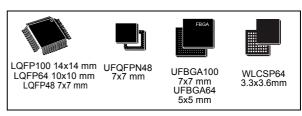
STM32F091xB STM32F091xC

ARM®-based 32-bit MCU, up to 256 KB Flash, CAN, 12 timers, ADC, DAC, and comm. interfaces, 2.0 - 3.6V

Datasheet - production data

Features

- Core: ARM[®] 32-bit Cortex[®]-M0 CPU, frequency up to 48 MHz
- Memories
 - 128 to 256 Kbytes of Flash memory
 - 32 Kbytes of SRAM with HW parity
- CRC calculation unit
- Reset and power management
 - Digital & I/Os supply: V_{DD} = 2.0 V to 3.6 V
 - Analog supply: V_{DDA} = V_{DD} to 3.6 V
 - Power-on/Power down reset (POR/PDR)
 - Programmable voltage detector (PVD)
 - Low power modes: Sleep, Stop, Standby
 - V_{BAT} supply for RTC and backup registers
- Clock management
 - 4 to 32 MHz crystal oscillator
 - 32 kHz oscillator for RTC with calibration
 - Internal 8 MHz RC with x6 PLL option
 - Internal 40 kHz RC oscillator
 - Internal 48 MHz oscillator with automatic trimming based on ext. synchronization
- Up to 88 fast I/Os
 - All mappable on external interrupt vectors
 - $-\,$ Up to 69 I/Os with 5V-tolerant capability and 19 with independent supply $\rm V_{DDIO2}$
- 12-channel DMA controller
- One 12-bit, 1.0 µs ADC (up to 16 channels)
 - Conversion range: 0 to 3.6 V
 - Separate analog supply: 2.4 V to 3.6 V
- One 12-bit D/A converter (with 2 channels)
- Two fast low-power analog comparators with programmable input and output
- Up to 24 capacitive sensing channels for touchkey, linear and rotary touch sensors
- Calendar RTC with alarm and periodic wakeup from Stop/Standby



12 timers

- One 16-bit advanced-control timer for 6 channel PWM output
- One 32-bit and seven 16-bit timers, with up to 4 IC/OC, OCN, usable for IR control decoding or DAC control
- Independent and system watchdog timers
- SysTick timer
- Communication interfaces
 - Two I²C interfaces supporting Fast Mode Plus (1 Mbit/s) with 20 mA current sink, one supporting SMBus/PMBus and wakeup
 - Up to eight USARTs supporting master synchronous SPI and modem control, three with ISO7816 interface, LIN, IrDA, auto baud rate detection and wakeup feature
 - Two SPIs (18 Mbit/s) with 4 to 16 programmable bit frames, and with I²S interface multiplexed
 - CAN interface
- HDMI CEC wakeup on header reception
- Serial wire debug (SWD)
- 96-bit unique ID
- All packages ECOPACK[®]2

Table 1. Device summary

	,
Reference	Part number
STM32F091xB	STM32F091CB, STM32F091RB, STM32F091VB
STM32F091xC	STM32F091CC, STM32F091RC, STM32F091VC

Contents

1	Intro	duction		9
2	Desc	ription .		10
3	Fund	tional o	verview	13
	3.1	ARM®-0	Cortex [®] -M0 core	13
	3.2	Memori	es	13
	3.3	Boot mo	odes	13
	3.4	Cyclic r	edundancy check calculation unit (CRC)	14
	3.5	Power r	management	14
		3.5.1	Power supply schemes	14
		3.5.2	Power supply supervisors	14
		3.5.3	Voltage regulator	15
		3.5.4	Low-power modes	15
	3.6	Clocks	and startup	15
	3.7	Genera	I-purpose inputs/outputs (GPIOs)	17
	3.8	Direct n	nemory access controller (DMA)	17
	3.9	Interrup	ots and events	17
		3.9.1	Nested vectored interrupt controller (NVIC)	17
		3.9.2	Extended interrupt/event controller (EXTI)	18
	3.10	Analog-	to-digital converter (ADC)	18
		3.10.1	Temperature sensor	18
		3.10.2	Internal voltage reference (V _{REFINT})	18
		3.10.3	V _{BAT} battery voltage monitoring	19
	3.11	Digital-t	co-analog converter (DAC)	19
	3.12	Compa	rators (COMP)	19
	3.13	Touch s	sensing controller (TSC)	20
	3.14	Timers	and watchdogs	21
		3.14.1	Advanced-control timer (TIM1)	22
		3.14.2	General-purpose timers (TIM2, 3, 14, 15, 16, 17)	22
		3.14.3	Basic timers TIM6 and TIM7	23
		3.14.4	Independent watchdog (IWDG)	23
		3.14.5	System window watchdog (WWDG)	23



		3.14.6	SysTick timer	3
	3.15	Real-tim	ne clock (RTC) and backup registers	3
	3.16	Inter-inte	egrated circuit interface (I ² C)	4
	3.17	Universa	al synchronous/asynchronous receiver/transmitter (USART) 2	5
	3.18		eripheral interface (SPI) / Inter-integrated sound interface (I ² S) 20	
	3.19	•	finition multimedia interface (HDMI) - consumer ics control (CEC)	7
	3.20	Controll	er area network (CAN)	7
	3.21	Clock re	covery system (CRS)2	7
	3.22	Serial w	ire debug port (SW-DP)	7
4	Pinou	ıts and ı	oin descriptions 28	8
5	Memo	ory map	ping	5
6	Electi	rical cha	aracteristics 49	9
	6.1	Parame	ter conditions	9
		6.1.1	Minimum and maximum values	9
		6.1.2	Typical values	9
		6.1.3	Typical curves	9
		6.1.4	Loading capacitor	9
		6.1.5	Pin input voltage	9
		6.1.6	Power supply scheme	0
		6.1.7	Current consumption measurement5	1
	6.2	Absolute	e maximum ratings	2
	6.3	Operatir	ng conditions 54	4
		6.3.1	General operating conditions	4
		6.3.2	Operating conditions at power-up / power-down 5-	4
		6.3.3	Embedded reset and power control block characteristics	5
		6.3.4	Embedded reference voltage	6
		6.3.5	Supply current characteristics	6
		6.3.6	Wakeup time from low-power mode6	7
		6.3.7	External clock source characteristics 6	7
		6.3.8	Internal clock source characteristics	1
		6.3.9	PLL characteristics	5
		6.3.10	Memory characteristics	5

		6.3.11	EMC characteristics
		6.3.12	Electrical sensitivity characteristics
		6.3.13	I/O current injection characteristics
		6.3.14	I/O port characteristics
		6.3.15	NRST pin characteristics
		6.3.16	12-bit ADC characteristics
		6.3.17	DAC electrical specifications
		6.3.18	Comparator characteristics
		6.3.19	Temperature sensor characteristics
		6.3.20	V _{BAT} monitoring characteristics
		6.3.21	Timer characteristics
		6.3.22	Communication interfaces
7	Pack	cage info	ormation
	7.1	UFBGA	A100 package information
	7.2	LQFP1	00 package information
	7.3	UFBGA	A64 package information
	7.4	WLCSI	P64 package information
	7.5	LQFP6	4 package information
	7.6	LQFP4	.8 package information
	7.7	UFQFF	PN48 package information
	7.8	Therma	al characteristics
		7.8.1	Reference document
		7.8.2	Selecting the product temperature range121
8	Orde	ering inf	ormation 124
9	Revi	sion his	story

List of tables

Table 1.	Device summary	1
Table 2.	STM32F091xB/xC family device features and peripheral counts	
Table 3.	Temperature sensor calibration values	
Table 4.	Internal voltage reference calibration values	
Table 5.	Capacitive sensing GPIOs available on STM32F091xB/xC devices	
Table 6.	Number of capacitive sensing channels available	
	on STM32F091xB/xC devices	21
Table 7.	Timer feature comparison	21
Table 8.	Comparison of I ² C analog and digital filters	
Table 9.	STM32F091xB/xC I ² C implementation	
Table 10.	STM32F091xB/xC USART implementation	
Table 11.	STM32F091xB/xC SPI/I ² S implementation	
Table 12.	Legend/abbreviations used in the pinout table	33
Table 13.	STM32F091xB/xC pin definitions	
Table 14.	Alternate functions selected through GPIOA_AFR registers for port A	41
Table 15.	Alternate functions selected through GPIOB_AFR registers for port B	
Table 16.	Alternate functions selected through GPIOC_AFR registers for port C	
Table 17.	Alternate functions selected through GPIOD_AFR registers for port D	
Table 18.	Alternate functions selected through GPIOE_AFR registers for port E	
Table 19.	Alternate functions selected through GPIOF_AFR registers for port F	
Table 20.	STM32F091xB/xC peripheral register boundary addresses	
Table 21.	Voltage characteristics	
Table 22.	Current characteristics	53
Table 23.	Thermal characteristics	53
Table 24.	General operating conditions	54
Table 25.	Operating conditions at power-up / power-down	55
Table 26.	Embedded reset and power control block characteristics	55
Table 27.	Programmable voltage detector characteristics	55
Table 28.	Embedded internal reference voltage	56
Table 29.	Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6 V	58
Table 30.	Typical and maximum current consumption from the V _{DDA} supply	59
Table 31.	Typical and maximum consumption in Stop and Standby modes	60
Table 32.	Typical and maximum current consumption from the V _{BAT} supply	61
Table 33.	Typical current consumption, code executing from Flash memory,	
	running from HSE 8 MHz crystal	
Table 34.	Switching output I/O current consumption	64
Table 35.	Peripheral current consumption	
Table 36.	Low-power mode wakeup timings	67
Table 37.	High-speed external user clock characteristics	67
Table 38.	Low-speed external user clock characteristics	
Table 39.	HSE oscillator characteristics	69
Table 40.	LSE oscillator characteristics (f _{LSE} = 32.768 kHz)	70
Table 41.	HSI oscillator characteristics	
Table 42.	HSI14 oscillator characteristics	
Table 43.	HSI48 oscillator characteristics	
Table 44.	LSI oscillator characteristics	
Table 45.	PLL characteristics	
Table 46.	Flash memory characteristics	75



List of tables

Table 47.	Flash memory endurance and data retention
Table 48.	EMS characteristics
Table 49.	EMI characteristics
Table 50.	ESD absolute maximum ratings
Table 51.	Electrical sensitivities
Table 52.	I/O current injection susceptibility
Table 53.	I/O static characteristics
Table 54.	Output voltage characteristics
Table 55.	I/O AC characteristics
Table 56.	NRST pin characteristics
Table 57.	ADC characteristics
Table 58.	R _{AIN} max for f _{ADC} = 14 MHz
Table 59.	ADC accuracy87
Table 60.	DAC characteristics
Table 61.	Comparator characteristics91
Table 62.	TS characteristics
Table 63.	V _{BAT} monitoring characteristics
Table 64.	TIMx characteristics
Table 65.	IWDG min/max timeout period at 40 kHz (LSI)94
Table 66.	WWDG min/max timeout value at 48 MHz (PCLK)
Table 67.	I ² C analog filter characteristics
Table 68.	SPI characteristics
Table 69.	I ² S characteristics97
Table 70.	UFBGA100 package mechanical data
Table 71.	UFBGA100 recommended PCB design rules
Table 72.	LQPF100 package mechanical data103
Table 73.	UFBGA64 package mechanical data
Table 74.	UFBGA64 recommended PCB design rules
Table 75.	WLCSP64 package mechanical data
Table 76.	WLCSP64 recommended PCB design rules
Table 77.	LQFP64 package mechanical data112
Table 78.	LQFP48 package mechanical data116
Table 79.	UFQFPN48 package mechanical data
Table 80.	Package thermal characteristics
Table 81.	Ordering information scheme
Table 82.	Document revision history



List of figures

Figure 1.	Block diagram	. 12
Figure 2.	Clock tree	
Figure 3.	UFBGA100 package pinout	
Figure 4.	LQFP100 package pinout	
Figure 5.	UFBGA64 package pinout	
Figure 6.	LQFP64 package pinout	
Figure 7.	WLCSP64 package pinout	
Figure 8.	LQFP48 package pinout	
Figure 9.	UFQFPN48 package pinout	
Figure 10.	STM32F091xC memory map	
Figure 11.	Pin loading conditions	
Figure 12.	Pin input voltage	
Figure 13.	Power supply scheme.	
Figure 14.	Current consumption measurement scheme	
Figure 15.	High-speed external clock source AC timing diagram	
Figure 16.	Low-speed external clock source AC timing diagram	
Figure 17.	Typical application with an 8 MHz crystal	
Figure 18.	Typical application with a 32.768 kHz crystal	
Figure 19.	HSI oscillator accuracy characterization results for soldered parts	
Figure 20.	HSI14 oscillator accuracy characterization results	
Figure 21.	HSI48 oscillator accuracy characterization results	
Figure 22.	TC and TTa I/O input characteristics	
Figure 23.	Five volt tolerant (FT and FTf) I/O input characteristics	
Figure 24.	I/O AC characteristics definition	
Figure 25.	Recommended NRST pin protection	
Figure 26.	ADC accuracy characteristics	
Figure 27.	Typical connection diagram using the ADC	
Figure 28.	SPI timing diagram - slave mode and CPHA = 0	
Figure 29.	SPI timing diagram - slave mode and CPHA = 1	
Figure 30.	SPI timing diagram - master mode	
Figure 31.	I ² S slave timing diagram (Philips protocol)	
Figure 32.	I ² S master timing diagram (Philips protocol)	
Figure 33.	UFBGA100 package outline	
Figure 34.	Recommended footprint for UFBGA100 package	
Figure 35.	UFBGA100 package marking example	
Figure 36.	LQFP100 package outline	
Figure 37.	Recommended footprint for LQFP100 package	
Figure 38.	LQFP100 package marking example	
Figure 39.	UFBGA64 package outline	
Figure 40.	Recommended footprint for UFBGA64 package	
Figure 41.	UFBGA64 package marking example	
Figure 42.	WLCSP64 package outline	
Figure 43.	Recommended footprint for WLCSP64 package	
Figure 44.	WLCSP64 package marking example	
Figure 45.	LQFP64 package outline	
Figure 46.	Recommended footprint for LQFP64 package	113
Figure 47.	LQFP64 package marking example	
Figure 48.	LQFP48 package outline	
.gai 0 TO.		



List of figures

STM32F091xB STM32F091xC

Figure 49.	Recommended footprint for LQFP48 package	116
Figure 50.	LQFP48 package marking example	117
Figure 51.	UFQFPN48 package outline	118
Figure 52.	Recommended footprint for UFQFPN48 package	119
Figure 53.	UFQFPN48 package marking example	120
Figure 54.	LQFP64 P _D max versus T _A	123



1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F091xB/xC microcontrollers.

This document should be read in conjunction with the STM32F0xxxx reference manual (RM0091). The reference manual is available from the STMicroelectronics website www.st.com.

For information on the ARM[®] Cortex[®]-M0 core, please refer to the Cortex[®]-M0 Technical Reference Manual, available from the www.arm.com website.





2 Description

The STM32F091xB/xC microcontrollers incorporate the high-performance ARM® Cortex®-M0 32-bit RISC core operating at up to 48 MHz frequency, high-speed embedded memories (up to 256 Kbytes of Flash memory and 32 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. The device offers standard communication interfaces (two I²Cs, two SPIs/one I²S, one HDMI CEC and up to eight USARTs), one CAN, one 12-bit ADC, one 12-bit DAC with two channels, seven 16-bit timers, one 32-bit timer and an advanced-control PWM timer.

The STM32F091xB/xC microcontrollers operate in the -40 to +85 °C and -40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F091xB/xC microcontrollers include devices in seven different packages ranging from 48 pins to 100 pins with a die form also available upon request. Depending on the device chosen, different sets of peripherals are included.

These features make the STM32F091xB/xC microcontrollers suitable for a wide range of applications such as application control and user interfaces, hand-held equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms and HVACs.

577

Table 2. STM32F091xB/xC family device features and peripheral counts

Peripheral		STM32	F091Cx	STM32	2F091Rx	STM32	PF091Vx	
Flash mem	nory (Kbyte)	128	256	128	256	128	256	
SRAM	(Kbyte)		32					
	Advanced control		1 (16-bit)					
Timers	General purpose		5 (16-bit) 1 (32-bit)					
	Basic			2	(16-bit)			
	SPI [I ² S] ⁽¹⁾				2 [2]			
	I ² C				2			
Comm. interfaces	USART	(3			8		
mionacco	CAN	1						
	CEC		1					
	t ADC f channels)	1 1 (10 ext. + 3 int.) (16 ext. + 3 int.)						
	t DAC f channels)	1 (2)						
Analog co	omparator	2						
GP	lOs	3	8		52	3	38	
	re sensing nnels	17		18 24		24		
Max. CPU	frequency		48 MHz					
Operatin	g voltage	2.0 to 3.6 V						
Operating temperature Packages		Ambient operating temperature: -40°C to 85°C / -40°C to 105°C Junction temperature: -40°C to 105°C / -40°C to 125°C				5°C		
		LQF UFQF	P48 PN48	UFB	FP64 GA64 CSP64		P100 GA100	

^{1.} The SPI interface can be used either in SPI mode or in I²S audio mode.

SWCLK SWDIO as AF POWER Serial Wire Debug VOLT.REG $V_{DD} = 2 \text{ to } 3.6 \text{ V}$ 3.3 V to 1.8 V Obl Flash Or memory interface Flash GPL up to 256 KB 32-bit CORTEX-M0 CPU OKIN ← SUPPLY SUPERVISION $f_{MAX} = 48 \text{ MHz}$ V_{DDIO2} OKIN ◀ NRST SRAM 32 KB SRAM controller matri Reset ◀ V_{DDA} POR/PDR Int ◀ V_{SSA} NVIC @ V_{DDA} V_{DD} Bus HSI14 RC 14 MHz PVD HSI RC 8 MHz @ V_{DDA} PLLCLK @ V_{DD} LSI GP DMA RC 40 kHz XTAL OSC OSC_IN 12 channels HSI48 4-32 MHz RC 48MHz Ind. Window WDG PA[15:0] GPIO port A RESET & CLOCK ₹. CONTROL V_{BAT} = 1.65 to 3.6 V PB[15:0] GPIO port B OSC32_IN OSC32_OUT PC[15:0] GPIO port C System and peripheral XTAL32 kHz clocks PD[15:0] GPIO port D 3 TAMPER-RTC RTC AHB reg (ALARM OUT) PE[15:0] GPIO port E RTC interface PF[10:9], PF6 PF[3:0] Щ GPIO port F CRS SYNC 4 channels 3 compl. channels BRK, ETR input as AF PWM TIMER 1 CRC PAD 8 groups of 4 channels 4 ch., ETR as AF TIMER 2 32-bit Sensing Controller switches AHB TIMER 3 4 ch., ETR as AF SYNC APR TIMER 14 1 channel as AF EXT. IT WKUP 88 AF [2 channels 1 compl, BRK as AF TIMER 15 SRAM 1 channel 1 compl, BRK as AF 256 B TIMER 16 į į 1 channel 1 compl, BRK as AF IR_OUT as AF TIMER 17 TX, RX as AF **BxCAN** Window WDG RX, TX,CTS, RTS, CK as AF USART1 MOSI/SD SPI1/I2S1 MISO/MCK SCK/CK NSS/WS as AF RX, TX,CTS, RTS, CK as AF USART2 DBGMCU RX, TX,CTS, RTS, CK as AF USART3 MOSI/SD SPI2/I2S2 RX, TX,CTS, RTS, CK as AF USART4 SCK/CK NSS/WS as AF SYSCFG IF USART5 RX, TX, RTS, CK as AF USART6 RX, TX, RTS, CK as AF INPUT + GP comparator 1 USART7 RX, TX, RTS, CK as AF OUTPUT GP comparator 2 USART8 RX, TX, RTS, CK as AF as AF @ V_{DDA} SCL, SDA, SMBA (20 mA FM+) as AF I2C1 Temp. SCL, SDA (20 mA FM+) as AF I2C2 16x AD input IF 12-bit ADC CEC as AF HDMI-CEC TIMER 6 12-bit DAC ►DAC OUT1 V_{DDA} V_{SSA} TIMER 7 @ V_{DDA} 12-bit DAC ► DAC_OUT2 @ V_{DDA} Power domain of analog blocks: V_{BAT} V_{DD} V_{DDA} MSv34957V2

Figure 1. Block diagram



3 Functional overview

Figure 1 shows the general block diagram of the STM32F091xB/xC devices.

3.1 ARM[®]-Cortex[®]-M0 core

The ARM[®] Cortex[®]-M0 is a generation of ARM 32-bit RISC processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM[®] Cortex[®]-M0 processors feature exceptional code-efficiency, delivering the high performance expected from an ARM core, with memory sizes usually associated with 8- and 16-bit devices.

The STM32F091xB/xC devices embed ARM core and are compatible with all ARM tools and software.

3.2 Memories

The device has the following features:

- 32 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
 - up to 256 Kbytes of embedded Flash memory for programs and data
 - Option bytes

The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no readout protection
- Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- Level 2: chip readout protection, debug features (Cortex[®]-M0 serial wire) and boot in RAM selection disabled

3.3 Boot modes

At startup, the boot pin and boot selector option bits are used to select one of the three boot options:

- boot from User Flash memory
- boot from System Memory
- boot from embedded SRAM

The boot pin is shared with the standard GPIO and can be disabled through the boot selector option bits. The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART on pins PA14/PA15 or PA9/PA10 or I²C on pins PB6/PB7.



3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.5 Power management

3.5.1 Power supply schemes

- V_{DD} = V_{DDIO1} = 2.0 to 3.6 V: external power supply for I/Os (V_{DDIO1}) and the internal regulator. It is provided externally through VDD pins.
- V_{DDA} = from V_{DD} to 3.6 V: external analog power supply for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC or DAC are used). It is provided externally through VDDA pin. The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be established first.
- V_{DDIO2} = 1.65 to 3.6 V: external power supply for marked I/Os. V_{DDIO2} is provided externally through the VDDIO2 pin. The V_{DDIO2} voltage level is completely independent from V_{DD} or V_{DDA}, but it must not be provided without a valid supply on V_{DD}. The V_{DDIO2} supply is monitored and compared with the internal reference voltage (V_{REFINT}). When the V_{DDIO2} is below this threshold, all the I/Os supplied from this rail are disabled by hardware. The output of this comparator is connected to EXTI line 31 and it can be used to generate an interrupt. Refer to the pinout diagrams or tables for concerned I/Os list.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to Figure 13: Power supply scheme.

3.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD}



threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.5.3 Voltage regulator

The regulator has two operating modes and it is always enabled after reset.

- Main (MR) is used in normal operating mode (Run).
- Low power (LPR) can be used in Stop mode where the power demand is reduced.

In Standby mode, it is put in power down mode. In this mode, the regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

3.5.4 Low-power modes

The STM32F091xB/xC microcontrollers support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines, the PVD output, RTC, I2C1, USART1, USART2, USART3, COMPx, V_{DDIO2} supply comparator or the CEC.

The CEC, USART1, USART2, USART3 and I2C1 peripherals can be configured to enable the HSI RC oscillator so as to get clock for processing incoming data. If this is used when the voltage regulator is put in low power mode, the regulator is first switched to normal mode before the clock is provided to the given peripheral.

Standby mode

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the RTC domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC event occurs.

The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches



Note:

back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

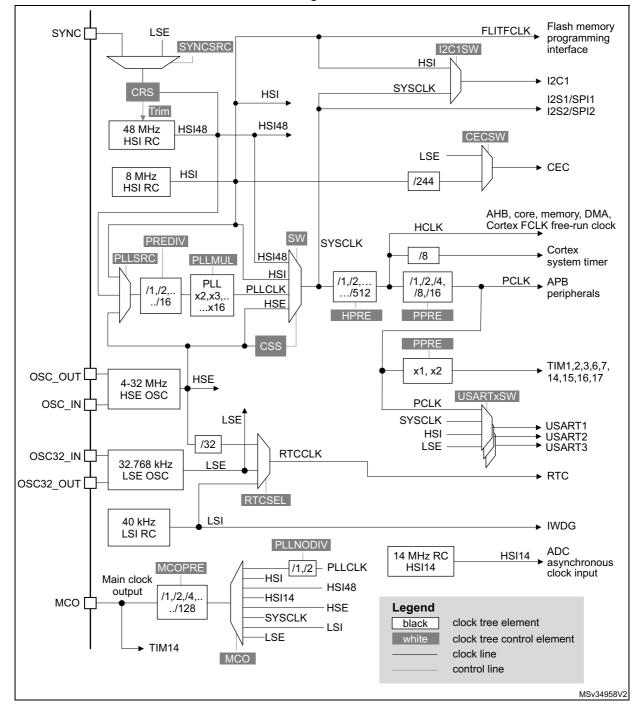


Figure 2. Clock tree

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.



Additionally, also the internal RC 48 MHz oscillator can be selected for system clock or PLL input source. This oscillator can be automatically fine-trimmed by the means of the CRS peripheral using the external synchronization.

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.8 Direct memory access controller (DMA)

The 12-channel general-purpose DMAs (seven channels for DMA1 and five channels for DMA2) manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMAs support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPIx, I2Sx, I2Cx, USARTx, all TIMx timers (except TIM14), DAC and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F0xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex[®]-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 32 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 88 GPIOs can be connected to the 16 external interrupt lines.

3.10 Analog-to-digital converter (ADC)

The 12-bit analog-to-digital converter has up to 16 external and 3 internal (temperature sensor, voltage reference, VBAT voltage measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), V _{DDA} = 3.3 V (± 10 mV)	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at a temperature of 110 °C (± 5 °C), V _{DDA} = 3.3 V (± 10 mV)	0x1FFF F7C2 - 0x1FFF F7C3

Table 3. Temperature sensor calibration values

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. The



precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 4. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at a temperature of 30 °C (± 5 °C), V _{DDA} = 3.3 V (± 10 mV)	0x1FFF F7BA - 0x1FFF F7BB

3.10.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN18. As the V_{BAT} voltage may be higher than V_{DDA} , and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.11 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This digital Interface supports the following features:

- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion

Six DAC trigger inputs are used in the device. The DAC is triggered through the timer trigger outputs and the DAC interface is generating its own DMA requests.

3.12 Comparators (COMP)

The device embeds two fast rail-to-rail low-power comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pins
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to Table 28: Embedded internal reference voltage for the value and precision of the internal reference voltage.

Both comparators can wake up from STOP mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

3.13 Touch sensing controller (TSC)

The STM32F091xB/xC devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 24 capacitive sensing channels distributed over 8 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists in charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage, this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate. For operation, one capacitive sensing GPIO in each group is connected to an external capacitor and cannot be used as effective touch sensing channel.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library, which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 5. Capacitive sensing GPIOs available on STM32F091xB/xC devices

Group	Capacitive sensing signal name	Pin name
	TSC_G1_IO1	
1	TSC_G1_IO2	PA1
ı	TSC_G1_IO3	PA2
	TSC_G1_IO4	
	TSC_G2_IO1	PA4
2	TSC_G2_IO2	PA5
2	TSC_G2_IO3	PA6
	TSC_G2_IO4	PA7
	TSC_G3_IO1	PC5
3	TSC_G3_IO2	PB0
3	TSC_G3_IO3	PB1
	TSC_G3_IO4	PB2
	TSC_G4_IO1	PA9
4	TSC_G4_IO2	PA10
'1	TSC_G4_IO3	PA11
	TSC_G4_IO4	PA12

Group	Capacitive sensing signal name	Pin name
	TSC_G5_IO1	PB3
5	TSC_G5_IO2	PB4
	TSC_G5_IO3	PB6
	TSC_G5_IO4	PB7
	TSC_G6_IO1	PB11
6	TSC_G6_IO2	PB12
6	TSC_G6_IO3	PB13
	TSC_G6_IO4	PB14
7	TSC_G7_IO1	PE2
	TSC_G7_IO2	PE3
	TSC_G7_IO3	PE4
	TSC_G7_IO4	PE5
	TSC_G8_IO1	PD12
8	TSC_G8_IO2	PD13
	TSC_G8_IO3	PD14
	TSC_G8_IO4	PD15



Table 6. Number of capacitive sensing channels available on STM32F091xB/xC devices

Analog I/O gracino	Number of capacitive sensing channels			
Analog I/O group	STM32F091Vx	STM32F091Rx	STM32F091Cx	
G1	3	3	3	
G2	3	3	3	
G3	3	3	2	
G4	3	3	3	
G5	3	3	3	
G6	3	3	3	
G7	3	0	0	
G8	G8 3		0	
Number of capacitive sensing channels	24	18	17	

3.14 Timers and watchdogs

The STM32F091xB/xC devices include up to six general-purpose timers, two basic timers and an advanced control timer.

Table 7 compares the features of the different timers.

Table 7. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	3
	TIM2	32-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
General purpose TIM	TIM3	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
	TIM14	16-bit	Up	integer from 1 to 65536	No	1	-
	TIM15	16-bit	Up	integer from 1 to 65536	Yes	2	1
	TIM16 TIM17	16-bit	Up	integer from 1 to 65536	Yes	1	1
Basic	TIM6 TIM7	16-bit	Up	integer from 1 to 65536	Yes	-	-

3.14.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- input capture
- output compare
- PWM generation (edge or center-aligned modes)
- one-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

3.14.2 General-purpose timers (TIM2, 3, 14, 15, 16, 17)

There are six synchronizable general-purpose timers embedded in the STM32F091xB/xC devices (see *Table 7* for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM2, TIM3

STM32F091xB/xC devices feature two synchronizable 4-channel general-purpose timers. TIM2 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2 and TIM3 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2 and TIM3 both have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate with TIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16 and TIM17 have a complementary output with dead-time generation and independent DMA request generation.

Their counters can be frozen in debug mode.

3.14.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit time bases.

3.14.4 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.14.5 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.14.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- a 24-bit down counter
- autoreload capability
- maskable system interrupt generation when the counter reaches 0
- programmable clock source (HCLK or HCLK/8)

3.15 Real-time clock (RTC) and backup registers

The RTC and the five backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or at wake up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- automatic correction for 28, 29 (leap year), 30, and 31 day of the month
- programmable alarm with wake up from Stop and Standby mode capability
- Periodic wakeup unit with programmable resolution and period.
- on-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock
- digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- Three anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection
- timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection
- reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision

The RTC clock sources can be:

- a 32.768 kHz external crystal
- a resonator or oscillator
- the internal low-power RC oscillator (typical frequency of 40 kHz)
- the high-speed external clock divided by 32

3.16 Inter-integrated circuit interface (I²C)

Up to two I²C interfaces (I2C1 and I2C2) can operate in multimaster or slave modes. Both can support Standard mode (up to 100 kbit/s), Fast mode (up to 400 kbit/s) and Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive on most of the associated I/Os.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). They also include programmable analog and digital noise filters.

Table 8. Comparison of I²C analog and digital filters

Aspect	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2Cx peripheral clocks
Benefits	Available in Stop mode	–Extra filtering capability vs.standard requirements–Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts



verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C peripherals can be served by the DMA controller.

Refer to Table 9 for the differences between I2C1 and I2C2.

Table 9. STM32F091xB/xC I²C implementation

I ² C features ⁽¹⁾	I2C1	I2C2
7-bit addressing mode	Х	Х
10-bit addressing mode	Х	Х
Standard mode (up to 100 kbit/s)	Х	Х
Fast mode (up to 400 kbit/s)	Х	Х
Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive I/Os	Х	Х
Independent clock	Х	-
SMBus	Х	-
Wakeup from STOP	Х	-

^{1.} X = supported.

3.17 Universal synchronous/asynchronous receiver/transmitter (USART)

The device embeds up to eight universal synchronous/asynchronous receivers/transmitters (USART1, USART2, USART3, USART4, USART5, USART6, USART7, USART8) which communicate at speeds of up to 6 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1, USART2 and USART3 support also SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability and auto baud rate feature, and have a clock domain independent of the CPU clock, allowing to wake up the MCU from Stop mode.

The USART interfaces can be served by the DMA controller.

Table 10. STM32F091xB/xC USART implementation

USART modes/features ⁽¹⁾	USART1 USART2 USART3	USART4	USART5 USART6 USART7 USART8
Hardware flow control for modem	Х	Х	-
Continuous communication using DMA	Х	Х	Х
Multiprocessor communication	Х	Х	Х
Synchronous mode	Х	Х	Х
Smartcard mode	Х	-	-