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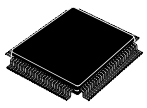
STM32F100xC STM32F100xD STM32F100xE

High-density value line, advanced ARM®-based 32-bit MCU with 256 to 512 KB Flash, 16 timers, ADC, DAC & 11 comm interfaces

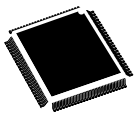
Datasheet –production data

Features

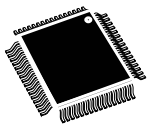
- Core: ARM® 32-bit Cortex®-M3 CPU
  - 24 MHz maximum frequency, 1.25 DMIPS /MHz (Dhrystone 2.1) performance
  - Single-cycle multiplication and hardware division
- Memories
  - 256 to 512 Kbytes of Flash memory
  - 24 to 32 Kbytes of SRAM
  - Flexible static memory controller with 4 Chip Selects. Supports SRAM, PSRAM and NOR memories
  - LCD parallel interface, 8080/6800 modes
- Clock, reset and supply management
  - 2.0 to 3.6 V application supply and I/Os
  - POR, PDR and programmable voltage detector (PVD)
  - 4-to-24 MHz crystal oscillator
  - Internal 8 MHz factory-trimmed RC
  - Internal 40 kHz RC
  - PLL for CPU clock
  - 32 kHz oscillator for RTC with calibration
- Low power
  - Sleep, Stop and Standby modes
  - V_{BAT} supply for RTC and backup registers
- Serial wire debug (SWD) and JTAG I/F
- DMA
  - 12-channel DMA controller
  - Peripherals supported: timers, ADC, SPIs, I^2Cs, USARTs and DACs
- 1 × 12-bit, 1.2 µs A/D converter (up to 16 ch.)
  - Conversion range: 0 to 3.6 V
  - Temperature sensor
- 2 × 12-bit D/A converters
- Up to 112 fast I/O ports
  - 51/80/112 I/Os, all mappable on 16 external interrupt vectors and almost all 5 V-tolerant



LQFP144
20 × 20 mm



LQFP100
14 × 14 mm



LQFP64
10 × 10 mm

- Up to 16 timers
  - Up to seven 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter
  - One 16-bit, 6-channel advanced-control timer: up to 6 channels for PWM output, dead time generation and emergency stop
  - One 16-bit timer, with 2 IC/OC, 1 OCN/PWM, dead-time generation and emergency stop
  - Two 16-bit timers, each with IC/OC/OCN/PWM, dead-time generation and emergency stop
  - Two watchdog timers
  - SysTick timer: 24-bit downcounter
  - Two 16-bit basic timers to drive the DAC
- Up to 11 communications interfaces
  - Up to two I^2C interfaces (SMBus/PMBus)
  - Up to 3 USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
  - Up to 2 UARTs
  - Up to 3 SPIs (12 Mbit/s)
  - Consumer electronics control (CEC) I/F
- CRC calculation unit, 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM32F100xC	STM32F100RC, STM32F100VC, STM32F100ZC
STM32F100xD	STM32F100RD, STM32F100VD, STM32F100ZD
STM32F100xE	STM32F100RE, STM32F100VE, STM32F100ZE

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F100xC, STM32F100xD and STM32F100xE value line microcontrollers. In the rest of the document, the STM32F100xC, STM32F100xD and STM32F100xE are referred to as high-density value line devices.

This STM32F100xC, STM32F100xD and STM32F100xE datasheet should be read in conjunction with the STM32F100xx high-density ARM®-based 32-bit MCUs *reference manual (RM0059)*. For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F100xx high-density value line Flash programming manual (PM0072).* The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the http://infocenter.arm.com.

2 Description

The STM32F100xx value line family incorporates the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a 24 MHz frequency, high-speed embedded memories (Flash memory up to 512 Kbytes and SRAM up to 32 Kbytes), a flexible static memory control (FSMC) interface (for devices offered in packages of 100 pins and more) and an extensive range of enhanced peripherals and I/Os connected to two APB buses. All devices offer standard communication interfaces (up to two I^2Cs, three SPIs, one HDMI CEC, up to three USARTs and 2 UARTS), one 12-bit ADC, two 12-bit DACs, up to 9 general-purpose 16-bit timers and an advanced-control PWM timer.

The STM32F100xx high-density value line family operates in the –40 to +85 °C and –40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F100xx value line family includes devices in three different packages ranging from 64 pins to 144 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F100xx value line microcontroller family suitable for a wide range of applications such as motor drives, application control, medical and handheld equipment, PC and gaming peripherals, GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

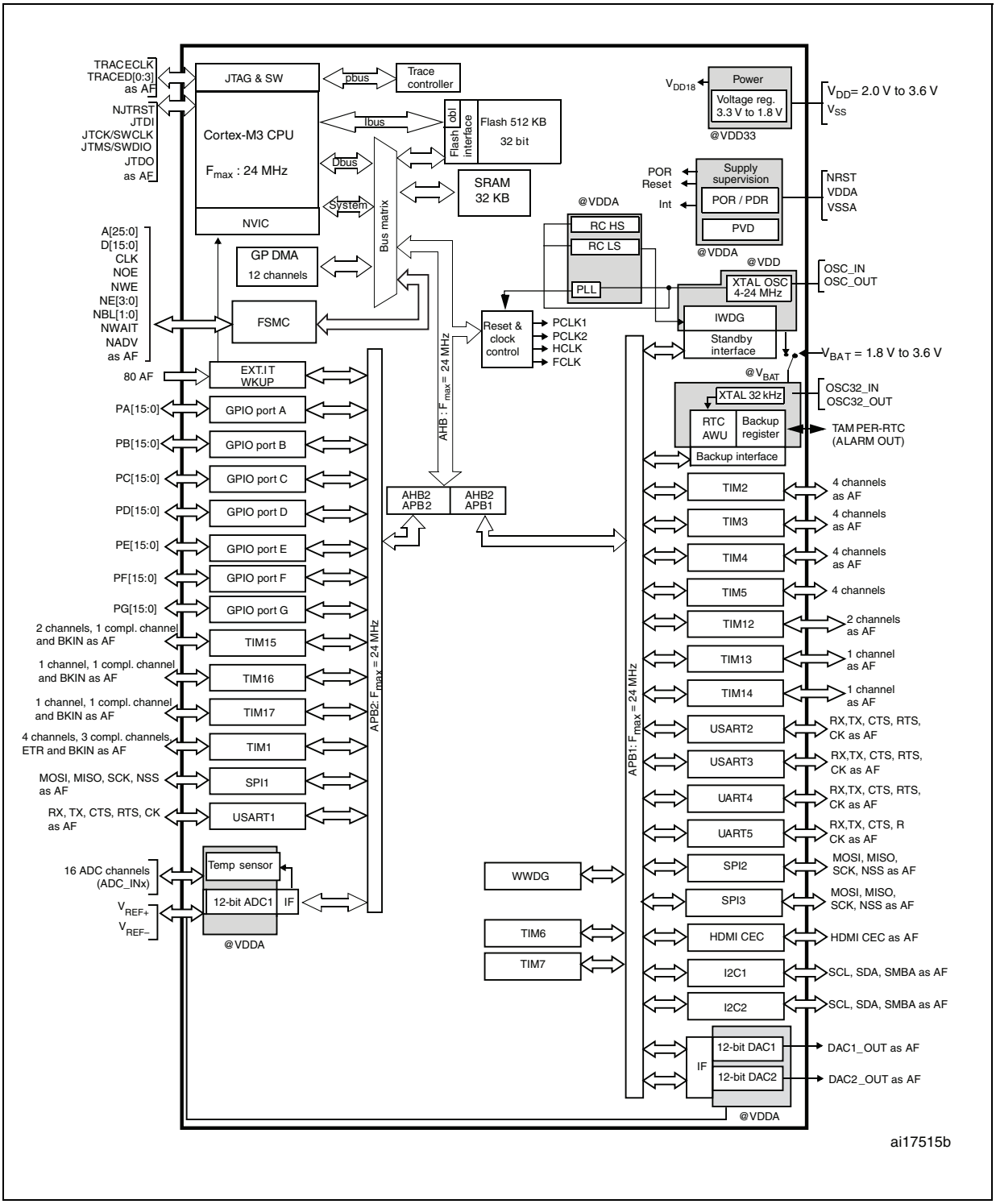
2.1 Device overview

Table 2. STM32F100xx features and peripheral counts

Peripheral		STM32F100Rx			STM32F100Vx			STM32F100Zx		
Flash - Kbytes		256	384	512	256	384	512	256	384	512
SRAM - Kbytes		24	32	32	24	32	32	24	32	32
FSMC		No			Yes(1)			Yes		
Timers	**Advanced-control**	1			1			1		
	General-purpose	10			10			10		
Communication interfaces	**SPI**	3			3			3		
	I^2C	2			2			2		
	USART	3			3			3		
	UART	2			2			2		
	CEC	1			1			1		
12-bit synchronized ADC number of channels		1 16 channels			1 16 channels			1 16 channels		
GPIOs		51			80			112		
12-bit DAC Number of channels		2 2			2 2			2 2		
CPU frequency		24 MHz								
Operating voltage		2.0 to 3.6 V								
Operating temperatures		Ambient operating temperature: –40 to +85 °C /–40 to +105 °C Junction temperature: –40 to +125 °C								
Packages		LQFP64			LQFP100			LQFP144		

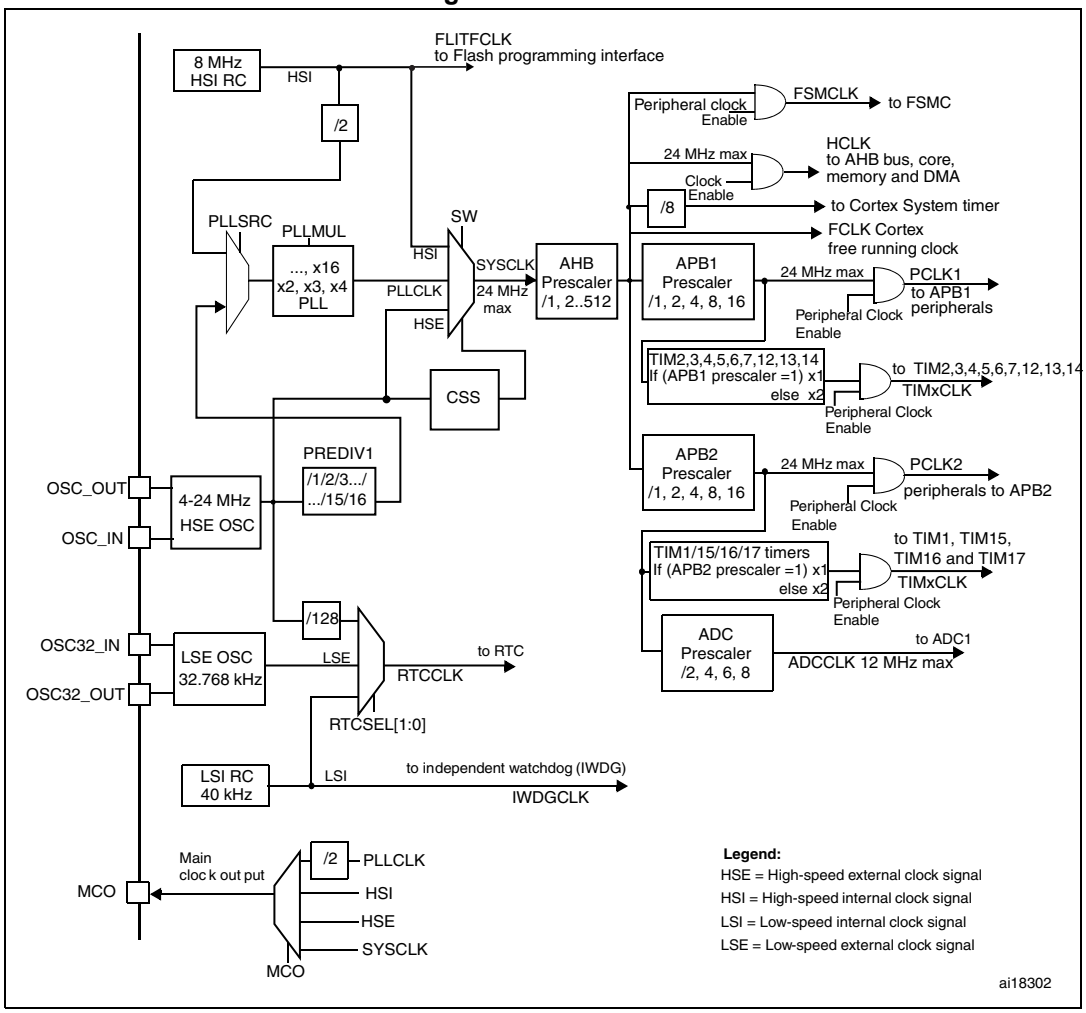
1. For the LQFP100 package, only FSMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory.

Figure 1. STM32F100xx value line block diagram



1. AF = alternate function on I/O port pin.
2. T_A = –40 °C to +85 °C (junction temperature up to 105 °C) or T_A = –40 °C to +105 °C (junction temperature up to 125 °C).

Figure 2. Clock tree



1. To obtain an ADC conversion time of 1.2 µs, APB2 must be at 24 MHz.

2.2 Overview

2.2.1 ARM® Cortex®-M3 core with embedded Flash and SRAM

The ARM Cortex®-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F100xx value line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

2.2.2 Embedded Flash memory

Up to 512 Kbytes of embedded Flash memory is available for storing programs and data.

2.2.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.2.4 Embedded SRAM

Up to 32 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.2.5 FSMC (flexible static memory controller)

The FSMC is embedded in the high-density value line family. It has four Chip Select outputs supporting the following modes: SRAM, PSRAM, and NOR.

Functionality overview:

- The three FSMC interrupt lines are ORed in order to be connected to the NVIC
- No read FIFO
- Code execution from external memory
- No boot capability
- The targeted frequency is HCLK/2, so external access is at 12 MHz when HCLK is at 24 MHz

2.2.6 LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to

specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

2.2.7 Nested vectored interrupt controller (NVIC)

The STM32F100xx value line embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.2.8 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 18 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

2.2.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-24 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 24 MHz.

2.2.10 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1. For further details please refer to AN2606.

2.2.11 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: External power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: External analog power supplies for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC or DAC is used).
  V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: Power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

2.2.12 Power supply supervisor

The device has an integrated power on reset (POR)/power down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

2.2.13 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop mode
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

2.2.14 Low-power modes

The STM32F100xx value line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put

either in normal or in low power mode.
The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output or the RTC alarm.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.2.15 DMA

The flexible 12-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The two DMA controllers support circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, DAC, I^2C, USART, all timers and ADC.

2.2.16 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.2.17 Timers and watchdogs

The STM32F100xx devices include an advanced-control timer, nine general-purpose timers, two basic timers and two watchdog timers.

Table 3 compares the features of the advanced-control, general-purpose and basic timers.

Table 3. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	Up, down, up/down	16 bits	Yes	4	Yes
TIM2, TIM3, TIM4, TIM5	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No
TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	Yes
TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	Yes
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard TIM timers which have the same architecture. The advanced control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIM2..5, TIM12..17)

There are ten synchronizable general-purpose timers embedded in the STM32F100xx devices (see *Table 3* for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM2, TIM3, TIM4, TIM5

STM32F100xx devices feature four synchronizable 4-channel general-purpose timers. These timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM12, TIM13 and TIM14

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM12 has two independent channels, whereas TIM13 and TIM14 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

Their counters can be frozen in debug mode.

TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate with TIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16, and TIM17 have a complementary output with dead-time generation and independent DMA request generation

Their counters can be frozen in debug mode.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.2.18 I²C bus

The I²C bus interface can operate in multimaster and slave modes. It can support standard and fast modes.

It supports dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.
The interface can be served by DMA and it supports SM Bus 2.0/PM Bus.

2.2.19 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F100xx value line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

The available USART interfaces communicate at up to 3 Mbit/s. They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and have LIN Master/Slave capability.

The USART interfaces can be served by the DMA controller.

2.2.20 Universal asynchronous receiver transmitter (UART)

The STM32F100xx value line embeds 2 universal asynchronous receiver transmitters (UART4, and UART5).

The available UART interfaces support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and have LIN Master/Slave capability.

The UART interfaces can be served by the DMA controller.

2.2.21 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 12 Mbit/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits.

The SPIs can be served by the DMA controller.

HDMI (high-definition multimedia interface) consumer electronics control (CEC)

The STM32F100xx value line embeds a HDMI-CEC controller that provides hardware support of consumer electronics control (CEC) (Appendix supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead.

2.2.22 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.2.23 Remap capability

This feature allows the use of a maximum number of peripherals in a given application. Indeed, alternate functions are available not only on the default pins but also on other specific pins onto which they are remappable. This has the advantage of making board design and port usage much more flexible.

For details refer to *Table 4: High-density STM32F100xx pin definitions*; it shows the list of remappable alternate functions and the pins onto which they can be remapped. See the STM32F100xx reference manual for software considerations.

2.2.24 ADC (analog-to-digital converter)

The 12-bit analog to digital converter has up to 16 external channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

2.2.25 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in noninverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- up to 10-bit output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channels' independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the STM32F100xx. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

2.2.26 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.2.27 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3 Pinouts and pin descriptions

Figure 3. STM32F100xx value line LQFP144 pinout

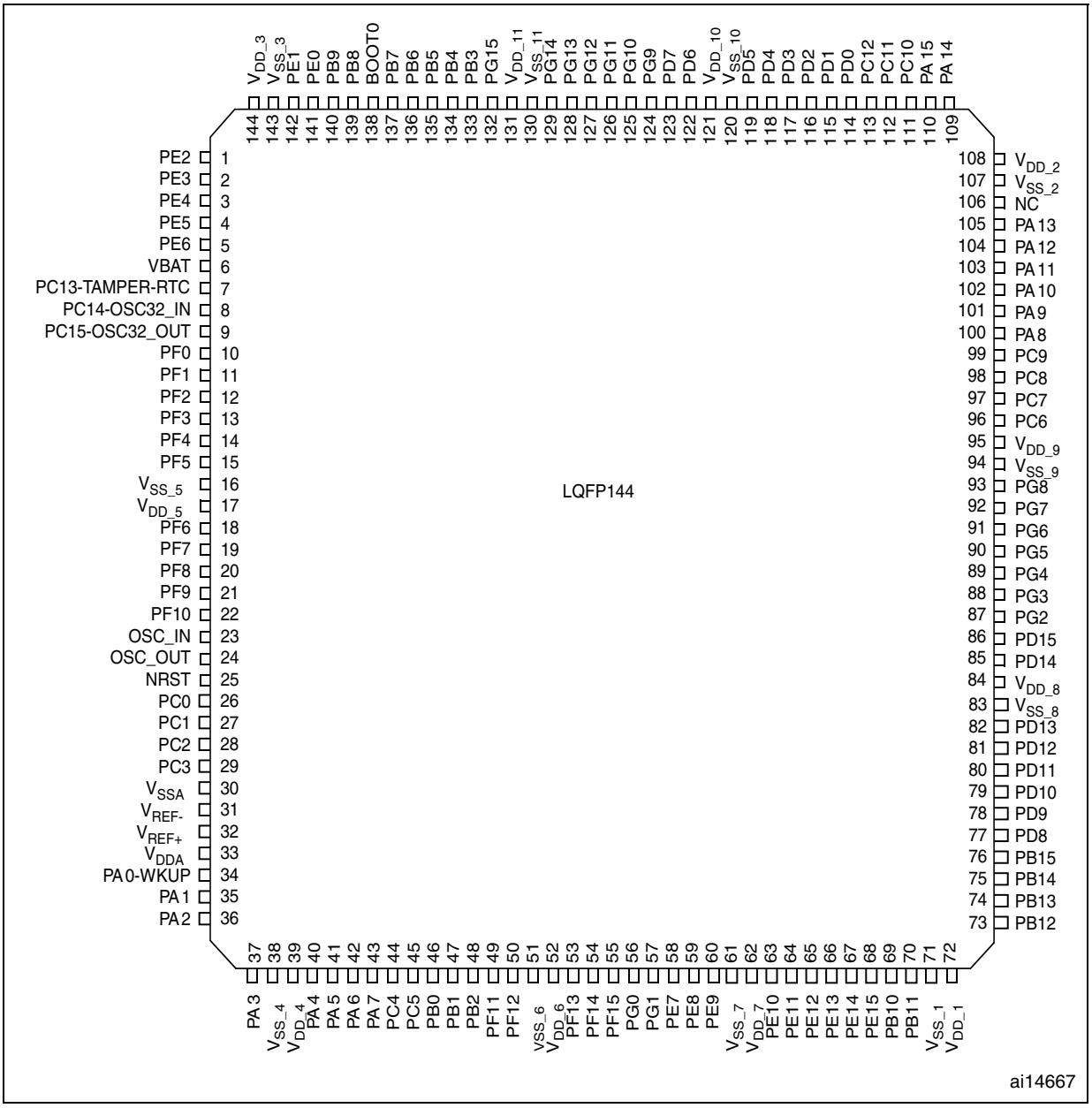


Figure 4. STM32F100xx value line LQFP100 pinout

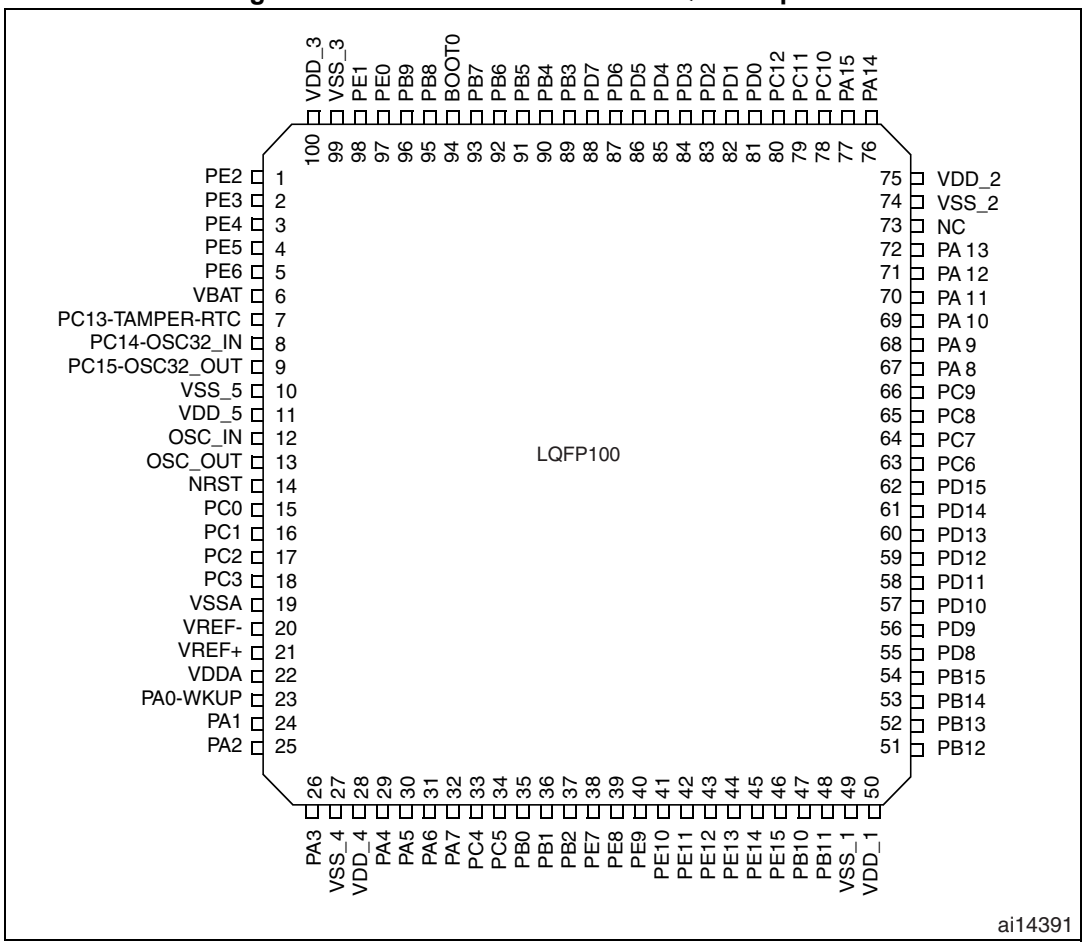


Figure 5. STM32F100xx value line in LQFP64 pinout

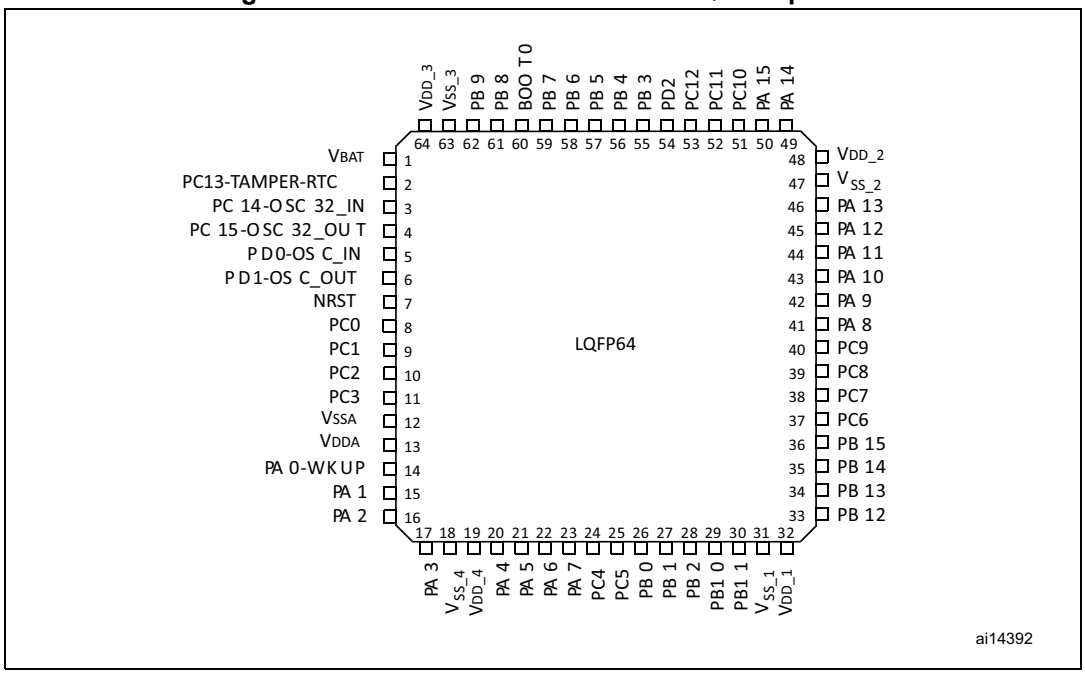


Table 4. High-density STM32F100xx pin definitions

Pins			Pin name	Type(1)	I/O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP100	LQFP64					Default	Remap
1	1	-	PE2	I/O	FT	PE2	TRACECK/ FSMC_A23	-
2	2	-	PE3	I/O	FT	PE3	TRACED0/FSMC_A19	-
3	3	-	PE4	I/O	FT	PE4	TRACED1/FSMC_A20	-
4	4	-	PE5	I/O	FT	PE5	TRACED2/FSMC_A21	-
5	5	-	PE6	I/O	FT	PE6	TRACED3/FSMC_A22	-
6	6	1	V_{BAT}	S	-	V_{BAT}	-	-
7	7	2	PC13-TAMPER-RTC(5)	I/O	-	PC13(6)	TAMPER-RTC	-
8	8	3	PC14-OSC32_IN(5)	I/O	-	PC14(6)	OSC32_IN	-
9	9	4	PC15-OSC32_OUT(5)	I/O	-	PC15(6)	OSC32_OUT	-
10	-	-	PF0	I/O	FT	PF0	FSMC_A0	-
11	-	-	PF1	I/O	FT	PF1	FSMC_A1	-
12	-	-	PF2	I/O	FT	PF2	FSMC_A2	-
13	-	-	PF3	I/O	FT	PF3	FSMC_A3	-