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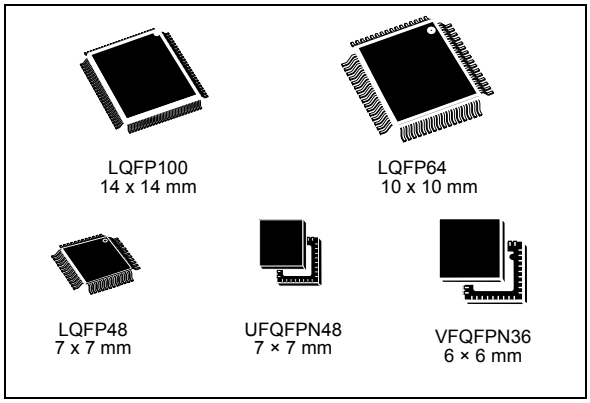
STM32F101x8
STM32F101xB

Medium-density access line, ARM®-based 32-bit MCU with 64 or 128 KB Flash, 6 timers, ADC and 7 communication interfaces

Datasheet - production data

Features

- Core: ARM® 32-bit Cortex® -M3 CPU
  - 36 MHz maximum frequency, 1.25 DMIPS/MHz (Dhrystone 2.1) performance at 0 wait state memory access
  - Single-cycle multiplication and hardware division
- Memories
  - 64 to 128 Kbytes of Flash memory
  - 10 to 16 Kbytes of SRAM
- Clock, reset and supply management
  - 2.0 to 3.6 V application supply and I/Os
  - POR, PDR and programmable voltage detector (PVD)
  - 4-to-16 MHz crystal oscillator
  - Internal 8 MHz factory-trimmed RC
  - Internal 40 kHz RC
  - PLL for CPU clock
  - 32 kHz oscillator for RTC with calibration
- Low power
  - Sleep, Stop and Standby modes
  - V_{BAT} supply for RTC and backup registers
- Debug mode
  - Serial wire debug (SWD) and JTAG interfaces
- DMA
  - 7-channel DMA controller
  - Peripherals supported: timers, ADC, SPIs, I^2Cs and USARTs
- 1 × 12-bit, 1 µs A/D converter (up to 16 channels)
  - Conversion range: 0 to 3.6 V
  - Temperature sensor
- Up to 80 fast I/O ports



  - 26/37/51/80 I/Os, all mappable on 16 external interrupt vectors and almost all 5 V-tolerant
- Six timers
  - Three 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter
  - 2 watchdog timers (Independent and Window)
  - SysTick timer: 24-bit downcounter
- Up to 7 communication interfaces
  - Up to 2 x I^2C interfaces (SMBus/PMBus)
  - Up to 3 USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
  - Up to 2 SPIs (18 Mbit/s)
- CRC calculation unit, 96-bit unique ID
- ECOPACK® packages

Table 1. Device summary

Reference	Part number
STM32F101x8	STM32F101C8, STM32F101R8 STM32F101V8, STM32F101T8
STM32F101xB	STM32F101RB, STM32F101VB, STM32F101CB STM32F101TB

Contents

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F101x8 and STM32F101xB medium-density access line microcontrollers. For more details on the whole STMicroelectronics STM32F101xx family, please refer to *Section 2.2: Full compatibility throughout the family*.

The medium-density STM32F101xx datasheet should be read in conjunction with the low-, medium- and high-density STM32F10xxx reference manual.
For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual.*
The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex® -M3 core please refer to the Cortex® -M3 Technical Reference Manual, available from the www.arm.com website.

2 Description

The STM32F101xB and STM32F101x8 medium-density access line family incorporates the high-performance ARM® Cortex® -M3 32-bit RISC core operating at a 36 MHz frequency, high-speed embedded memories (Flash memory up to 128 Kbytes and SRAM up to 16 Kbytes), and an extensive range of enhanced peripherals and I/Os connected to two APB buses. All devices offer standard communication interfaces (two I^2Cs, two SPIs, and up to three USARTs), one 12-bit ADC and three general-purpose 16-bit timers.

The STM32F101xx medium-density access line family operates in the –40 to +85 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F101xx medium-density access line family includes devices in four different packages ranging from 36 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F101xx medium-density access line microcontroller family suitable for a wide range of applications such as application control and user interface, medical and handheld equipment, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, Video intercoms, and HVACs.

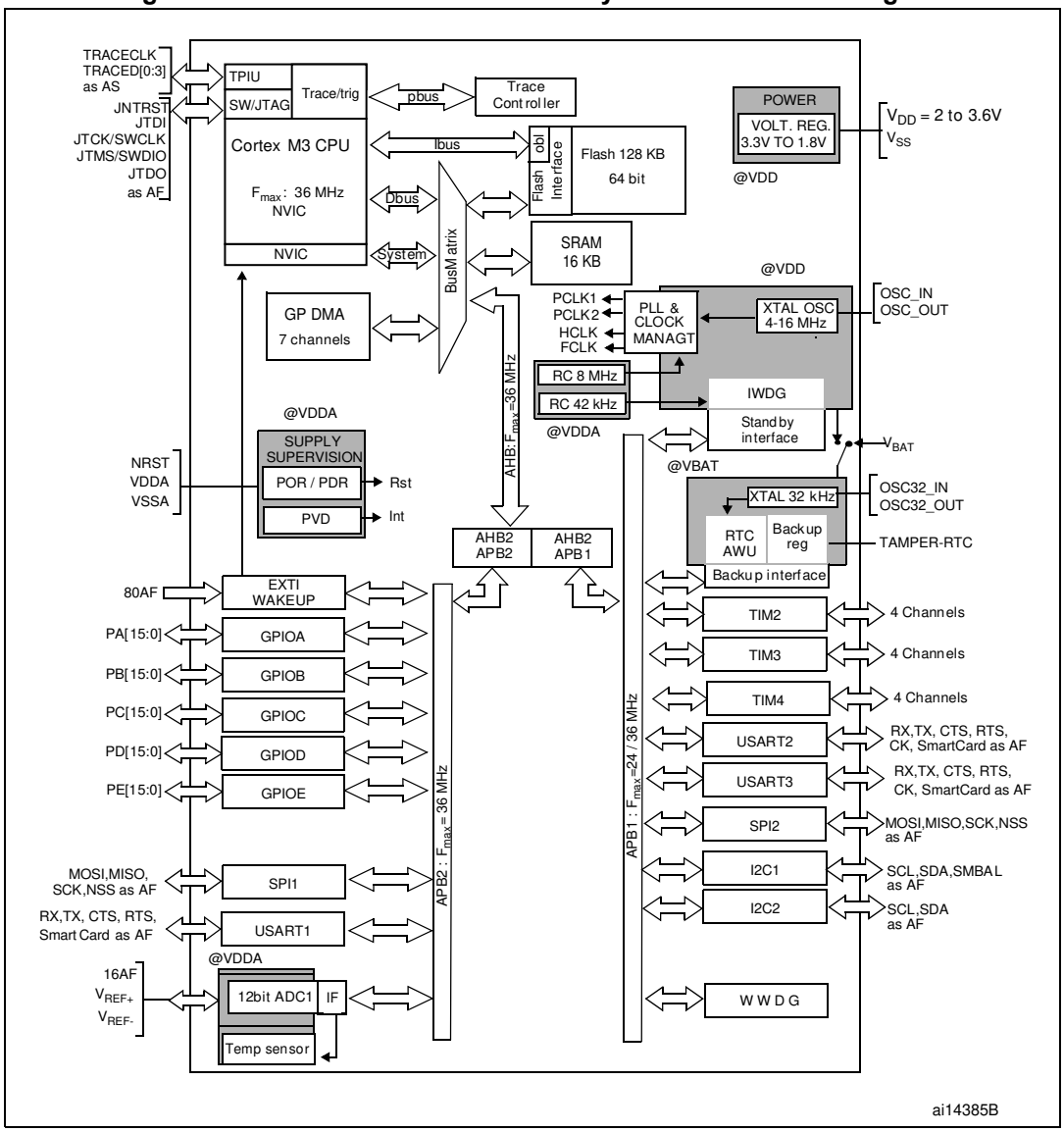
2.1 Device overview

Figure 1 shows the general block diagram of the device family.

Table 2. Device features and peripheral counts (STM32F101xx medium-density access line)

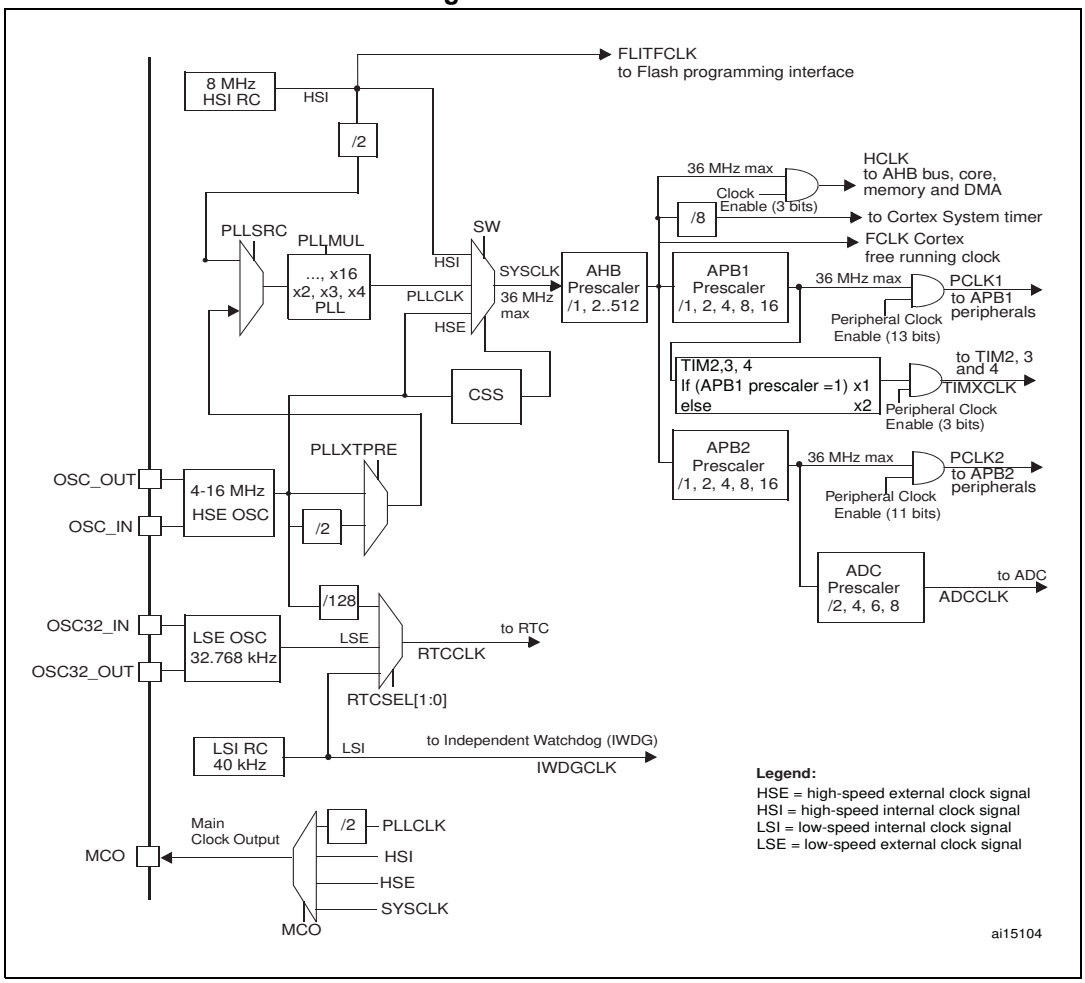
Peripheral		STM32F101Tx		STM32F101Cx		STM32F101Rx		STM32F101Vx	
Flash - Kbytes		64	128	64	128	64	128	64	128
SRAM - Kbytes		10	16	10	16	10	16	10	16
Timers	General -purpose	3		3		3		3	
Communication	SPI	1		2		2		2	
	I^2C	1		2		2		2	
	USART	2		3		3		3	
12-bit synchronized ADC number of channels		110 channels		110 channels		116 channels		116 channels	
GPIOs		26		37		51		80	
CPU frequency		36 MHz							
Operating voltage		2.0 to 3.6 V							
Operating temperatures		Ambient temperature: –40 to +85 °C (see *Table 8*) Junction temperature: –40 to +105 °C (see *Table 8*)							
Packages		VFQFPN36		LQFP48, UFQFPN48		LQFP64		LQFP100	

Figure 1. STM32F101xx medium-density access line block diagram



1. AF = alternate function on I/O port pin.
2. T_A = –40 °C to +85 °C (junction temperature up to 105 °C).

Figure 2. Clock tree



1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 36 MHz.
2. To have an ADC conversion time of 1 µs, APB2 must be at 14 MHz or 28 MHz.

2.2 Full compatibility throughout the family

The STM32F101xx is a complete family whose members are fully pin-to-pin, software and feature compatible. In the reference manual, the STM32F101x4 and STM32F101x6 are referred to as low-density devices, the STM32F101x8 and STM32F101xB are referred to as medium-density devices, and the STM32F101xC, STM32F101xD and STM32F101xE are referred to as high-density devices.

Low- and high-density devices are an extension of the STM32F101x8/B devices, they are specified in the STM32F101x4/6 and STM32F101xC/D/E datasheets, respectively. Low-density devices feature lower Flash memory and RAM capacities and a timer less. High-density devices have higher Flash memory and RAM capacities, and additional peripherals like FSMC and DAC, while remaining fully compatible with the other members of the STM32F101xx family.
The STM32F101x4, STM32F101x6, STM32F101xC, STM32F101xD and STM32F101xE are a drop-in replacement for the STM32F101x8/B medium-density devices, allowing the user to try different memory densities and providing a greater degree of freedom during the development cycle.

Moreover, the STM32F101xx performance line family is fully compatible with all existing STM32F101xx access line and STM32F102xx USB access line devices.

Table 3. STM32F101xx family

<table>
<tr><th rowspan="3">Pinout</th><th colspan="7">Memory size</th></tr>
<tr><th colspan="2">Low-density devices</th><th colspan="2">Medium-density devices</th><th colspan="3">High-density devices</th></tr>
<tr><th>16 KB Flash</th><th>32 KB Flash(1)</th><th>64 KB Flash</th><th>128 KB Flash</th><th>256 KB Flash</th><th>384 KB Flash</th><th>512 KB Flash</th></tr>
<tr><th></th><th>4 KB RAM</th><th>6 KB RAM</th><th>10 KB RAM</th><th>16 KB RAM</th><th>32 KB RAM</th><th>48 KB RAM</th><th>48 KB RAM</th></tr>
<tr><td>144</td><td>-</td><td>-</td><td>-</td><td>-</td><td colspan="3" rowspan="2">5 × USARTs
4 × 16-bit timers, 2 × basic timers
3 × SPIs, 2 × I2Cs, 1 × ADC,
2 × DACs, FSMC (100 and 144 pins)</td></tr>
<tr><td>100</td><td>-</td><td>-</td><td colspan="3" rowspan="3">3 × USARTs
3 × 16-bit timers
2 × SPIs, 2 × I2Cs,
1 × ADC</td></tr>
<tr><td>64</td><td colspan="2" rowspan="3">2 × USARTs
2 × 16-bit timers
1 × SPI, 1 × I2C
1 × ADC</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>48</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>36</td><td>-</td><td>-</td><td>-</td></tr>
</table>

1. For orderable part numbers that do not show the A internal code after the temperature range code (6), the reference datasheet for electrical characteristics is that of the STM32F101x8/B medium-density devices.

2.3 Overview

2.3.1 ARM® Cortex® -M3 core with embedded Flash and SRAM

The ARM® Cortex® -M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex® -M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F101xx medium-density access line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

2.3.2 Embedded Flash memory

64 or 128 Kbytes of embedded Flash is available for storing programs and data.

2.3.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.3.4 Embedded SRAM

Up to 16 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.3.5 Nested vectored interrupt controller (NVIC)

The STM32F101xx medium-density access line embeds a nested vectored interrupt controller able to handle up to 43 maskable interrupt channels (not including the 16 interrupt lines of Cortex® -M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.6 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

2.3.7 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 36 MHz. See *Figure 2* for details on the clock tree.

2.3.8 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1. For further details please refer to AN2606.

2.3.9 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: External power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: External analog power supplies for ADC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: Power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to *Figure 11: Power supply scheme*.

2.3.10 Power supply supervisor

The device has an integrated power on reset (POR)/power down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

Refer to *Table 10: Embedded reset and power control block characteristics* for the values of $V_{POR/PDR}$ and V_{PVD}.

2.3.11 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop mode
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

2.3.12 Low-power modes

The STM32F101xx medium-density access line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.
  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output or the RTC alarm.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.3.13 DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general purpose timers TIMx and ADC.

2.3.14 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.3.15 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

2.3.16 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

2.3.17 SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.3.18 General-purpose timers (TIMx)

There are three synchronizable general-purpose timers embedded in the STM32F101xx medium-density access line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture, output compare, PWM or one pulse mode output. This gives up to 12 input captures / output compares / PWMs on the largest packages.
The general-purpose timers can work together via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

2.3.19 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.
They can be served by DMA and they support SM Bus 2.0/PM Bus.

2.3.20 Universal synchronous/asynchronous receiver transmitter (USART)

The available USART interfaces communicate at up to 2.25 Mbit/s. They provide hardware management of the CTS and RTS signals, support IrDA SIR ENDEC, are ISO 7816 compliant and have LIN Master/Slave capability.

The USART interfaces can be served by the DMA controller.

2.3.21 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

2.3.22 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the

GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.3.23 ADC (analog to digital converter)

The 12-bit analog to digital converter has up to 16 external channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

2.3.24 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.3.25 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3 Pinouts and pin description

Figure 3. STM32F101xx medium-density access line LQFP100 pinout

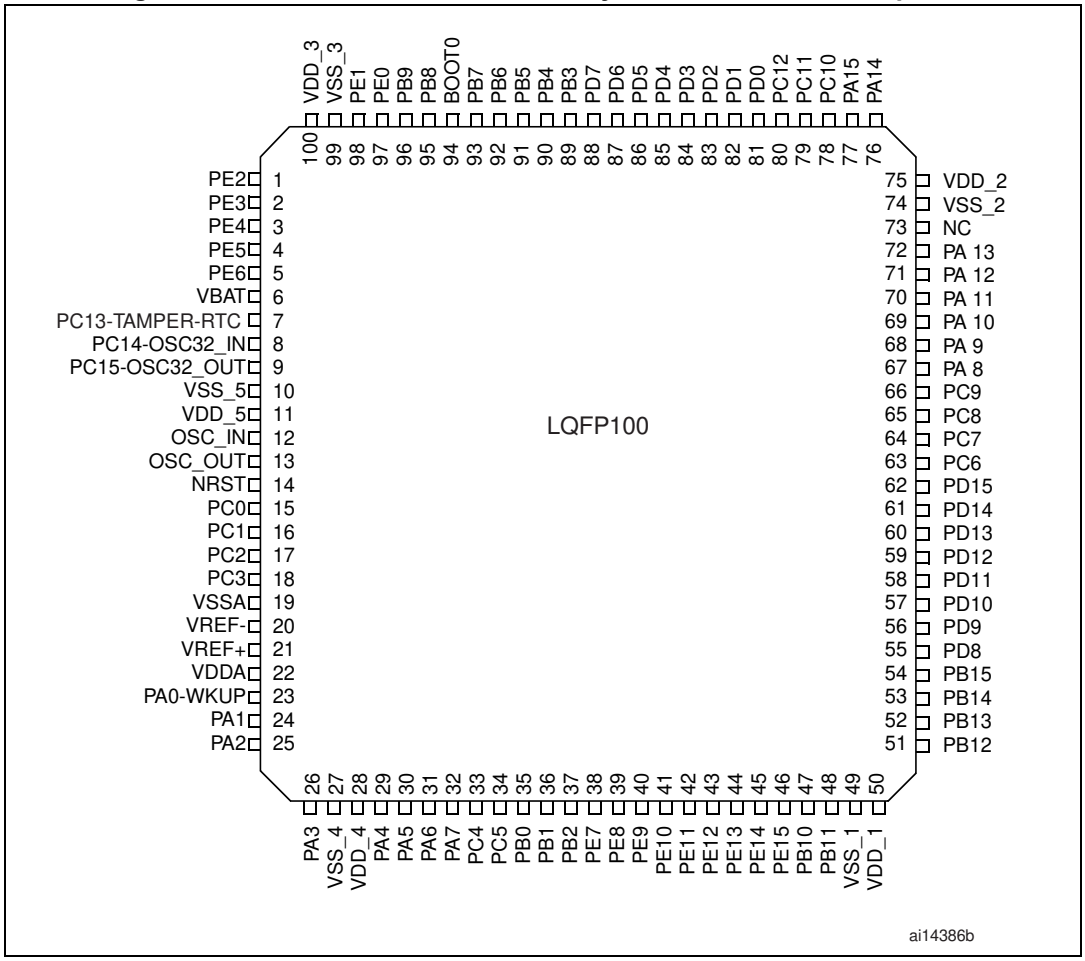


Figure 4. STM32F101xx medium-density access line LQFP64 pinout

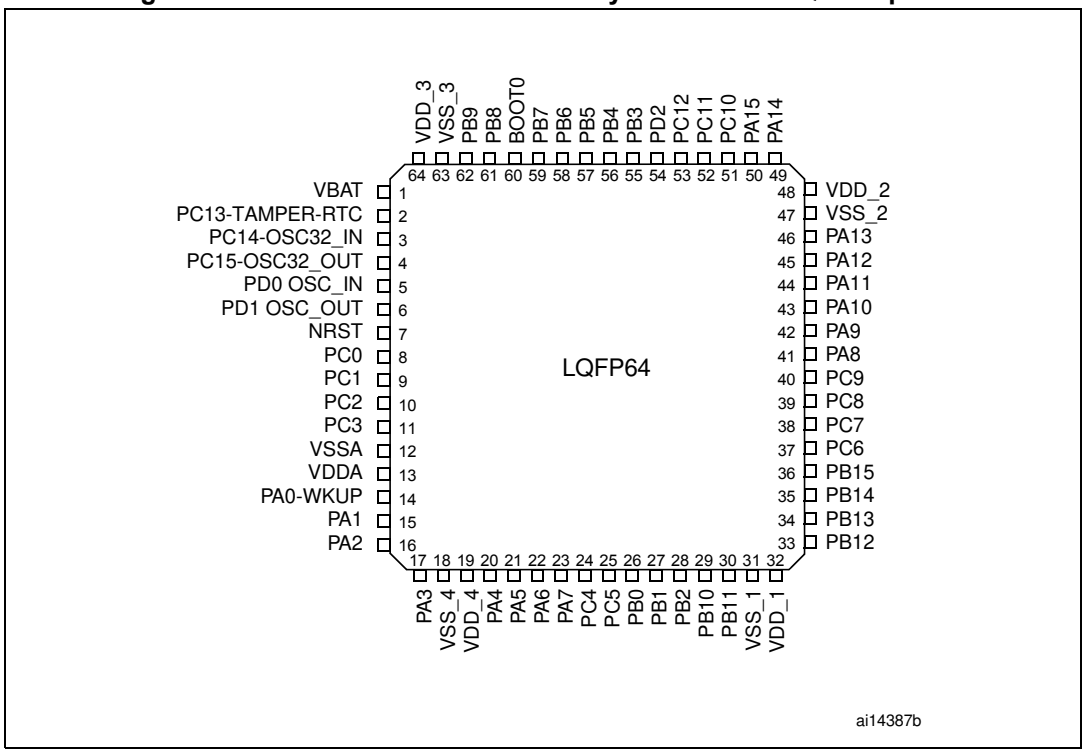


Figure 5. STM32F101xx medium-density access line LQFP48 pinout

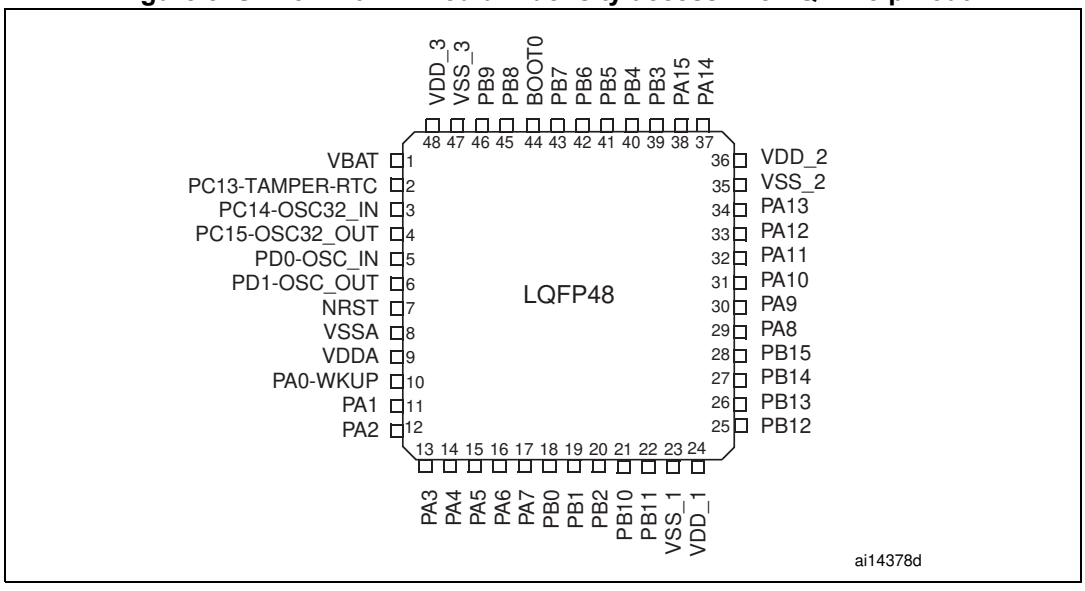


Figure 6. STM32F101xx medium-density access line UFQPFN48 pinout

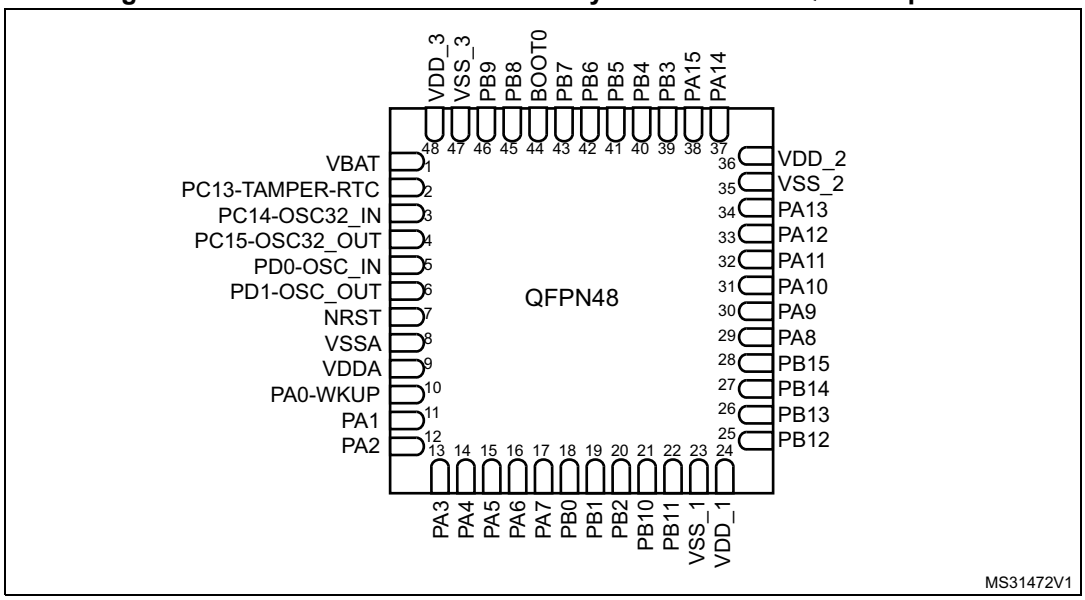


Figure 7. STM32F101xx medium-density access line VFQPFN36 pinout

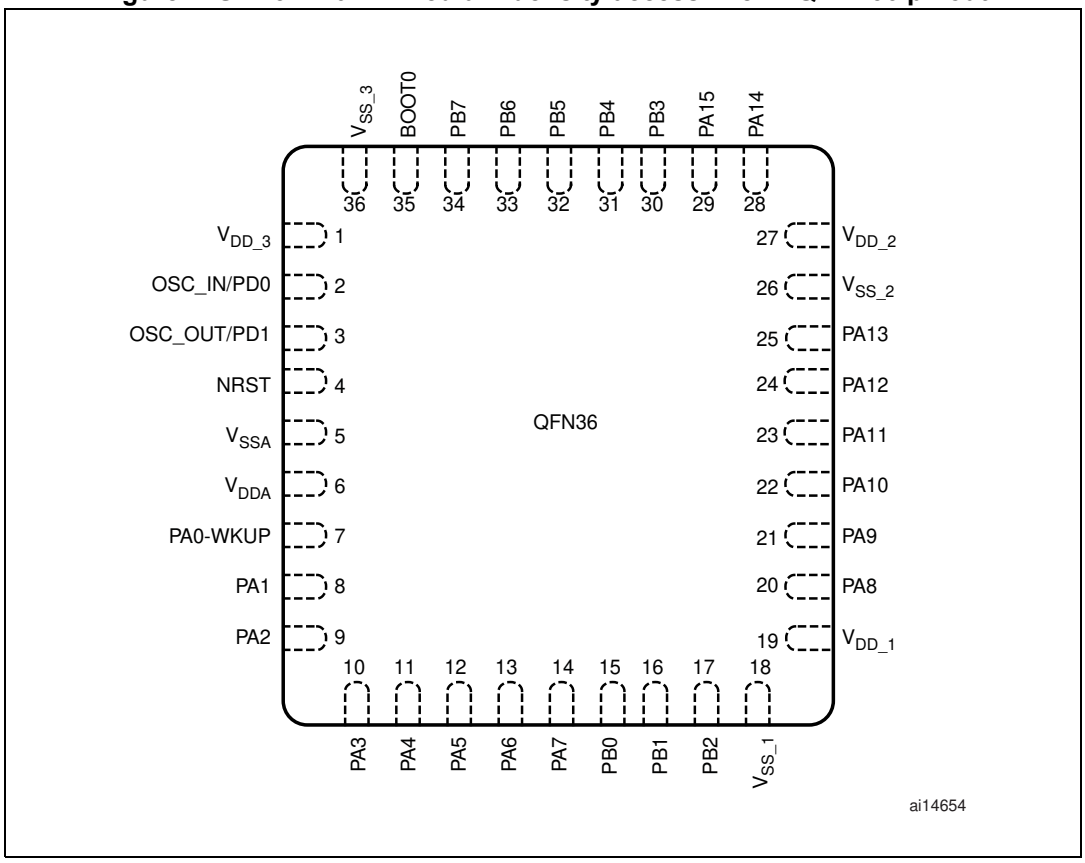


Table 4. Medium-density STM32F101xx pin definitions

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP48/ UFQFPN48	LQFP64	LQFP100	VFQFPN36					Default	Remap
-	-	1	-	PE2	I/O	FT	PE2	TRACECLK	-
-	-	2	-	PE3	I/O	FT	PE3	TRACED0	-
-	-	3	-	PE4	I/O	FT	PE4	TRACED1	-
-	-	4	-	PE5	I/O	FT	PE5	TRACED2	-
-	-	5	-	PE6	I/O	FT	PE6	TRACED3	-
1	1	6	-	V_{BAT}	S	-	V_{BAT}	-	-
2	2	7	-	PC13-TAMPER-RTC(5)	I/O	-	PC13(6)	TAMPER-RTC	-
3	3	8	-	PC14-OSC32_IN(5)	I/O	-	PC14(6)	OSC32_IN	-
4	4	9	-	PC15-OSC32_OUT(5)	I/O	-	PC15(6)	OSC32_OUT	-
-	-	10	-	V_{SS_5}	S	-	V_{SS_5}	-	-
-	-	11	-	V_{DD_5}	S	-	V_{DD_5}	-	-
5	5	12	2	OSC_IN	I	-	OSC_IN	-	PD0(7)
6	6	13	3	OSC_OUT	O	-	OSC_OUT	-	PD1(7)
7	7	14	4	NRST	I/O	-	NRST	-	-
-	8	15	-	PC0	I/O	-	PC0	ADC_IN10	-
-	9	16	-	PC1	I/O	-	PC1	ADC_IN11	-
-	10	17	-	PC2	I/O	-	PC2	ADC_IN12	-
-	11	18	-	PC3	I/O	-	PC3	ADC_IN13	-
8	12	19	5	V_{SSA}	S	-	V_{SSA}	-	-
-	-	20	-	V_{REF-}	S	-	V_{REF-}	-	-
-	-	21	-	V_{REF+}	S	-	V_{REF+}	-	-
9	13	22	6	V_{DDA}	S	-	V_{DDA}	-	-
10	14	23	7	PA0-WKUP	I/O	-	PA0	WKUP/USART2_CTS(8)/ ADC_IN0/ TIM2_CH1_ETR(8)	-
11	15	24	8	PA1	I/O	-	PA1	USART2_RTS(8)/ ADC_IN1/TIM2_CH2(8)	-

Table 4. Medium-density STM32F101xx pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP48/ UFQFPN48	LQFP64	LQFP100	VFQFPN36					Default	Remap
12	16	25	9	PA2	I/O	-	PA2	USART2_TX(8)/ ADC_IN2/TIM2_CH3(8)	-
13	17	26	10	PA3	I/O	-	PA3	USART2_RX(8)/ ADC_IN3/TIM2_CH4(8)	-
-	18	27	-	V_{SS_4}	S	-	V_{SS_4}	-	-
-	19	28	-	V_{DD_4}	S	-	V_{DD_4}	-	-
14	20	29	11	PA4	I/O	-	PA4	SPI1_NSS(8)/ADC_IN4 USART2_CK(8)/	-
15	21	30	12	PA5	I/O	-	PA5	SPI1_SCK(8)/ADC_IN5	-
16	22	31	13	PA6	I/O	-	PA6	SPI1_MISO(8)/ADC_IN6 TIM3_CH1(8)	-
17	23	32	14	PA7	I/O	-	PA7	SPI1_MOSI(8)/ADC_IN7 TIM3_CH2(8)	-
-	24	33	-	PC4	I/O	-	PC4	ADC_IN14	-
-	25	34	-	PC5	I/O	-	PC5	ADC_IN15	-
18	26	35	15	PB0	I/O	-	PB0	ADC_IN8/TIM3_CH3(8)	-
19	27	36	16	PB1	I/O	-	PB1	ADC_IN9/TIM3_CH4(8)	-
20	28	37	17	PB2	I/O	FT	PB2/BOOT1	-	-
-	-	38	-	PE7	I/O	FT	PE7	-	-
-	-	39	-	PE8	I/O	FT	PE8	-	-
-	-	40	-	PE9	I/O	FT	PE9	-	-
-	-	41	-	PE10	I/O	FT	PE10	-	-
-	-	42	-	PE11	I/O	FT	PE11	-	-
-	-	43	-	PE12	I/O	FT	PE12	-	-
-	-	44	-	PE13	I/O	FT	PE13	-	-
-	-	45	-	PE14	I/O	FT	PE14	-	-
-	-	46	-	PE15	I/O	FT	PE15	-	-
21	29	47	-	PB10	I/O	FT	PB10	I2C2_SCL/ USART3_TX (8)	TIM2_CH3
22	30	48	-	PB11	I/O	FT	PB11	I2C2_SDA/ USART3_RX (8)	TIM2_CH4