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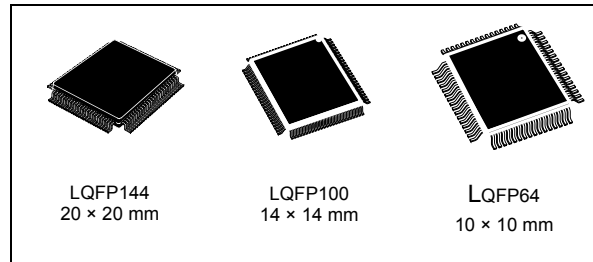


High-density access line, ARM[®]-based 32-bit MCU with 256 KB to 512 MB Flash, 9 timers, 1 ADC and 10 communication interfaces

Datasheet – production data

Features

- Core: ARM[®] 32-bit Cortex[®]-M3 CPU
 - 36 MHz maximum frequency, 1.25 DMIPS/MHz (Dhrystone 2.1) performance
 - Single-cycle multiplication and hardware division
- Memories
 - 256 to 512 Kbytes of Flash memory
 - up to 48 Kbytes of SRAM
 - Flexible static memory controller with 4 Chip Select. Supports Compact Flash, SRAM, PSRAM, NOR and NAND memories
 - LCD parallel interface, 8080/6800 modes
- Clock, reset and supply management
 - 2.0 to 3.6 V application supply and I/Os
 - POR, PDR, and programmable voltage detector (PVD)
 - 4-to-16 MHz crystal oscillator
 - Internal 8 MHz factory-trimmed RC
 - Internal 40 kHz RC with calibration capability
 - 32 kHz oscillator for RTC with calibration
- Low power
 - Sleep, Stop and Standby modes
 - V_{BAT} supply for RTC and backup registers
- 1 x 12-bit, 1 μs A/D converters (up to 16 channels)
 - Conversion range: 0 to 3.6 V
 - Temperature sensor
- 2 x 12-bit D/A converters
- DMA
 - 12-channel DMA controller
 - Peripherals supported: timers, ADC, DAC, SPIs, I²Cs and USARTs
- Up to 112 fast I/O ports



- 51/80/112 I/Os, all mappable on 16 external interrupt vectors and almost all 5 V-tolerant
- Debug mode
 - Serial wire debug (SWD) & JTAG interfaces
 - Cortex-M3 Embedded Trace Macrocell™
- Up to 9 timers
 - Up to four 16-bit timers, each with up to 4 IC/OC/PWM or pulse counters
 - 2 x watchdog timers (Independent and Window)
 - SysTick timer: a 24-bit downcounter
 - 2 x 16-bit basic timers to drive the DAC
- Up to 10 communication interfaces
 - Up to 2 x I²C interfaces (SMSTM32F101xC, STM32F101xD, STM32F101xE7816 interface, LIN, IrDA capability, modem control)
 - Up to 3 SPIs (18 Mbit/s)
- CRC calculation unit, 96-bit unique ID
- ECOPACK[®] packages

Table 1. Device summary

Reference	Part number
STM32F101xC	STM32F101RC STM32F101VC STM32F101ZC
STM32F101xD	STM32F101RD STM32F101VD STM32F101ZD
STM32F101xE	STM32F101RE STM32F101ZE STM32F101VE

Contents

1	Introduction	9
2	Description	10
2.1	Device overview	11
2.2	Full compatibility throughout the family	14
2.3	Overview	14
2.3.1	ARM® Cortex®-M3 core with embedded Flash and SRAM	14
2.3.2	Embedded Flash memory	15
2.3.3	CRC (cyclic redundancy check) calculation unit	15
2.3.4	Embedded SRAM	15
2.3.5	FSMC (flexible static memory controller)	15
2.3.6	LCD parallel interface	15
2.3.7	Nested vectored interrupt controller (NVIC)	16
2.3.8	External interrupt/event controller (EXTI)	16
2.3.9	Clocks and startup	16
2.3.10	Boot modes	16
2.3.11	Power supply schemes	17
2.3.12	Power supply supervisor	17
2.3.13	Voltage regulator	17
2.3.14	Low-power modes	17
2.3.15	DMA	18
2.3.16	RTC (real-time clock) and backup registers	18
2.3.17	Timers and watchdogs	18
2.3.18	I ² C bus	20
2.3.19	Universal synchronous/asynchronous receiver transmitters (USARTs)	20
2.3.20	Serial peripheral interface (SPI)	20
2.3.21	GPIOs (general-purpose inputs/outputs)	20
2.3.22	ADC (analog to digital converter)	21
2.3.23	DAC (digital-to-analog converter)	21
2.3.24	Temperature sensor	21
2.3.25	Serial wire JTAG debug port (SWJ-DP)	21
2.3.26	Embedded Trace Macrocell™	22
3	Pinouts and pin descriptions	23

4	Memory mapping	34
5	Electrical characteristics	36
5.1	Parameter conditions	36
5.1.1	Minimum and maximum values	36
5.1.2	Typical values	36
5.1.3	Typical curves	36
5.1.4	Loading capacitor	36
5.1.5	Pin input voltage	37
5.1.6	Power supply scheme	37
5.1.7	Current consumption measurement	38
5.2	Absolute maximum ratings	38
5.3	Operating conditions	40
5.3.1	General operating conditions	40
5.3.2	Operating conditions at power-up / power-down	40
5.3.3	Embedded reset and power control block characteristics	41
5.3.4	Embedded reference voltage	42
5.3.5	Supply current characteristics	42
5.3.6	External clock source characteristics	51
5.3.7	Internal clock source characteristics	56
5.3.8	PLL characteristics	58
5.3.9	Memory characteristics	58
5.3.10	FSMC characteristics	59
5.3.11	EMC characteristics	78
5.3.12	Absolute maximum ratings (electrical sensitivity)	80
5.3.13	I/O current injection characteristics	81
5.3.14	I/O port characteristics	82
5.3.15	NRST pin characteristics	87
5.3.16	TIM timer characteristics	89
5.3.17	Communications interfaces	89
5.3.18	12-bit ADC characteristics	95
5.3.19	DAC electrical specifications	100
5.3.20	Temperature sensor characteristics	102
6	Package information	103
6.1	LQFP144 package information	103
6.2	LQFP100 package information	107

6.3	LQFP64 information	110
6.4	Thermal characteristics	113
6.4.1	Reference document	113
6.4.2	Evaluating the maximum junction temperature for an application	114
7	Part numbering	115
8	Revision history	116

List of tables

Table 1.	Device summary	1
Table 2.	STM32F101xC, STM32F101xD and STM32F101xE features and peripheral counts	11
Table 3.	STM32F101xx family	14
Table 4.	Timer feature comparison	19
Table 5.	STM32F101xC/STM32F101xD/STM32F101xE pin definitions	25
Table 6.	FSMC pin definition	32
Table 7.	Voltage characteristics	38
Table 8.	Current characteristics	39
Table 9.	Thermal characteristics	39
Table 10.	General operating conditions	40
Table 11.	Operating conditions at power-up / power-down	40
Table 12.	Embedded reset and power control block characteristics	41
Table 13.	Embedded internal reference voltage	42
Table 14.	Maximum current consumption in Run mode, code with data processing running from Flash	43
Table 15.	Maximum current consumption in Run mode, code with data processing running from RAM	43
Table 16.	Maximum current consumption in Sleep mode, code running from Flash or RAM	45
Table 17.	Typical and maximum current consumptions in Stop and Standby modes	45
Table 18.	Typical current consumption in Run mode, code with data processing running from Flash	48
Table 19.	Typical current consumption in Sleep mode, code running from Flash or RAM	49
Table 20.	Peripheral current consumption	50
Table 21.	High-speed external user clock characteristics	51
Table 22.	Low-speed user external clock characteristics	52
Table 23.	HSE 4-16 MHz oscillator characteristics	54
Table 24.	LSE oscillator characteristics ($f_{LSE} = 32.768$ kHz)	55
Table 25.	HSI oscillator characteristics	56
Table 26.	LSI oscillator characteristics	57
Table 27.	Low-power mode wakeup timings	57
Table 28.	PLL characteristics	58
Table 29.	Flash memory characteristics	58
Table 30.	Flash memory endurance and data retention	59
Table 31.	Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings	60
Table 32.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings	61
Table 33.	Asynchronous multiplexed NOR/PSRAM read timings	62
Table 34.	Asynchronous multiplexed NOR/PSRAM write timings	64
Table 35.	Synchronous multiplexed NOR/PSRAM read timings	66
Table 36.	Synchronous multiplexed PSRAM write timings	68
Table 37.	Synchronous non-multiplexed NOR/PSRAM read timings	69
Table 38.	Synchronous non-multiplexed PSRAM write timings	70
Table 39.	Switching characteristics for PC Card/CF read and write cycles	75
Table 40.	Switching characteristics for NAND Flash read and write cycles	78
Table 41.	EMS characteristics	79
Table 42.	EMI characteristics	80
Table 43.	ESD absolute maximum ratings	80
Table 44.	Electrical sensitivities	80
Table 45.	I/O current injection susceptibility	81

Table 46.	I/O static characteristics	82
Table 47.	Output voltage characteristics	85
Table 48.	I/O AC characteristics	86
Table 49.	NRST pin characteristics	87
Table 50.	TIMx characteristics	89
Table 51.	I ² C characteristics	90
Table 52.	SCL frequency ($f_{PCLK1} = 36$ MHz, $V_{DD} = V_{DD_I2C} = 3.3$ V)	91
Table 53.	STM32F10xxx SPI characteristics	92
Table 54.	SPI characteristics	93
Table 55.	ADC characteristics	96
Table 56.	R_{AIN} max for $f_{ADC} = 14$ MHz	97
Table 57.	ADC accuracy - limited test conditions	97
Table 58.	ADC accuracy	98
Table 59.	DAC characteristics	100
Table 60.	TS characteristics	102
Table 61.	LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data	104
Table 62.	LQPF100 – 14 x 14 mm, 100-pin low-profile quad flat package mechanical data	107
Table 63.	LQFP64 – 10 x 10 mm, 64 pin low-profile quad flat package mechanical data	110
Table 64.	Package thermal characteristics	113
Table 65.	Ordering information scheme	115

List of figures

Figure 1.	STM32F101xC, STM32F101xD and STM32F101xE access line block diagram	12
Figure 2.	Clock tree	13
Figure 3.	LQFP144 pinout	23
Figure 4.	LQFP100 pinout	24
Figure 5.	LQFP64 pinout	25
Figure 6.	Memory map	35
Figure 7.	Pin loading conditions	37
Figure 8.	Pin input voltage	37
Figure 9.	Power supply scheme	37
Figure 10.	Current consumption measurement scheme	38
Figure 11.	Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled.	44
Figure 12.	Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled	44
Figure 13.	Typical current consumption on V_{BAT} with RTC on vs. temperature at different V_{BAT} values	46
Figure 14.	Typical current consumption in Stop mode with regulator in run mode versus temperature at different V_{DD} values	46
Figure 15.	Typical current consumption in Stop mode with regulator in low-power mode versus temperature at different V_{DD} values	47
Figure 16.	Typical current consumption in Standby mode versus temperature at different V_{DD} values	47
Figure 17.	High-speed external clock source AC timing diagram	53
Figure 18.	Low-speed external clock source AC timing diagram	53
Figure 19.	Typical application with an 8 MHz crystal	55
Figure 20.	Typical application with a 32.768 kHz crystal	56
Figure 21.	Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms	60
Figure 22.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms	61
Figure 23.	Asynchronous multiplexed NOR/PSRAM read waveforms.	62
Figure 24.	Asynchronous multiplexed NOR/PSRAM write waveforms	64
Figure 25.	Synchronous multiplexed NOR/PSRAM read timings	65
Figure 26.	Synchronous multiplexed PSRAM write timings.	67
Figure 27.	Synchronous non-multiplexed NOR/PSRAM read timings	69
Figure 28.	Synchronous non-multiplexed PSRAM write timings	70
Figure 29.	PC Card/CompactFlash controller waveforms for common memory read access	72
Figure 30.	PC Card/CompactFlash controller waveforms for common memory write access.	72
Figure 31.	PC Card/CompactFlash controller waveforms for attribute memory read access.	73
Figure 32.	PC Card/CompactFlash controller waveforms for attribute memory write access.	74
Figure 33.	PC Card/CompactFlash controller waveforms for I/O space read access	74
Figure 34.	PC Card/CompactFlash controller waveforms for I/O space write access	75
Figure 35.	NAND controller waveforms for read access	77
Figure 36.	NAND controller waveforms for write access	77
Figure 37.	NAND controller waveforms for common memory read access.	77
Figure 38.	NAND controller waveforms for common memory write access.	78
Figure 39.	Standard I/O input characteristics - CMOS port	83
Figure 40.	Standard I/O input characteristics - TTL port	83

Figure 41.	5 V tolerant I/O input characteristics - CMOS port	84
Figure 42.	5 V tolerant I/O input characteristics - TTL port	84
Figure 43.	I/O AC characteristics definition	87
Figure 44.	Recommended NRST pin protection	88
Figure 45.	I ² C bus AC waveforms and measurement circuit ⁽¹⁾	91
Figure 46.	SPI timing diagram - slave mode and CPHA=0	94
Figure 47.	SPI timing diagram - slave mode and CPHA=1 ⁽¹⁾	94
Figure 48.	SPI timing diagram - master mode ⁽¹⁾	95
Figure 49.	ADC accuracy characteristics	98
Figure 50.	Typical connection diagram using the ADC	99
Figure 51.	Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})	99
Figure 52.	Power supply and reference decoupling (V_{REF+} connected to V_{DDA})	100
Figure 53.	12-bit buffered /non-buffered DAC	102
Figure 54.	LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline	103
Figure 55.	LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package footprint	105
Figure 56.	LQFP144 marking (package top view)	106
Figure 57.	LQFP100 – 14 x 14 mm, 100-pin low-profile quad flat package outline	107
Figure 58.	LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint	108
Figure 59.	LQFP100 marking (package top view)	109
Figure 60.	LQFP64 – 10 x 10 mm, 64 pin low-profile quad flat package outline	110
Figure 61.	Recommended footprint	111
Figure 62.	LQFP64 marking (package top view)	112
Figure 63.	LQFP64 P_D max vs. T_A	114

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F101xC, STM32F101xD and STM32F101xE high-density access line microcontrollers. For more details on the whole STMicroelectronics STM32F101xx family, please refer to [Section 2.2: Full compatibility throughout the family](#).

The high-density STM32F101xx datasheet should be read in conjunction with the STM32F10xxx reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual*.

The reference and Flash programming manuals are both available from the STMicroelectronics website www.st.com.

For information on the Cortex[®]-M3 core please refer to the Cortex[®]-M3 Technical Reference Manual, available from the www.arm.com website.



2 Description

The STM32F101xC, STM32F101xD and STM32F101xE access line family incorporates the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a 36 MHz frequency, high-speed embedded memories (Flash memory up to 512 Kbytes and SRAM up to 48 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer one 12-bit ADC, four general-purpose 16-bit timers, as well as standard and advanced communication interfaces: up to two I²Cs, three SPIs and five USARTs.

The STM32F101xx high-density access line family operates in the –40 to +85 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

These features make the STM32F101xx high-density access line microcontroller family suitable for a wide range of applications such as medical and handheld equipment, PC peripherals and gaming, GPS platforms, industrial applications, PLC, printers, scanners alarm systems and video intercom.

2.1 Device overview

The STM32F101xx high-density access line family offers devices in 3 different package types: from 64 pins to 144 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

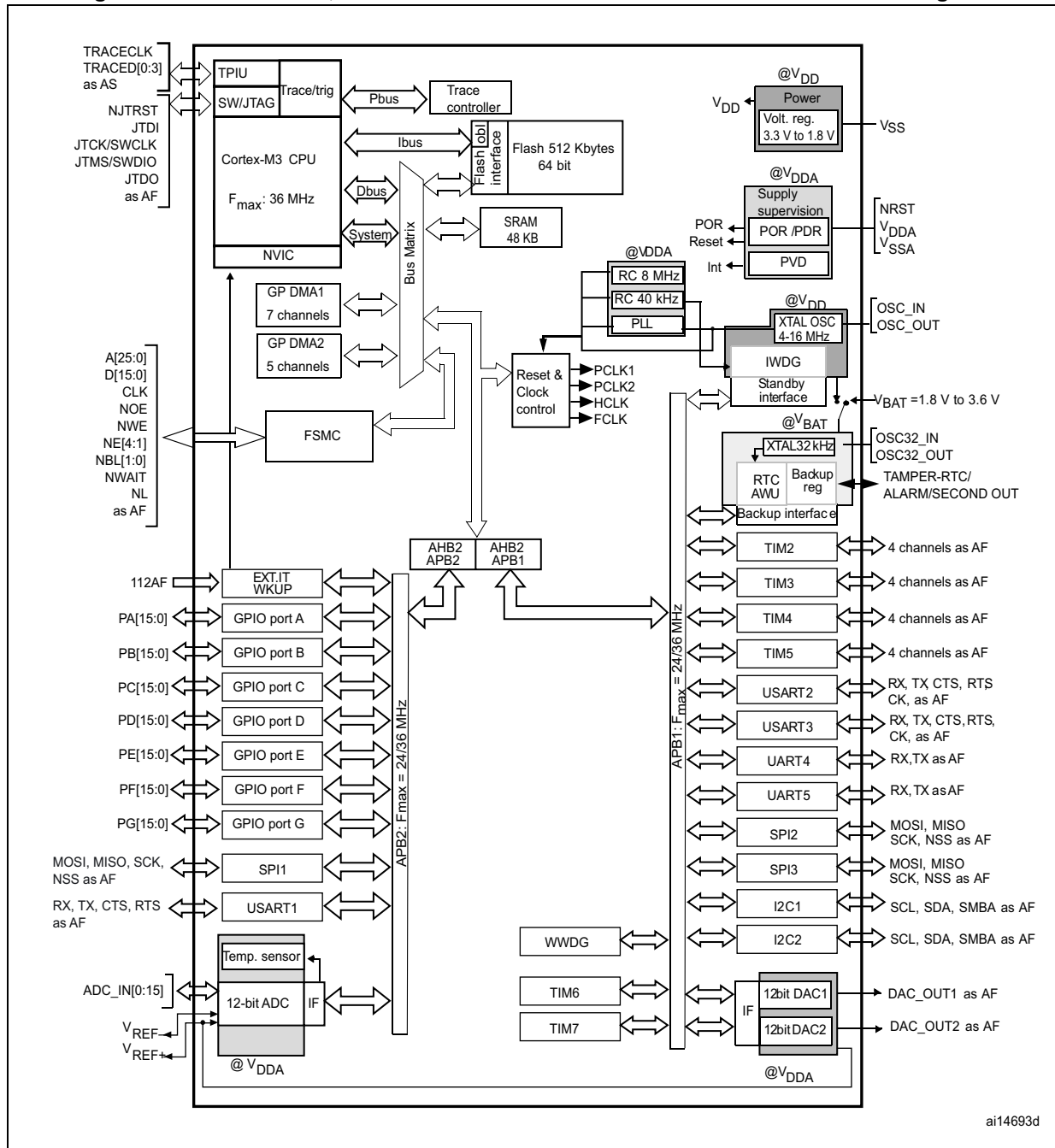
[Figure 1](#) shows the general block diagram of the device family.

Table 2. STM32F101xC, STM32F101xD and STM32F101xE features and peripheral counts

Peripherals		STM32F101Rx			STM32F101Vx			STM32F101Zx		
Flash memory in Kbytes		256	384	512	256	384	512	256	384	512
SRAM in Kbytes		32	48		32	48		32	48	
FSMC		No			Yes ⁽¹⁾			Yes		
Timers	General-purpose	4								
	Basic	2								
Comm	SPI	3								
	I ² C	2								
	USART	5								
GPIOs		51			80			112		
12-bit ADC		Yes			Yes			Yes		
Number of channels		16			16			16		
12-bit DAC		1								
Number of channels		2								
CPU frequency		36 MHz								
Operating voltage		2.0 to 3.6 V								
Operating temperatures		Ambient temperature: -40 to +85 °C (see Table 10) Junction temperature: -40 to +105 °C (see Table 10)								
Package		LQFP64			LQFP100			LQFP144		

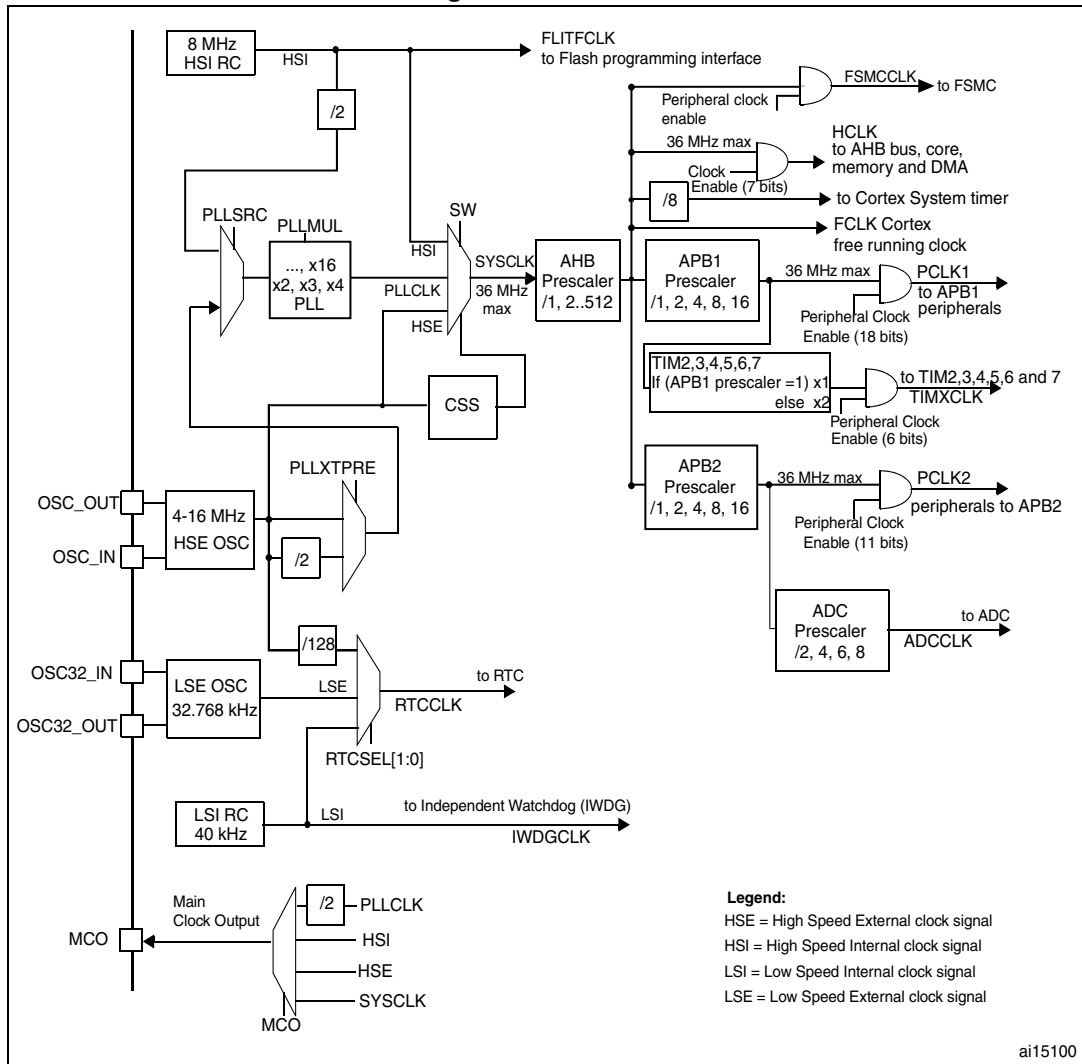
1. For the LQFP100 package, only FSMC Bank1 and Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.

Figure 1. STM32F101xC, STM32F101xD and STM32F101xE access line block diagram



1. $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ (junction temperature up to $105\text{ }^{\circ}\text{C}$).
2. AF = alternate function on I/O port pin.

Figure 2. Clock tree



1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 36 MHz.
2. To have an ADC conversion time of 1 μ s, APB2 must be at 14 MHz or 28 MHz.

2.2 Full compatibility throughout the family

The STM32F101xx is a complete family whose members are fully pin-to-pin, software and feature compatible. In the reference manual, the STM32F101x4 and STM32F101x6 are identified as low-density devices, the STM32F101x8 and STM32F101xB are referred to as medium-density devices, and the STM32F101xC, STM32F101xD and STM32F101xE are referred to as high-density devices .

Low- and high-density devices are an extension of the STM32F101x8/B medium-density devices, they are specified in the STM32F101x4/6 and STM32F101xC/D/E datasheets, respectively.

Low-density devices feature lower Flash memory and RAM capacities, less timers and peripherals. High-density devices have higher Flash memory and RAM densities, and additional peripherals like FSMC and DAC, while remaining fully compatible with the other members of the family.

The STM32F101x4, STM32F101x6, STM32F101xC, STM32F101xD and STM32F101xE are a drop-in replacement for the STM32F101x8/B devices, allowing the user to try different memory densities and providing a greater degree of freedom during the development cycle.

Moreover, the STM32F101xx access line family is fully compatible with all existing STM32F103xx performance line and STM32F102xx USB access line devices.

Table 3. STM32F101xx family

Pinout	Memory size						
	Low-density devices		Medium-density devices		High-density devices		
	16 KB Flash	32 KB Flash ⁽¹⁾	64 KB Flash	128 KB Flash	256 KB Flash	384 KB Flash	512 KB Flash
	4 KB RAM	6 KB RAM	10 KB RAM	16 KB RAM	32 KB RAM	48 KB RAM	48 KB RAM
144					5 × USARTs		
100					4 × 16-bit timers. 2 × basic timers		
64	2 × USARTs		3 × USARTs		3 × SPIs, 2 × I ² Cs, 1 × ADC. 2 × DACs		
48	2 × 16-bit timers		3 × 16-bit timers		FSMC (100 and 144 pins)		
	1 × SPI, 1 × I ² C		2 × SPIs, 2 × I ² Cs,				
36	1 × ADC		1 × ADC				

1. For orderable part numbers that do not show the A internal code after the temperature range code (6), the reference datasheet for electrical characteristics is that of the STM32F101x8/B medium-density devices.

2.3 Overview

2.3.1 ARM[®] Cortex[®]-M3 core with embedded Flash and SRAM

The ARM[®] Cortex[®]-M3 processor is the latest generation of ARM[®] processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while

delivering outstanding computational performance and an advanced system response to interrupts.

The ARM[®] Cortex[®]-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM[®] core in the memory size usually associated with 8- and 16-bit devices.

The STM32F101xC, STM32F101xD and STM32F101xE access line family having an embedded ARM[®] core, is therefore compatible with all ARM[®] tools and software.

Figure 1 shows the general block diagram of the device family.

2.3.2 Embedded Flash memory

256 to 512 Kbytes of embedded Flash are available for storing programs and data.

2.3.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.3.4 Embedded SRAM

Up to 48 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.3.5 FSMC (flexible static memory controller)

The FSMC is embedded in the STM32F101xC, STM32F101xD and STM32F101xE access line family. It has four Chip Select outputs supporting the following modes: PC Card/Compact Flash, SRAM, PSRAM, NOR and NAND.

Functionality overview:

- The three FSMC interrupt lines are ORed in order to be connected to the NVIC
- Write FIFO
- Code execution from external memory except for NAND Flash and PC Card
- The targeted frequency is HCLK/2, so external access is at 18 MHz when HCLK is at 36 MHz

2.3.6 LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

2.3.7 Nested vectored interrupt controller (NVIC)

The STM32F101xC, STM32F101xD and STM32F101xE access line embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex[®]-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.8 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

2.3.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers are used to configure the AHB frequency, the high-speed APB (APB2) domain and the low-speed APB (APB1) domain. The maximum frequency of the AHB and APB domains is 36 MHz. See [Figure 2](#) for details on the clock tree.

2.3.10 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash: you have an option to boot from any of two memory banks. By default, boot from Flash memory bank 1 is selected. You can choose to boot from Flash memory bank 2 by setting a bit in the option bytes.
- Boot from system memory
- Boot from embedded SRAM

The bootloader is located in system memory. It is used to reprogram the Flash memory by using USART1.

2.3.11 Power supply schemes

- $V_{DD} = 2.0$ to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA} , $V_{DDA} = 2.0$ to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC or DAC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.
- $V_{BAT} = 1.8$ to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to [Figure 9: Power supply scheme](#).

2.3.12 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software. Refer to [Table 12: Embedded reset and power control block characteristics](#) for the values of $V_{POR/PDR}$ and V_{PVD} .

2.3.13 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop modes.
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode.

2.3.14 Low-power modes

The STM32F101xC, STM32F101xD and STM32F101xE access line supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**
In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop mode**
Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output or the RTC alarm.

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.3.15 DMA

The flexible 12-channel general-purpose DMAs (7 channels for DMA1 and 5 channels for DMA2) are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPI, I²C, USART, general-purpose and basic timers TIMx, DAC and ADC.

2.3.16 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high speed external clock divided by 128. The internal low-speed RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.3.17 Timers and watchdogs

The high-density STM32F101xx access line devices include up to four general-purpose timers, two basic timers, two watchdog timers and a SysTick timer.

[Table 4](#) compares the features of the general-purpose and basic timers.

Table 4. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3, TIM4, TIM5	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

General-purpose timers (TIMx)

There are up to 4 synchronizable general-purpose timers (TIM2, TIM3, TIM4 and TIM5) embedded in the STM32F101xC, STM32F101xD and STM32F101xE access line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input captures / output compares / PWMs on the largest packages.

The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.3.18 I²C bus

Up to two I²C bus interfaces can operate in multi-master and slave modes. They support standard and fast modes.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.3.19 Universal synchronous/asynchronous receiver transmitters (USARTs)

The STM32F101xC, STM32F101xD and STM32F101xE access line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The five interfaces are able to communicate at speeds of up to 2.25 Mbit/s.

USART1, USART2 and USART3 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

2.3.20 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

All SPIs can be served by the DMA controller.

2.3.21 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.3.22 ADC (analog to digital converter)

A 12-bit analog-to-digital converter is embedded into STM32F101xC, STM32F101xD and STM32F101xE access line devices. It has up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

2.3.23 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Seven DAC trigger inputs are used in the STM32F101xC, STM32F101xD and STM32F101xE access line family. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

2.3.24 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between $2\text{ V} < V_{DDA} < 3.6\text{ V}$. The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.3.25 Serial wire JTAG debug port (SWJ-DP)

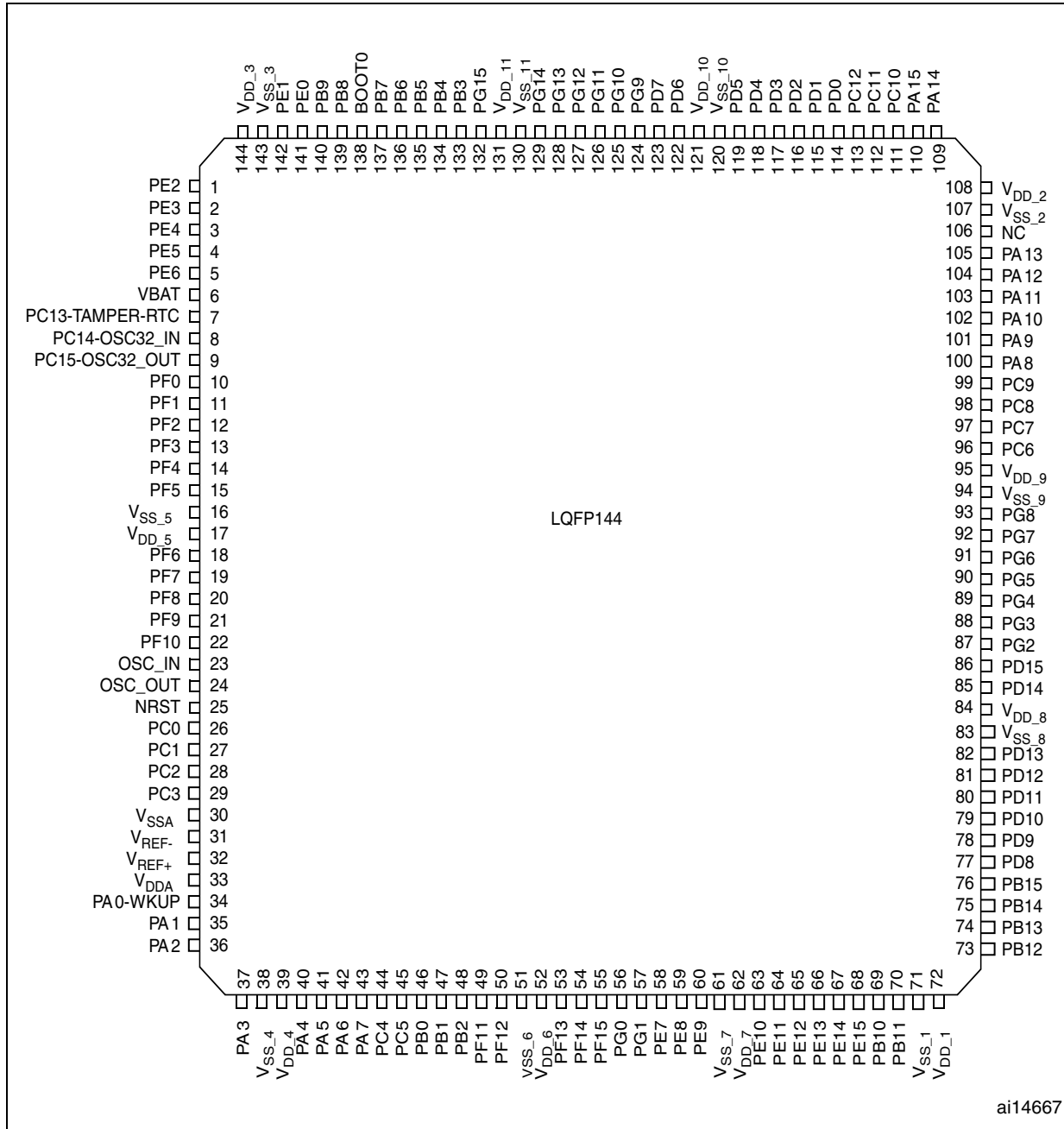
The ARM[®] SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.3.26 Embedded Trace Macrocell™

The ARM® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F10xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

3 Pinouts and pin descriptions

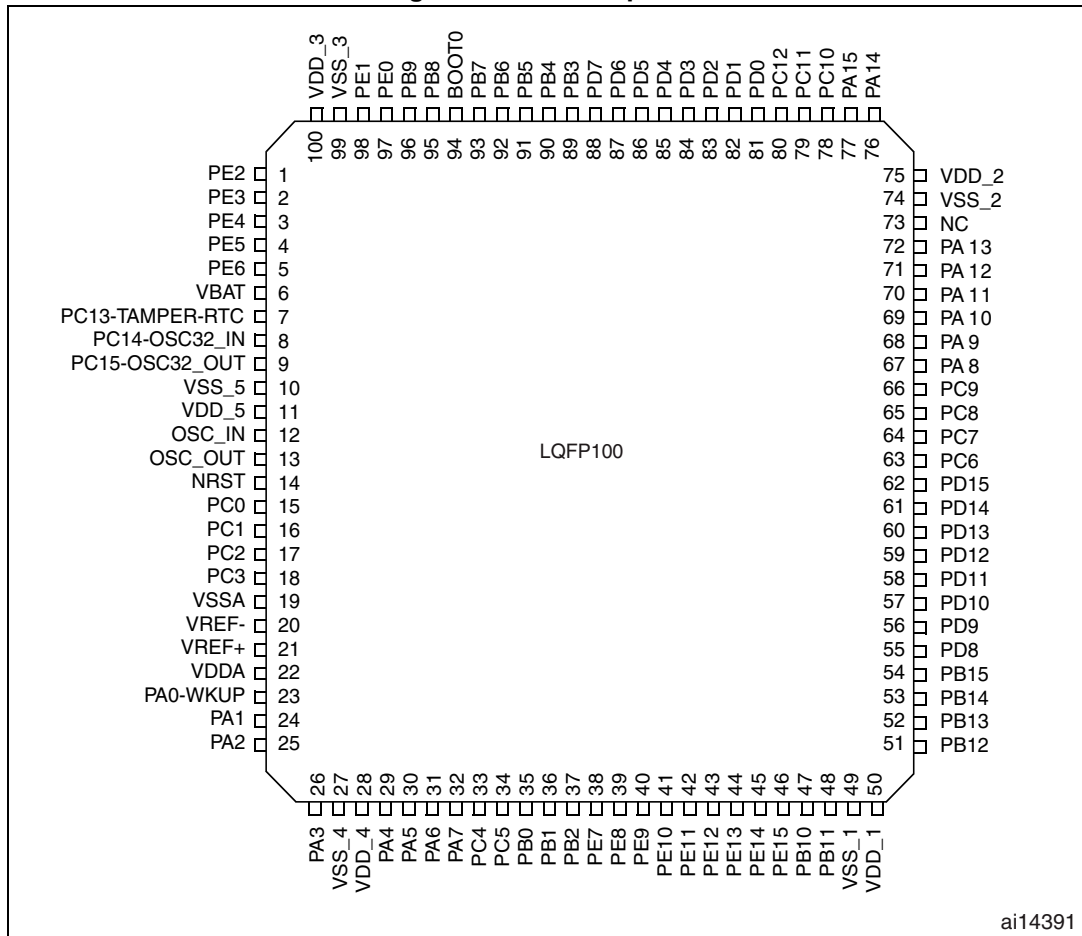
Figure 3. LQFP144 pinout



ai14667

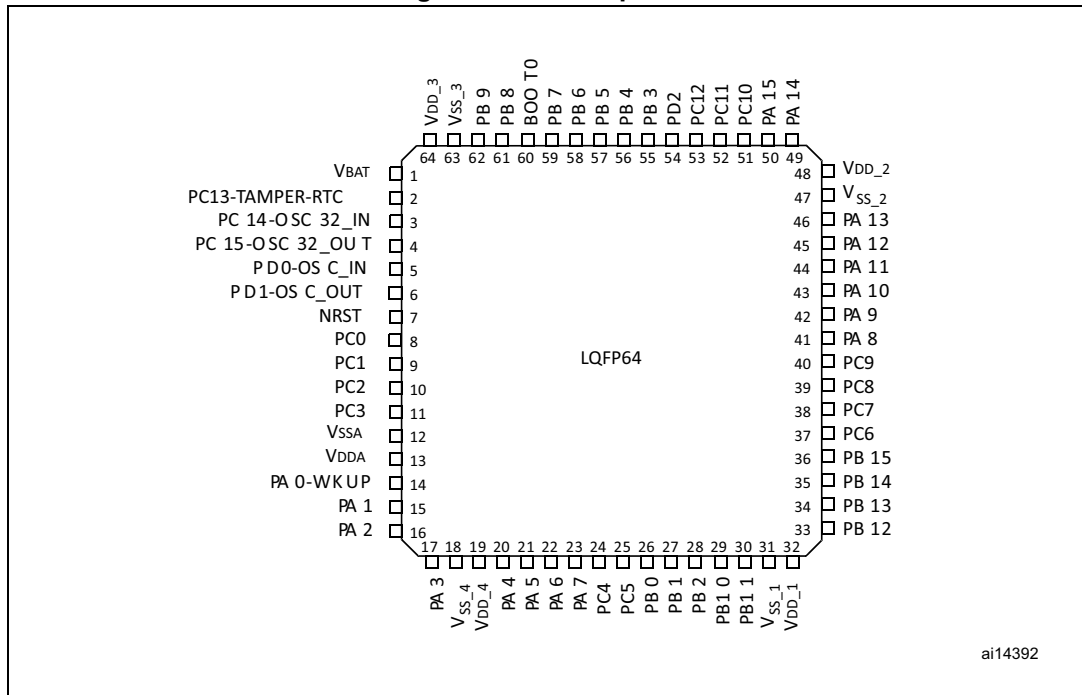
1. The above figure shows the package top view.

Figure 4. LQFP100 pinout



1. The above figure shows the package top view.

Figure 5. LQFP64 pinout



ai14392

1. The above figure shows the package top view.

Table 5. STM32F101xC/STM32F101xD/STM32F101xE pin definitions

Pins			Pin name	Type ⁽¹⁾	I / O Level ⁽²⁾	Main function ⁽³⁾ (after reset)	Alternate functions ⁽⁴⁾	
LQFP144	LQFP64	LQFP100					Default	Remap
1	-	1	PE2	I/O	FT	PE2	TRACECLK/ FSMC_A23	-
2	-	2	PE3	I/O	FT	PE3	TRACED0/FSMC_A19	-
3	-	3	PE4	I/O	FT	PE4	TRACED1/FSMC_A20	-
4	-	4	PE5	I/O	FT	PE5	TRACED2/FSMC_A21	-
5	-	5	PE6	I/O	FT	PE6	TRACED3/FSMC_A22	-
6	1	6	V _{BAT}	S	-	V _{BAT}	-	-
7	2	7	PC13-TAMPER-RTC ⁽⁵⁾	I/O	-	PC13 ⁽⁶⁾	TAMPER-RTC	-
8	3	8	PC14-OSC32_IN ⁽⁵⁾	I/O	-	PC14 ⁽⁶⁾	OSC32_IN	-
9	4	9	PC15-OSC32_OUT ⁽⁵⁾	I/O	-	PC15 ⁽⁶⁾	OSC32_OUT	-
10	-	-	PF0	I/O	FT	PF0	FSMC_A0	-
11	-	-	PF1	I/O	FT	PF1	FSMC_A1	-