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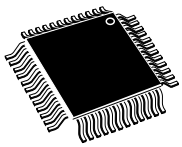
STM32F303x6/x8

ARM®Cortex®-M4 32b MCU+FPU, up to 64KB Flash, 16KB SRAM 2 ADCs, 3 DACs, 3 comp., op-amp 2.0 - 3.6 V

Datasheet - production data

Features

- Core: ARM® Cortex®-M4 32-bit CPU with FPU (72 MHz max), single-cycle multiplication and HW division, 90 DMIPS (from CCM), DSP instruction
- Memories
  - Up to 64 Kbytes of Flash memory
  - 12 Kbytes of SRAM with HW parity check
  - Routine booster: 4 Kbytes of SRAM on instruction and data bus with HW parity check (CCM)
- CRC calculation unit
- Reset and supply management
  - Low-power modes: Sleep, Stop, Standby
  - V_{DD},V_{DDA} voltage range: 2.0 to 3.6 V
  - Power-on/Power-down reset (POR/PDR)
  - Programmable voltage detector (PVD)
  - V_{BAT} supply for RTC and backup registers
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC (up to 64 MHz with PLL option)
  - Internal 40 kHz oscillator
- Up to 51 fast I/O ports, all mappable on external interrupt vectors, several 5 V-tolerant
- Interconnect Matrix
- 7-channel DMA controller
- Up to two ADC 0.20 µs (up to 21 channels) with selectable resolution of 12/10/8/6 bits, 0 to 3.6 V conversion range, single-ended/differential mode, separate analog supply from 2.0 to 3.6 V
- Temperature sensor
- Up to three 12-bit DAC channels with analog supply from 2.4 V to 3.6 V



LQFP32 (7 x 7 mm)
LQFP48 (7 x 7 mm)
LQFP64 (10 x 10 mm)

- Three ultra-fast rail-to-rail analog comparators with analog supply from 2 V to 3.6 V
- One operational amplifiers that can be used in PGA mode, all terminals accessible with analog supply from 2.4 to 3.6 V
- Up to 18 capacitive sensing channels supporting touchkeys, linear and rotary touch sensors
- Up to 11 timers
  - One 32-bit timer and one 16-bit timer with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - One 16-bit 6-channel advanced-control timer, with up to 6 PWM channels, deadtime generation and emergency stop
  - One 16-bit timer with 2 IC/OCs, 1 OCN/PWM, deadtime generation, emergency stop
  - Two 16-bit timers with IC/OC/OCN/PWM, deadtime generation and emergency stop
  - Two watchdog timers (independent, window)
  - SysTick timer: 24-bit downcounter
  - Up to two 16-bit basic timers to drive DAC
- Calendar RTC with alarm, periodic wakeup from Stop
- Communication interfaces
  - CAN interface (2.0 B Active) and one SPI
  - One I^2C with 20 mA current sink to support Fast mode plus, SMBus/PMBus
  - Up to 3 USARTs, one with ISO/IEC 7816 interface, LIN, IrDA, modem control
- Debug mode: serial wire debug (SWD), JTAG

- 96-bit unique ID
- All packages ECOPACK®2

Table 1. Device summary

Reference	Part number
STM32F303x6	STM32F303K6/C6/R6
STM32F303x8	STM32F303K8/C8/R8

Contents

List of tables

List of figures

1 Introduction

This datasheet provides the ordering information and the mechanical device characteristics of the STM32F303x6/8 microcontrollers.

This document should be read in conjunction with the STM32F303xx, STM32F358xx and STM32F328xx advanced ARM®-based 32-bit MCUs reference manual (RM00316) available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M4 core with FPU, refer to:

- ARM® Cortex®-M4 Processor Technical Reference Manual available from the www.arm.com website.
- STM32F3xxx and STM32F4xxx Cortex®-M4 programming manual (PM0214) available from the *www.st.com* website.

2 Description

The STM32F303x6/8 family incorporates the high-performance ARM® Cortex®-M4 32-bit RISC core operating at up to 72 MHz frequency embedding a floating point unit (FPU), high-speed embedded memories (up to 64 Kbytes of Flash memory, 12 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The STM32F303x6/8 microcontrollers offer up to two fast 12-bit ADCs (5 Msps), up to three ultra-fast comparators, an operational amplifier, three DAC channels, a low-power RTC, one general-purpose, 32-bit timer, one timer dedicated to motor control, and four general-purpose, 16-bit timers. They also feature standard and advanced communication interfaces: one I^2C, one SPI, up to three USARTs and one CAN.

The STM32F303x6/8 family operates in the –40 to +85 °C and –40 to +105 °C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F303x6/8 family offers devices in 32, and 64-pin packages.

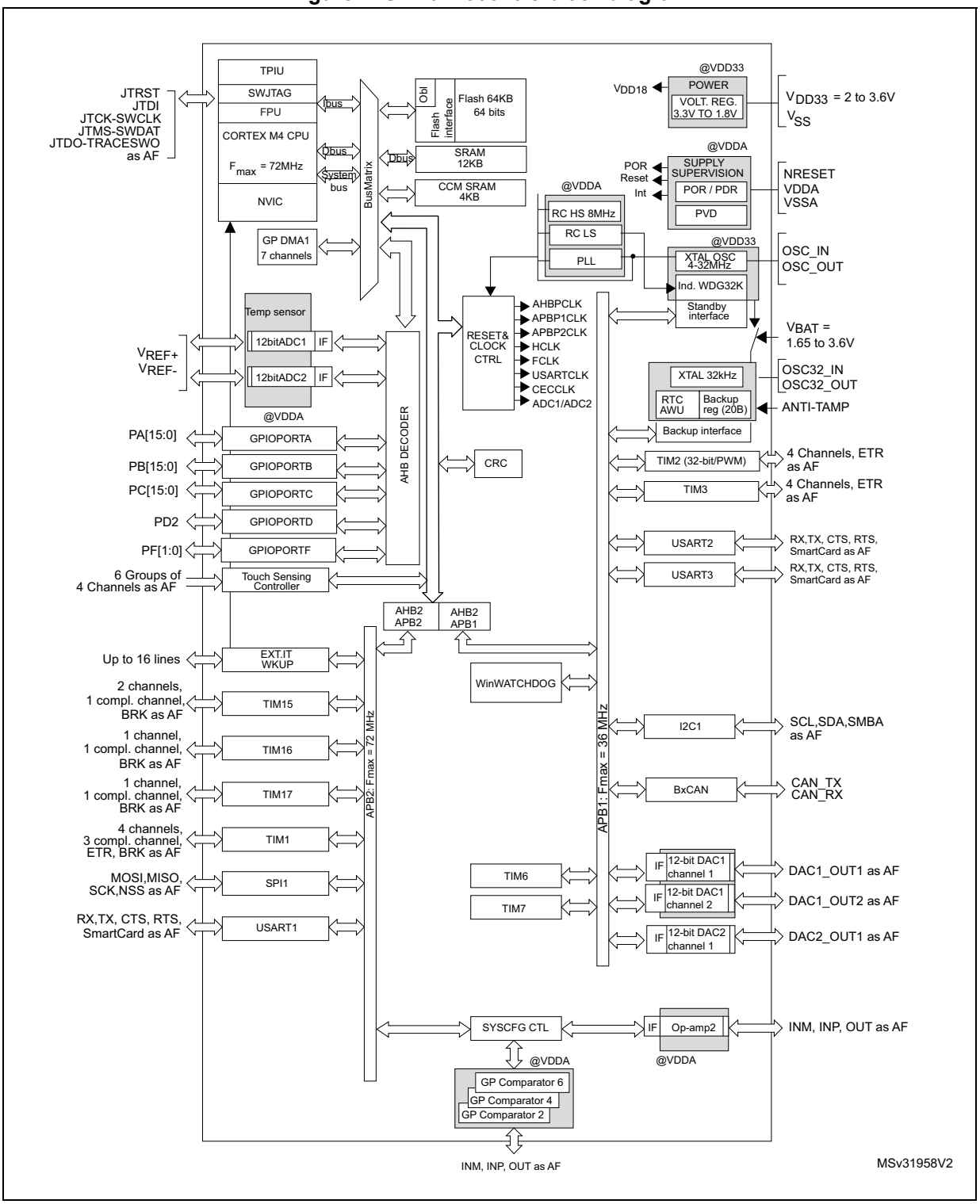
Depending on the device chosen, different sets of peripherals are included.

Table 2. STM32F303x6/8 family device features and peripherals count

Peripheral		STM32F303Kx		STM32F303Cx		STM32F303Rx	
Flash (Kbytes)		32	64	32	64	32	64
SRAM on data bus (Kbytes)		12					
Core coupled memory SRAM on instruction bus (CCM SRAM) (Kbytes)		4					
Timers	Advanced control	1 (16-bit)					
	General purpose	4 (16-bit) 1 (32 bit)					
	Basic	2 (16-bit)					
	SysTick timer	1					
	Watchdog timers (independent, window)	2					
	PWM channels (all)(1)	20		22		22	
	PWM channels (except complementary)	14		16		16	
Comm. interfaces	SPI	1					
	I^2C	1					
	USART	2		3		3	
	CAN	1					
GPIOs	Normal I/Os (TC, TTa)	10		20		26	
	5-Volt tolerant I/Os (FT,FTf)	15		17		25	
Capacitive sensing channels		14		17		18	
DMA channels		7					
12-bit ADCs Number of channels		2 9		2 15		2 21	
12-bit DAC channels		3					
Ultra-fast analog comparator		2		3			
Operational amplifiers		1					
CPU frequency		72 MHz					
Operating voltage		2.0 to 3.6 V					
Operating temperature		Ambient operating temperature: - 40 to 85 °C / - 40 to 105 °C Junction temperature: - 40 to 125 °C					
Packages		LQFP32		LQFP48		LQFP64	

1. This total considers also the PWMs generated on the complementary output channels.

Figure 1. STM32F303x6/8 block diagram



1. AF: alternate function on I/O pins.

3 Functional overview

3.1 ARM® Cortex®-M4 core with FPU with embedded Flash and SRAM

The ARM Cortex-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM 32-bit Cortex-M4 RISC processor with FPU features exceptional code-efficiency, delivering the high performance expected from an ARM core, with memory sizes usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allows efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32F303x6/8 family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32F303x6/8 family devices.

3.2 Memories

3.2.1 Embedded Flash memory

All STM32F303x6/8 devices feature up to 64 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

3.2.2 Embedded SRAM

The STM32F303x6/8 devices feature 12 Kbytes of embedded SRAM with hardware parity check. The memory can be accessed in read/write at CPU clock speed with 0 wait states, allowing the CPU to achieve 90 Dhrystone Mips at 72 MHz when running code from CCM (core coupled memory) RAM.

The SRAM is organized as follows:

- 4 Kbytes of SRAM on instruction and data bus with parity check (core coupled memory or CCM) and used to execute critical routines or to access data
- 12 Kbytes of SRAM with parity check mapped on the data bus.

3.2.3 Boot modes

At startup, BOOT0 pin and BOOT1 option bit are used to select one of the three boot options:

- Boot from user Flash memory
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART2 (PA2/PA3), I2C1 (PB6/PB7).

3.3 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.4 Power management

3.4.1 Power supply schemes

- V_{SS}, V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. It is provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supply for ADC, DACs, comparators operational amplifiers, reset blocks, RCs and PLL.The minimum voltage to be applied to V_{DDA} differs from one analog peripherals to another. See the *Table 3* below, summarizing the V_{DDA} ranges for analog peripherals. The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be provided first.
- V_{DD18} = 1.65 to 1.95 V (V_{DD18} domain): power supply for digital core, SRAM and Flash memory. V_{DD18} is internally generated through an internal voltage regulator.

Table 3. V_{DDA} ranges for analog peripherals

Analog peripheral	Min V_{DDA}supply	Max V_{DDA}supply
ADC/COMP	2 V	3.6 V
DAC/OPAMP	2.4 V	3.6 V

- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4.2 Power supply supervisor

The device has an integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device

remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.4.3 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR), and power-down.

- The MR mode is used in the nominal regulation mode (Run)
- The LPR mode is used in Stop mode.
- The power-down mode is used in Standby mode: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The voltage regulator is always enabled after reset. It is disabled in Standby mode.

3.4.4 Low-power modes

The STM32F303x6/8 supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm, COMPx, I^2C or USARTx.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.5 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Table 4. STM32F303x6/8 peripheral interconnect matrix

Interconnect source	Interconnect destination	Interconnect action
TIMx	TIMx	Timers synchronization or chaining
	ADCx DACx	Conversion triggers
	DMA	Memory to memory transfer trigger
	COMPx	Comparator output blanking
COMPx	TIMx	Timer input: ocrefclear input, input capture
ADCx	TIM1	Timer triggered by analog watchdog
GPIO RTCCLK HSE/32 MC0	TIM16	Clock source used as input channel for HSI and LSI calibration
CSS CPU (hard fault) RAM (parity error) COMPx PVD GPIO	TIM1 TIM15, 16, 17	Timer break
GPIO	TIMx	External trigger, timer break
	ADCx DACx	Conversion external trigger
DACx	COMPx	Comparator inverting input

Note: For more details about the interconnect actions, refer to the corresponding sections in the RM0364 reference manual.

3.6 Clocks and startup

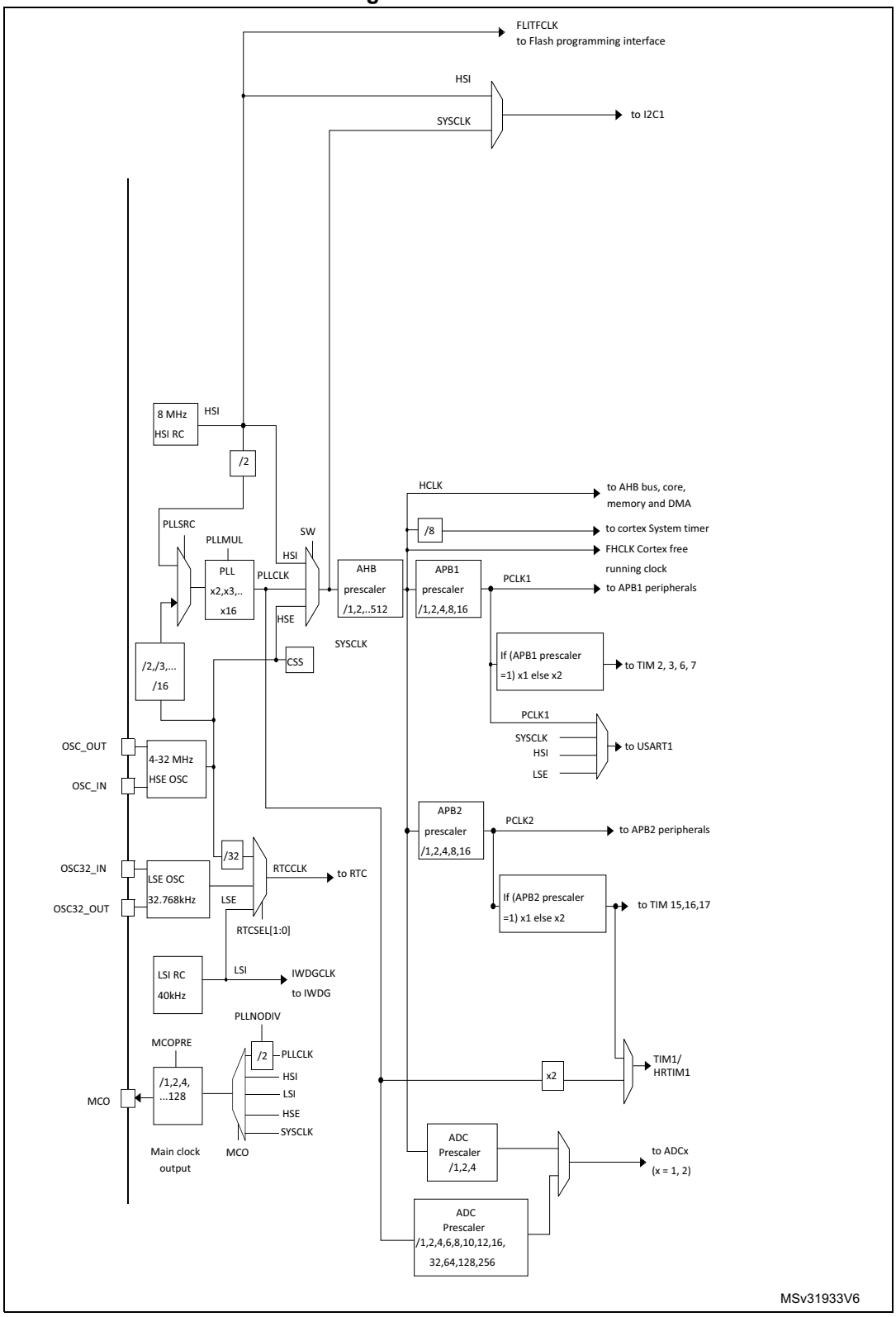
System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the

high-speed APB domains is 72 MHz, while the maximum allowed frequency of the low-speed APB domain is 36 MHz.

TIM1 maximum frequency is 144 MHz.

Figure 2. Clock tree



3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed, following a specific sequence to avoid spurious writing to the I/Os registers.

Fast I/O handling allows I/O toggling up to 36 MHz.

3.8 Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 7 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers, DAC and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F303x6/8 devices embed a nested vectored interrupt controller (NVIC) able to handle up to 60 interrupt channels, that can be masked and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The external interrupt/event controller consists of 27 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked

independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 51 GPIOs can be connected to the 16 external interrupt lines.

3.10 Fast analog-to-digital converter (ADC)

Two 5 MSPS fast analog-to-digital converters, with selectable resolution between 12 and 6 bit, are embedded in the STM32F303x6/8 family devices. The ADCs have up to 21 external channels. Some of the external channels are shared between ADC1 and ADC2, performing conversions in single-shot or scan modes. The channels can be configured to be either single-ended input or differential input. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADCs also have internal channels: temperature sensor connected to ADC1 channel 16, $V_{BAT}/2$ connected to ADC1 channel 17, voltage reference V_{REFINT} connected to both ADC1 and ADC2 channel 18 and VOPAMP2 connected to ADC2 channel 17.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single-shunt phase current reading techniques.

Three analog watchdogs are available per ADC. The ADC can be served by the DMA controller.

The analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIM2, TIM3, TIM6, TIM15) and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

3.10.2 Internal voltage reference (VREFINT)

The internal voltage reference (VREFINT) provides a stable (bandgap) voltage output for the ADC and Comparators. VREFINT is internally connected to the ADC1_IN18 and ADC2_IN18

input channels. The precise voltage of VREFINT is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

3.10.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC1_IN17. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.10.4 OPAMP2 reference voltage (VOPAMP2)

OPAMP2 reference voltage can be measured using ADC2 internal channel 17.

3.11 Digital-to-analog converter (DAC)

One 12-bit buffered DAC channel (DAC1_OUT1) and two 12-bit unbuffered DAC channels (DAC1_OUT2 and DAC2_OUT1) can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- Three DAC output channels
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation (only on DAC1)
- Triangular-wave generation (only on DAC1)
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion

3.12 Operational amplifier (OPAMP)

The STM32F303x6/8 embeds an operational amplifier (OPAMP2) with external or internal follower routing and PGA capability (or even amplifier and filter capability with external components). When an operational amplifier is selected, an external ADC channel is used to enable output measurement.

The operational amplifier features:

- 8 MHz GBP
- 0.5 mA output capability
- Rail-to-rail input/output
- In PGA mode, the gain can be programmed to 2, 4, 8 or 16.

3.13 Ultra-fast comparators (COMP)

The STM32F303x6/8 devices embed three ultra-fast rail-to-rail comparators (COMP2/4/6) which offer the features below:

- Programmable internal or external reference voltage
- Selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to *Table 24: Embedded internal reference voltage* for values and parameters of the internal reference voltage.

All comparators can wake up from STOP mode, generate interrupts and breaks for the timers.

3.14 Timers and watchdogs

The STM32F303x6/8 includes advanced control timer, 5 general-purpose timers, basic timer, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare Channels	Complementary outputs
Advanced control	TIM1(1)	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	Yes
General-purpose	TIM2	32-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

1. TIM1 can be clocked from the PLL x 2 running at up to 144 MHz when the system clock source is the PLL and AHB or APB2 subsystem clocks are not divided by more than 2 cumulatively.

3.14.1 Advanced timer (TIM1)

The advanced-control timer can be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timers (described in *Section 3.14.2* using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

3.14.2 General-purpose timers (TIM2, TIM3, TIM15, TIM16, TIM17)

There are up to three general-purpose timers embedded in the STM32F303x6/8 (see *Table 5* for differences), that can be synchronized. Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2 and TIM3

  They are full-featured general-purpose timers:

  – TIM2 has a 32-bit auto-reload up/down counter and 32-bit prescaler

  – TIM3 has a 16-bit auto-reload up/down counter and 16-bit prescaler

  These timers feature four independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.

- TIM15, 16 and 17

  They are three general-purpose timers with mid-range features.

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  – TIM15 has two channels and one complementary channel

  – TIM16 and TIM17 have one channel and one complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.14.3 Basic timers (TIM6 and TIM7)

The basic timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit timebases.

3.14.4 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.14.5 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.14.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.15 Real-time clock (RTC) and backup registers

The RTC and the 5 backup registers are supplied through a switch that takes power from either the V_{DD} supply when present or the VBAT pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.

They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms with wake up from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Two anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be

woken up from Stop and Standby modes on timestamp event detection.

- 17-bit Auto-reload counter for periodic interrupt with wakeup from STOP/STANDBY capability.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

3.16 Communication interfaces

3.16.1 Inter-integrated circuit interface (I^2C)

The devices feature an I^2C bus interface which can operate in multimaster and slave mode. It can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes.

It supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). It also includes programmable analog and digital noise filters.

Table 6. Comparison of I^2C analog and digital filters

-	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I^2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, it provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. It also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I^2C interface can be served by the DMA controller.

The features available in I2C1 are showed below in *Table 7*.

Table 7. STM32F303x6/8 I^2C implementation

I^2C features(1)	I2C1
7-bit addressing mode	X
10-bit addressing mode	X
Standard mode (up to 100 kbit/s)	X
Fast mode (up to 400 kbit/s)	X