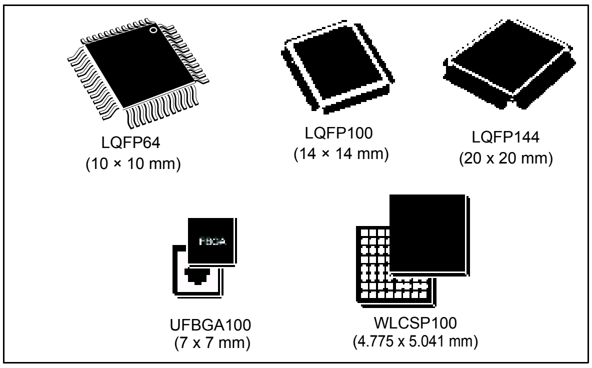
# STM32F303xD STM32F303xE

## ARM® Cortex®-M4 32b MCU+FPU, up to 512KB Flash, 80KB SRAM, FSMC, 4 ADCs, 2 DAC ch., 7 comp, 4 Op-Amp, 2.0-3.6 V

**Datasheet - production data**

## Features

- Core: ARM® Cortex®-M4 32-bit CPU with 72 MHz FPU, single-cycle multiplication and HW division, 90 DMIPS (from CCM), DSP instruction and MPU (memory protection unit)
- Operating conditions:
  - $V_{DD}$, $V_{DDA}$ voltage range: 2.0 V to 3.6 V
- Memories
  - Up to 512 Kbytes of Flash memory
  - 64 Kbytes of SRAM, with HW parity check implemented on the first 32 Kbytes.
  - Routine booster: 16 Kbytes of SRAM on instruction and data bus, with HW parity check (CCM)
  - Flexible memory controller (FSMC) for static memories, with four Chip Select
- CRC calculation unit
- Reset and supply management
  - Power-on/Power-down reset (POR/PDR)
  - Programmable voltage detector (PVD)
  - Low-power modes: Sleep, Stop and Standby
  - $V_{BAT}$ supply for RTC and backup registers
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC with x 16 PLL option
  - Internal 40 kHz oscillator
- Up to 115 fast I/Os
  - All mappable on external interrupt vectors
  - Several 5 V-tolerant
- Interconnect matrix
- 12-channel DMA controller
- Four ADCs 0.20 µs (up to 40 channels) with selectable resolution of 12/10/8/6 bits, 0 to 3.6 V conversion range, separate analog supply from 2.0 to 3.6 V




- Two 12-bit DAC channels with analog supply from 2.4 to 3.6 V
- Seven ultra-fast rail-to-rail analog comparators with analog supply from 2.0 to 3.6 V
- Four operational amplifiers that can be used in PGA mode, all terminals accessible with analog supply from 2.4 to 3.6 V
- Up to 24 capacitive sensing channels supporting touchkey, linear and rotary touch sensors
- Up to 14 timers:
  - One 32-bit timer and two 16-bit timers with up to four IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - Three 16-bit 6-channel advanced-control timers, with up to six PWM channels, deadtime generation and emergency stop
  - One 16-bit timer with two IC/OCs, one OCN/PWM, deadtime generation and emergency stop
  - Two 16-bit timers with IC/OC/OCN/PWM, deadtime generation and emergency stop
  - Two watchdog timers (independent, window)
  - One SysTick timer: 24-bit downcounter
  - Two 16-bit basic timers to drive the DAC
- Calendar RTC with Alarm, periodic wakeup from Stop/Standby
- Communication interfaces
  - CAN interface (2.0B Active)

 – Three $I^2C$ Fast mode plus (1 Mbit/s) with 20 mA current sink, SMBus/PMBus, wakeup from STOP
 – Up to five USART/UARTs (ISO 7816 interface, LIN, IrDA, modem control)
 – Up to four SPIs, 4 to 16 programmable bit frames, two with multiplexed half/full duplex $I^2S$ interface
 – USB 2.0 full-speed interface with LPM support
 – Infrared transmitter
- SWD, Cortex®-M4 with FPU ETM, JTAG
- 96-bit unique ID

**Table 1. Device summary**

| Reference | Part number |
|---|---|
| STM32F303xD | STM32F303RD, STM32F303VD, STM32F303ZD. |
| STM32F303xE | STM32F303RE, STM32F303VE, STM32F303ZE. |

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# 1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F303xD/E microcontrollers.

This STM32F303xD/E datasheet should be read in conjunction with the reference manual of STM32F303xB/C/D/E, STM32F358xC and STM32F328x4/6/8 devices (RM0316) available on STMicroelectronics website at *www.st.com*.

For information on the ARM® Cortex®-M4 core with FPU, refer to the following documents:

- *Cortex® -M4 with FPU Technical Reference Manual*, available from the www.arm.com website
- *STM32F3 and STM32F4 Series Cortex® -M4 programming manual* (PM0214) available on STMicroelectronics website at *www.st.com*.

# 2 Description

The STM32F303xD/E family is based on the high-performance ARM® Cortex®-M4 32-bit RISC core with FPU operating at a frequency of 72 MHz, and embedding a floating point unit (FPU), a memory protection unit (MPU) and an embedded trace macrocell (ETM). The family incorporates high-speed embedded memories (512-Kbyte Flash memory, 80-Kbyte SRAM), a flexible memory controller (FSMC) for static memories (SRAM, PSRAM, NOR and NAND), and an extensive range of enhanced I/Os and peripherals connected to an AHB and two APB buses.

The devices offer four fast 12-bit ADCs (5 Msps), seven comparators, four operational amplifiers, two DAC channels, a low-power RTC, up to five general-purpose 16-bit timers, one general-purpose 32-bit timer, and up,to three timers dedicated to motor control. They also feature standard and advanced communication interfaces: up to three $I^2$Cs, up to four SPIs (two SPIs are with multiplexed full-duplex $I^2$Ss), three USARTs, up to two UARTs, CAN and USB. To achieve audio class accuracy, the $I^2$S peripherals can be clocked via an external PLL.

The STM32F303xD/E family operates in the -40 to +85°C and -40 to +105°C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F303xD/E family offers devices in different packages ranging from 64 to 144 pins.

Depending on the device chosen, different sets of peripherals are included.

**Table 2. STM32F303xD/E family device features and peripheral counts**

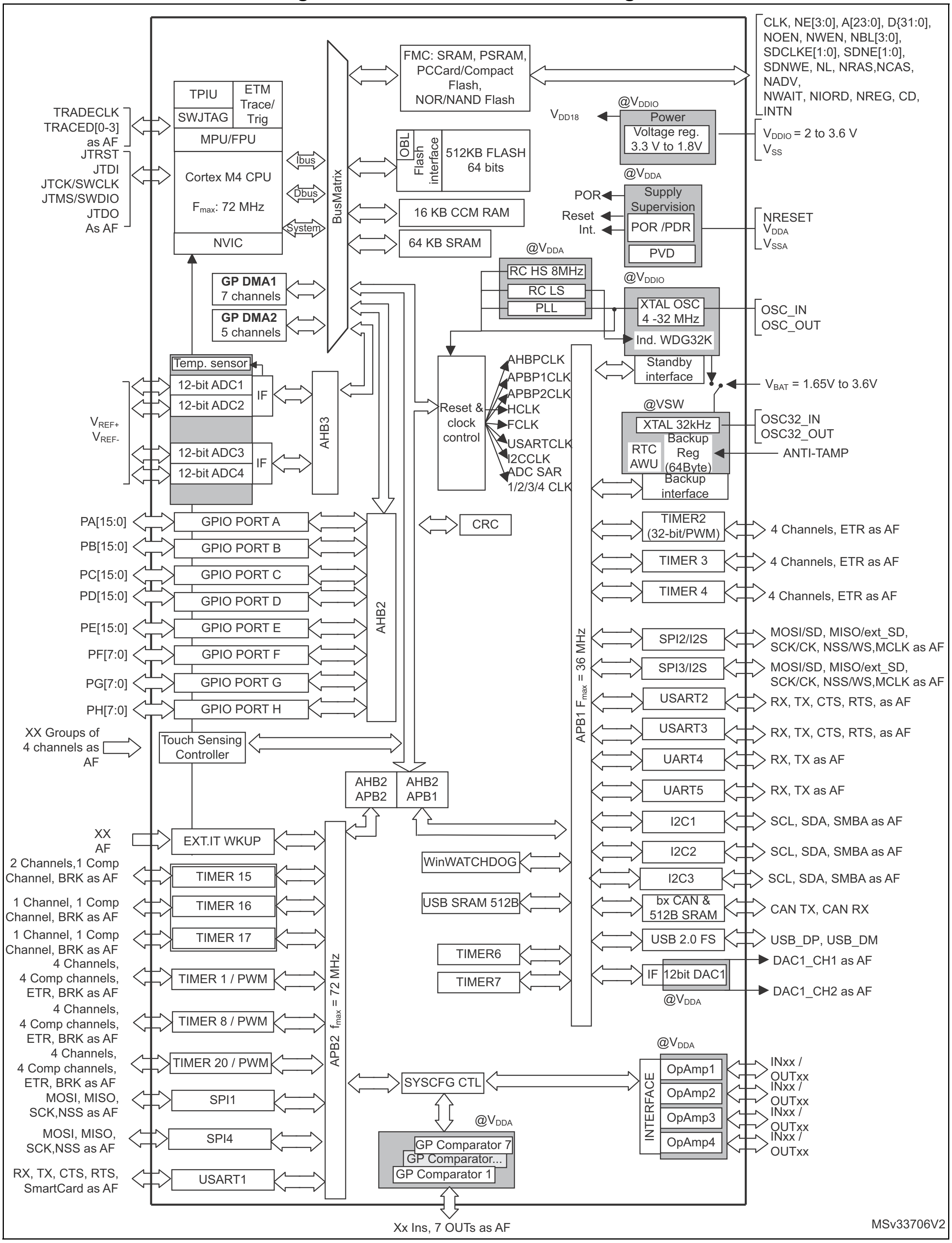
| Peripheral | | STM32F303Rx | | STM32F303Vx | | STM32F303Zx | |
|---|---|---|---|---|---|---|---|
| Flash (Kbytes) | | 384 | 512 | 384 | 512 | 384 | 512 |
| SRAM (Kbytes) on data bus | | 64 | | | | | |
| CCM (Core Coupled Memory) RAM (Kbytes) | | 16 | | | | | |
| FMC (flexible memory controller) | | NO | | YES | | | |
| Timers | Advanced control | 2 (16-bit)(1) | | 3 (16-bit) | | | |
| | General purpose | 5 (16-bit)<br>1 (32-bit) | | | | | |
| | PWM channels (all) (2) | 31 | | 40 | | 40 | |
| | Basic | 2 (16-bit) | | | | | |
| | PWM channels (except complementary) | 22 | | 28 | | 28 | |
| Communication interfaces | SPI ($I^2S$)(3) | 4(2) | | | | | |
| | $I^2C$ | 3 | | | | | |
| | USART | 3 | | | | | |
| | UART | 2 | | | | | |
| | CAN | 1 | | | | | |
| | USB | 1 | | | | | |
| GPIOs | Normal I/Os (TC, TTa) | 26 | | 37 in WLCSP100,44 in LQFP100 and UFBGA100 | | 45 | |
| | 5-volt tolerant I/Os (FT, FTf) | 25 | | 42 in LQFP100<br>40 in WLCSP100 and UFBGA100 | | 70 | |
| DMA channels | | 12 | | | | | |
| Capacitive sensing channels | | 18 | | 24 | | | |
| 12-bit ADCs | | 4<br>22 channels | | 4<br>39 channels in LQFP100-pin and UFBGA100<br>33 channels in WLCSP100 | | 4<br>40 channels | |
| 12-bit DAC channels | | | | | | | |
| Analog comparator | | | | | | | |
| Operational amplifiers | | | | | | | |
| CPU frequency | | 72 MHz | | | | | |
| Operating voltage | | 2.0 to 3.6 V | | | | | |

**Table 2. STM32F303xD/E family device features and peripheral counts (continued)**

| Peripheral | STM32F303Rx | STM32F303Vx | STM32F303Zx |
|---|---|---|---|
| Operating temperature | Ambient operating temperature: - 40 to 85 °C / - 40 to 105 °C<br>Junction temperature: - 40 to 125 °C | | |
| Packages | LQFP64 | LQFP100<br>WLCSP100<br>UFBGA100 | LQFP144 |

1. TIM1 and TIM8 are the two available advanced timers.
2. This total number considers also the PWMs generated on the complementary output channels.
3. The SPI interfaces works in an exclusive way in either the SPI mode or the $I^2S$ audio mode.

**Figure 1. STM32F303xD/E block diagram**




1. AF: alternate function on I/O pins.

# 3 Functional overview

## 3.1 ARM® Cortex®-M4 core with FPU with embedded Flash and SRAM

The ARM® Cortex®-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 32-bit RISC processor with FPU features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allows efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32F303xD/E family is compatible with all ARM tools and software.

*Figure 1* shows the general block diagram of the STM32F303xD/E family devices.

## 3.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU manage up to 8 protection areas that are further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS detects it and takes action. In an RTOS environment, the kernel dynamically updates the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

## 3.3 Embedded Flash memory

All STM32F303xD/E devices feature 384/512 Kbyte of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

## 3.4 Embedded SRAM

STM32F303xD/E devices feature 80 Kbytes of embedded SRAM with hardware parity check. The memory can be accessed in read/write at CPU clock speed with 0 wait states, allowing the CPU to achieve 90 Dhrystone MIPS at 72 MHz (when running code from the CCM (Core Coupled Memory) RAM).

- 16 Kbytes of CCM SRAM mapped on both instruction and data bus, used to execute critical routines or to access data (parity check on all of CCM SRAM).
- 64 Kbytes of SRAM mapped on the data bus (parity check on first 32 Kbytes of SRAM).

## 3.5 Boot modes

At startup, Boot0 pin and Boot1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in the system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART2 (PA2/PA3) or USB (PA11/PA12) through DFU (device firmware upgrade).

## 3.6 Cyclic redundancy check (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

## 3.7 Power management

### 3.7.1 Power supply schemes

- $V_{SS}$, $V_{DD}$ = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. It is provided externally through $V_{DD}$ pins.
- $V_{SSA}$, $V_{DDA}$ = 2.0 to 3.6 V: external analog power supply for ADC, DAC, comparators, operational amplifier, reset blocks, RCs and PLL. The minimum voltage to be applied to $V_{DDA}$ differs from one analog peripheral to another. *Table 3* provides the summary of the $V_{DDA}$ ranges for analog peripherals. The $V_{DDA}$ voltage level must always be greater than or equal to the $V_{DD}$ voltage level and must be provided first.

**Table 3. External analog supply values for analog peripherals**

| Analog peripheral | Minimum $V_{DDA}$ supply | Maximum $V_{DDA}$ supply |
|---|---|---|
| ADC/COMP | 2.0 V | 3.6 V |
| DAC/OPAMP | 2.4 V | 3.6 V |

- $V_{BAT}$ = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when $V_{DD}$ is not present.

### 3.7.2 Power supply supervisor

The device has an integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the $V_{DD}$ supply voltage. During the startup phase it is required that $V_{DDA}$ should arrive first and be greater than or equal to $V_{DD}$.
- The PDR monitors both the $V_{DD}$ and $V_{DDA}$ supply voltages, however the $V_{DDA}$ power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that $V_{DDA}$ is higher than or equal to $V_{DD}$.

The device features an embedded programmable voltage detector (PVD) that monitors the $V_{DD}$ power supply and compares it to the $V_{PVD}$ threshold. An interrupt can be generated when $V_{DD}$ drops below the $V_{PVD}$ threshold and/or when $V_{DD}$ is higher than the $V_{PVD}$ threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

### 3.7.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR), and power-down.

- The MR mode is used in the nominal regulation mode (Run)
- The LPR mode is used in Stop mode.
- The power-down mode is used in Standby mode: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The voltage regulator is always enabled after reset. It is disabled in Standby mode.

### 3.7.4 Low-power modes

The STM32F303xD/E supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- Sleep mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and wake up the CPU when an interrupt/event occurs.
- Stop mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the USB wakeup, the RTC alarm, COMPx, I2Cx or U(S)ARTx.
- Standby mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin or an RTC alarm occurs.

*Note: The RTC, the IWDG and the corresponding clock sources are not stopped by entering Stop or Standby mode.*

## 3.8 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

**Table 4. STM32F303xD/E peripheral interconnect matrix**

| Interconnect source | Interconnect destination | Interconnect action |
|---|---|---|
| TIMx | TIMx | Timers synchronization or chaining |
| | ADCx<br>DAC1 | Conversion triggers |
| | DMA | Memory to memory transfer trigger |
| | Compx | Comparator output blanking |
| COMPx | TIMx | Timer input: OCREF_CLR input, input capture |
| ADCx | TIMx | Timer triggered by analog watchdog |

**Table 4. STM32F303xD/E peripheral interconnect matrix (continued)**

| Interconnect source | Interconnect destination | Interconnect action |
|---|---|---|
| GPIO<br>RTCCLK<br>HSE/32<br>MC0 | TIM16 | Clock source used as input channel for HSI and LSI calibration |
| CSS<br>CPU (hard fault)<br>COMPx<br>GPIO | TIM1, TIM8, TIM20<br>TIM15, 16, 17 | Timer break |
| GPIO | TIMx | External trigger, timer break |
| | ADCx<br>DAC1 | Conversion external trigger |
| DAC1 | COMPx | Comparator inverting input |

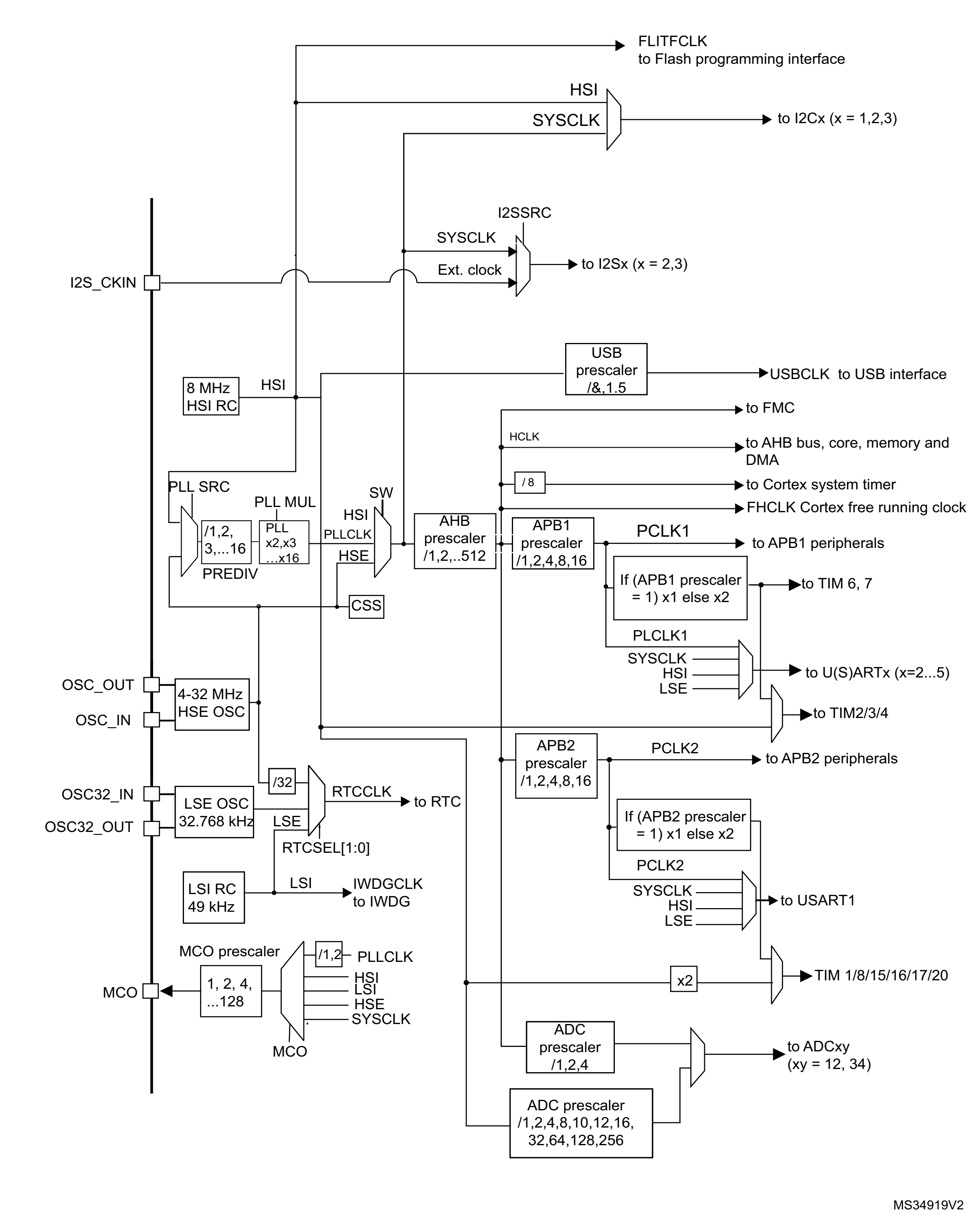
*Note: For more details about the interconnect actions, refer to the corresponding sections in the STM32F303xD/Ereference manual (RM0316).*

## 3.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

**Figure 2. STM32F303xD/E clock tree**



## 3.10 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence to avoid spurious writing to the I/Os registers.

Fast I/O handling allows I/O toggling up to 36 MHz.

## 3.11 Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 12 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA is used with the main peripherals: SPI, $I^2C$, USART, general-purpose timers, DAC and ADC.

## 3.12 Flexible static memory controller (FSMC)

The flexible static memory controller (FSMC) includes two memory controllers:

- The NOR/PSRAM memory controller,
- The NAND/PC Card memory controller.

This memory controller is also named Flexible memory controller (FMC).

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM),
  - NOR Flash memory/OneNAND Flash memory,
  - PSRAM (four memory banks),
  - NAND Flash memory with ECC hardware to check up to 8 Kbyte of data,
  - 16-bit PC Card compatible devices.
- 8-,16-bit data bus width,
- Independent Chip Select control for each memory bank,
- Independent configuration for each memory bank,
- Write FIFO,
- LCD parallel interface.

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

## 3.13 Interrupts and events

### 3.13.1 Nested vectored interrupt controller (NVIC)

The STM32F303xD/E devices embed a nested vectored interrupt controller (NVIC) able to handle up to 73 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

## 3.14 Fast analog-to-digital converter (ADC)

Four fast analog-to-digital converters 5 MSPS, with selectable resolution between 12 and 6 bit, are embedded in the STM32F303xD/E family devices. The ADCs have up to 40 external channels. Some of the external channels are shared between ADC1&2 and between ADC3&4. The ADCs can perform conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADCs have also internal channels: Temperature sensor connected to ADC1 channel 16, VBAT/2 connected to ADC1 channel 17, Voltage reference VREFINT connected to the 4 ADCs channel 18, VREFOPAMP1 connected to ADC1 channel 15, VREFOPAMP2 connected to ADC2 channel 17, VREFOPAMP3 connected to ADC3 channel 17 and VREFOPAMP4 connected to ADC4 channel 17.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single-shunt phase current reading techniques.

The ADC can be served by the DMA controller.

Three analog watchdogs are available per ADC.

The analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers and the advanced-control timers (TIM1, TIM8 and TIM20) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

### 3.14.1 Temperature sensor

The temperature sensor (TS) generates a voltage $V_{SENSE}$ that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

### 3.14.2 Internal voltage reference ($V_{REFINT}$)

The internal voltage reference ($V_{REFINT}$) provides a stable (bandgap) voltage output for the ADC and Comparators. $V_{REFINT}$ is internally connected to the ADCx_IN18, x=1...4 input channel. The precise voltage of $V_{REFINT}$ is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

### 3.14.3 $V_{BAT}$ battery voltage monitoring

This embedded hardware feature allows the application to measure the $V_{BAT}$ battery voltage using the internal ADC channel ADC1_IN17. As the $V_{BAT}$ voltage may be higher than $V_{DDA}$, and thus outside the ADC input range, the $V_{BAT}$ pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the $V_{BAT}$ voltage.

### 3.14.4 OPAMP reference voltage (VREFOPAMP)

Every OPAMP reference voltage can be measured using a corresponding ADC internal channel: VREFOPAMP1 connected to ADC1 channel 15, VREFOPAMP2 connected to ADC2 channel 17, VREFOPAMP3 connected to ADC3 channel 17 and VREFOPAMP4 connected to ADC4 channel 17.

## 3.15 Digital-to-analog converter (DAC)

Two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- Two DAC output channels
- 8-bit or 10-bit monotonic output

- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability (for each channel)
- External triggers for conversion
- Input voltage reference VREF+

## 3.16 Operational amplifier (OPAMP)

The STM32F303xD/E embed four operational amplifiers with external or internal follower routing and PGA capability (or even amplifier and filter capability with external components). When an operational amplifier is selected, an external ADC channel is used to enable output measurement.

The operational amplifier features:

- 8.2 MHz bandwidth
- 0.5 mA output capability
- Rail-to-rail input/output
- In PGA mode, the gain is programmed to be 2, 4, 8 or 16.

## 3.17 Ultra-fast comparators (COMP)

The STM32F303xD/E devices embed seven ultra-fast rail-to-rail comparators with programmable reference voltage (internal or external) and selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pin
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to *Table 23: Embedded internal reference voltage* for the value and precision of the internal reference voltage.

All comparators can wake up from STOP mode, generate interrupts and breaks for the timers.

## 3.18 Timers and watchdogs

The STM32F303xD/E include three advanced control timers, up to six general-purpose timers, two basic timers, two watchdog timers and one SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.