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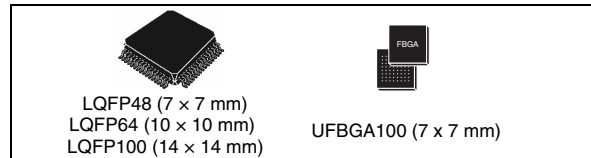
STM32F372xx STM32F373xx

ARM Cortex-M4F 32b MCU+FPU, up to 256KB Flash+32KB SRAM
timers, 4 ADCs (12/16-bit), 3 DACs, 2 comp., 2.0-3.6 V operation

Datasheet – production data

Features

- Core: ARM 32-bit Cortex™-M4F CPU (72 MHz max), single-cycle multiplication and HW division, DSP instruction with FPU (floating-point unit) and MPU (memory protection unit)
- Memories
 - 64 to 256 Kbytes of Flash memory
 - 32 Kbytes of SRAM with HW parity check
- CRC calculation unit
- Reset and power management
 - Voltage range: 2.0 to 3.6 V
 - Power-on/Power down reset (POR/PDR)
 - Programmable voltage detector (PVD)
 - Low power modes: Sleep, Stop, Standby
 - V_{BAT} supply for RTC and backup registers
- Clock management
 - 4 to 32 MHz crystal oscillator
 - 32 kHz oscillator for RTC with calibration
 - Internal 8 MHz RC with x16 PLL option
 - Internal 40 kHz oscillator
- Up to 84 fast I/Os
 - All mappable on external interrupt vectors
 - Up to 45 I/Os with 5 V tolerant capability
- 12-channel DMA controller
- One 12-bit, 1.0 μs ADC (up to 16 channels)
 - Conversion range: 0 to 3.6 V
 - Separate analog supply from 2.4 up to 3.6
- Up to three 16-bit Sigma Delta ADC
 - Separate analog supply from 2.2 to 3.6 V, up to 21 single/ 11 diff channels
- Up to three 12-bit DAC channels
- Two fast rail-to-rail analog comparators with programmable input and output
- Up to 24 capacitive sensing channels supporting touchkey, linear and rotary touchsensors



- 17 timers
 - Two 32-bit timer and three 16-bit timers with up to 4 IC/OC/PWM or pulse counter
 - Two 16-bit timers with up to 2 IC/OC/PWM or pulse counter
 - Four 16-bit timers with up to 1 IC/OC/PWM or pulse counter
 - Independent and system watchdog timers
 - SysTick timer: 24-bit downcounter
 - Three 16-bit basic timers to drive the DAC
- Calendar RTC with Alarm and periodic wakeup from Stop/Standby
- Communication interfaces
 - CAN interface (2.0B Active)
 - Two I²C interfaces; supporting Fast Mode Plus (1 Mbit/s) with 20 mA current sink, SMBus/PMBus, wakeup from STOP
 - Three USARTs supporting master synchronous SPI and modem control; with ISO7816 interface, LIN, IrDA capability, auto baud rate detection, wakeup feature
 - Three SPIs (18 Mbit/s) with 4 to 16 programmable bit frame, muxed I2S
 - HDMI-CEC bus interface
 - USB 2.0 full speed interface
- Serial wire devices, JTAG, Cortex-M4F ETM
- 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM32F372xx	STM32F372C8, STM32F372R8, STM32F372V8, STM32F372CB, STM32F372RB, STM32F372VB, STM32F372CC, STM32F372RC, STM32F372VC
STM32F373xx	STM32F373C8, STM32F373R8, STM32F373V8, STM32F373CB, STM32F373RB, STM32F373VB, STM32F373CC, STM32F373RC, STM32F373VC

Contents

1	Introduction	8
2	Description	9
3	Functional overview	12
3.1	ARM® Cortex™-M4F core with embedded Flash and SRAM	12
3.2	Memory protection unit	12
3.3	Embedded Flash memory	13
3.4	Cyclic redundancy check (CRC) calculation unit	13
3.5	Embedded SRAM	13
3.6	Boot modes	13
3.7	Power management	14
3.7.1	Power supply schemes	14
3.7.2	Power supply supervisor	14
3.7.3	Voltage regulator	14
3.7.4	Low-power modes	15
3.8	Clocks and startup	15
3.9	General-purpose input/outputs (GPIOs)	15
3.10	Direct memory access (DMA)	16
3.11	Interrupts and events	16
3.11.1	Nested vectored interrupt controller (NVIC)	16
3.11.2	Extended interrupt/event controller (EXTI)	16
3.12	12-bit analog-to-digital converter (ADC)	17
3.12.1	Temperature sensor	17
3.12.2	Internal voltage reference (V_{REFINT})	17
3.12.3	V_{BAT} battery voltage monitoring	17
3.13	16-bit sigma delta analog-to-digital converters (SDADC)	18
3.14	Digital-to-analog converter (DAC)	19
3.15	Fast comparators (COMP)	19
3.16	Touch sensing controller (TSC)	20
3.17	Timers and watchdogs	21
3.17.1	General-purpose timers (TIM2 to TIM5, TIM12 to TIM17, TIM19)	22

3.17.2	Basic timers (TIM6, TIM7, TIM18)	22
3.17.3	Independent watchdog (IWDG)	23
3.17.4	System window watchdog (WWDG)	23
3.17.5	SysTick timer	23
3.18	Real-time clock (RTC) and backup registers	23
3.19	Inter-integrated circuit interface (I ² C)	24
3.20	Universal synchronous/asynchronous receiver transmitter (USART)	25
3.21	Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I ² S)	25
3.22	High-definition multimedia interface (HDMI) - consumer electronics control (CEC)	26
3.23	Controller area network (CAN)	26
3.24	Universal serial bus (USB)	26
3.25	Serial wire JTAG debug port (SWJ-DP)	27
3.26	Embedded trace macrocell™	27
4	Pinouts and pin description	28
5	Memory mapping	46
6	Electrical characteristics	50
6.1	Parameter conditions	50
6.1.1	Minimum and maximum values	50
6.1.2	Typical values	50
6.1.3	Typical curves	50
6.1.4	Loading capacitor	50
6.1.5	Pin input voltage	50
6.1.6	Power supply scheme	51
6.1.7	Current consumption measurement	52
6.2	Absolute maximum ratings	53
6.3	Operating conditions	55
6.3.1	General operating conditions	55
6.3.2	Operating conditions at power-up / power-down	56
6.3.3	Embedded reset and power control block characteristics	57
6.3.4	Embedded reference voltage	58
6.3.5	Supply current characteristics	59
6.3.6	Wakeup time from low-power mode	70

6.3.7	External clock source characteristics	70
6.3.8	Internal clock source characteristics	75
6.3.9	PLL characteristics	76
6.3.10	Memory characteristics	77
6.3.11	EMC characteristics	78
6.3.12	Electrical sensitivity characteristics	79
6.3.13	I/O current injection characteristics	80
6.3.14	I/O port characteristics	82
6.3.15	NRST characteristics	87
6.3.16	Communications interfaces	89
6.3.17	12-bit ADC characteristics	96
6.3.18	DAC electrical specifications	99
6.3.19	Comparator characteristics	101
6.3.20	Temperature sensor characteristics	103
6.3.21	V _{BAT} monitoring characteristics	103
6.3.22	Timer characteristics	103
6.3.23	USB characteristics	105
6.3.24	CAN (controller area network) interface	106
6.3.25	SDADC characteristics	106
7	Package characteristics	113
7.1	Package mechanical data	113
7.2	Thermal characteristics	121
7.2.1	Reference document	121
7.2.2	Selecting the product temperature range	122
8	Part numbering	124
9	Revision history	125

List of tables

Table 1.	Device summary	1
Table 2.	Device overview	10
Table 3.	Capacitive sensing GPIOs available on STM32F37x devices	20
Table 4.	No. of capacitive sensing channels available on STM32F37x devices.	21
Table 5.	Timer feature comparison.	21
Table 6.	Comparison of I ² C analog and digital filters	24
Table 7.	STM32F37x I ² C implementation.	24
Table 8.	STM32F37x USART implementation	25
Table 9.	STM32F37x SPI/I2S implementation	26
Table 10.	Legend/abbreviations used in the pinout table	32
Table 11.	STM32F37x pin definitions	32
Table 12.	Alternate functions for port PA	39
Table 13.	Alternate functions for port PB	41
Table 14.	Alternate functions for port PC	42
Table 15.	Alternate functions for port PD	43
Table 16.	Alternate functions for port PE	44
Table 17.	Alternate functions for port PF	45
Table 18.	STM32F37x peripheral register boundary addresses.	47
Table 19.	Voltage characteristics	53
Table 20.	Current characteristics	54
Table 21.	Thermal characteristics.	54
Table 22.	General operating conditions	55
Table 23.	Operating conditions at power-up / power-down	56
Table 24.	Embedded reset and power control block characteristics.	57
Table 25.	Programmable voltage detector characteristics	57
Table 26.	Embedded internal reference voltage calibration values	58
Table 27.	Embedded internal reference voltage.	58
Table 28.	Typical and maximum current consumption from V _{DD} supply at V _{DD} = 3.6 V	59
Table 29.	Typical and maximum current consumption from V _{DDA} supply	61
Table 30.	Typical and maximum V _{DD} consumption in Stop and Standby modes.	61
Table 31.	Typical and maximum V _{DDA} consumption in Stop and Standby modes.	62
Table 32.	Typical and maximum current consumption from V _{BAT} supply.	62
Table 33.	Typical current consumption in Run mode, code with data processing running from Flash	64
Table 34.	Typical current consumption in Sleep mode, code running from Flash or RAM.	65
Table 35.	Switching output I/O current consumption	67
Table 36.	Peripheral current consumption	68
Table 37.	Low-power mode wakeup timings	70
Table 38.	High-speed external user clock characteristics.	70
Table 39.	Low-speed external user clock characteristics	71
Table 40.	HSE oscillator characteristics	72
Table 41.	LSE oscillator characteristics (f _{LSE} = 32.768 kHz)	74
Table 42.	HSI oscillator characteristics.	75
Table 43.	LSI oscillator characteristics	76
Table 44.	PLL characteristics	76
Table 45.	Flash memory characteristics	77
Table 46.	Flash memory endurance and data retention.	77
Table 47.	EMS characteristics	78
Table 48.	EMI characteristics	79

Table 49.	ESD absolute maximum ratings	79
Table 50.	Electrical sensitivities	80
Table 51.	I/O current injection susceptibility	81
Table 52.	I/O static characteristics	82
Table 53.	Output voltage characteristics	85
Table 54.	I/O AC characteristics	86
Table 55.	NRST pin characteristics	87
Table 56.	I ² C characteristics	89
Table 57.	I ² C analog filter characteristics	90
Table 58.	SPI characteristics	91
Table 59.	I ² S characteristics	94
Table 60.	ADC characteristics	96
Table 61.	R _{SRC} max for f _{ADC} = 14 MHz	97
Table 62.	ADC accuracy	97
Table 63.	DAC characteristics	99
Table 64.	Comparator characteristics	101
Table 65.	Temperature sensor calibration values	103
Table 66.	TS characteristics	103
Table 67.	V _{BAT} monitoring characteristics	103
Table 68.	TIMx characteristics	104
Table 69.	IWDG min/max timeout period at 40 kHz (LSI)	104
Table 70.	WWDG min-max timeout value @72 MHz (PCLK)	104
Table 71.	USB startup time	105
Table 72.	USB DC electrical characteristics	105
Table 73.	USB: Full-speed electrical characteristics	106
Table 74.	SDADC characteristics	106
Table 75.	VREFSD+ pin characteristics	112
Table 76.	UFPGA100 – ultra fine pitch ball grid array, 7 x 7 mm, 0.50 mm pitch, package mechanical data	114
Table 77.	LQPF100 – 14 x 14 mm low-profile quad flat package mechanical data	115
Table 78.	LQFP64 – 10 x 10 mm low-profile quad flat package mechanical data	117
Table 79.	LQFP48 – 7 x 7 mm, low-profile quad flat package mechanical data	119
Table 80.	Package thermal characteristics	121
Table 81.	Ordering information scheme	124
Table 82.	Document revision history	125

List of figures

Figure 1.	Block diagram	11
Figure 2.	STM32F37x LQFP48 pinout	28
Figure 3.	STM32F37x LQFP64 pinout	29
Figure 4.	STM32F37x LQFP100 pinout	30
Figure 5.	STM32F37x BGA100 pinout	31
Figure 6.	STM32F37x memory map	46
Figure 7.	Pin loading conditions	50
Figure 8.	Pin input voltage	50
Figure 9.	Power supply scheme	51
Figure 10.	Current consumption measurement scheme	52
Figure 11.	Typical V_{BAT} current consumption (LSE and RTC ON/LSEDRV[1:0]='00')	63
Figure 12.	High-speed external clock source AC timing diagram	71
Figure 13.	Low-speed external clock source AC timing diagram	72
Figure 14.	Typical application with an 8 MHz crystal	73
Figure 15.	Typical application with a 32.768 kHz crystal	75
Figure 16.	HSI oscillator accuracy characterization results	76
Figure 17.	TC and TTA I/O input characteristics - CMOS port	83
Figure 18.	TC and TTA I/O input characteristics - TTL port	83
Figure 19.	Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port	84
Figure 20.	Five volt tolerant (FT and FTf) I/O input characteristics - TTL port	84
Figure 21.	I/O AC characteristics definition	87
Figure 22.	Recommended NRST pin protection	88
Figure 23.	I ² C bus AC waveforms and measurement circuit	90
Figure 24.	SPI timing diagram - slave mode and CPHA = 0	92
Figure 25.	SPI timing diagram - slave mode and CPHA = 1 ⁽¹⁾	92
Figure 26.	SPI timing diagram - master mode ⁽¹⁾	93
Figure 27.	I ² S slave timing diagram (Philips protocol) ⁽¹⁾	95
Figure 28.	I ² S master timing diagram (Philips protocol) ⁽¹⁾	95
Figure 29.	ADC accuracy characteristics	98
Figure 30.	Typical connection diagram using the ADC	98
Figure 31.	12-bit buffered /non-buffered DAC	100
Figure 32.	USB timings: definition of data signal rise and fall time	106
Figure 33.	UFPGA100 – ultra fine pitch ball grid array, 7 x 7 mm, 0.50 mm pitch, package outline	114
Figure 34.	LQFP100 –14 x 14 mm 100-pin low-profile quad flat package outline	115
Figure 35.	Recommended footprint	116
Figure 36.	LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline	117
Figure 37.	Recommended footprint	118
Figure 38.	LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package outline	119
Figure 39.	Recommended footprint	120
Figure 40.	LQFP64 P _D max vs. T _A	123

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F37x microcontrollers.

This STM32F37x datasheet should be read in conjunction with the STM32F37x reference manual. The reference manual is available from the STMicroelectronics website www.st.com.

For information on the Cortex™-M4F core please refer to the Cortex™-M4F Technical Reference Manual, available from the www.arm.com website at the following address: <http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.subset.cortexm.m4/index.html> and also refer to the STM32F3xxx and STM32F4xxx Cortex-M4 programming manual (PM0214) at address: http://www.st.com/internet/com/TECHNICAL_RESOURCES/TECHNICAL_LITERATURE/PROGRAMMING_MANUAL/DM00046982.pdf



2 Description

The STM32F37x family is based on the high-performance ARM® Cortex™-M4F 32-bit RISC core operating at a frequency of up to 72 MHz, and embedding a floating point unit (FPU), a memory protection unit (MPU) and an embedded trace macrocell (ETM). The family incorporates high-speed embedded memories (up to 256 Kbyte of Flash memory, up to 32 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The STM32F37x devices offer one fast 12-bit ADC (1 Msps), up to three 16-bit Sigma delta ADCs, up to two comparators, up to two DACs (DAC1 with 2 channels and DAC2 with 1 channel), a low-power RTC, 9 general-purpose 16-bit timers, two general-purpose 32-bit timers, three basic timers.

They also feature standard and advanced communication interfaces: up to two I2Cs, three SPIs, all with muxed I2Ss, three USARTs, CAN and USB.

The STM32F37x family operates in the -40 to +85 °C and -40 to +105 °C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

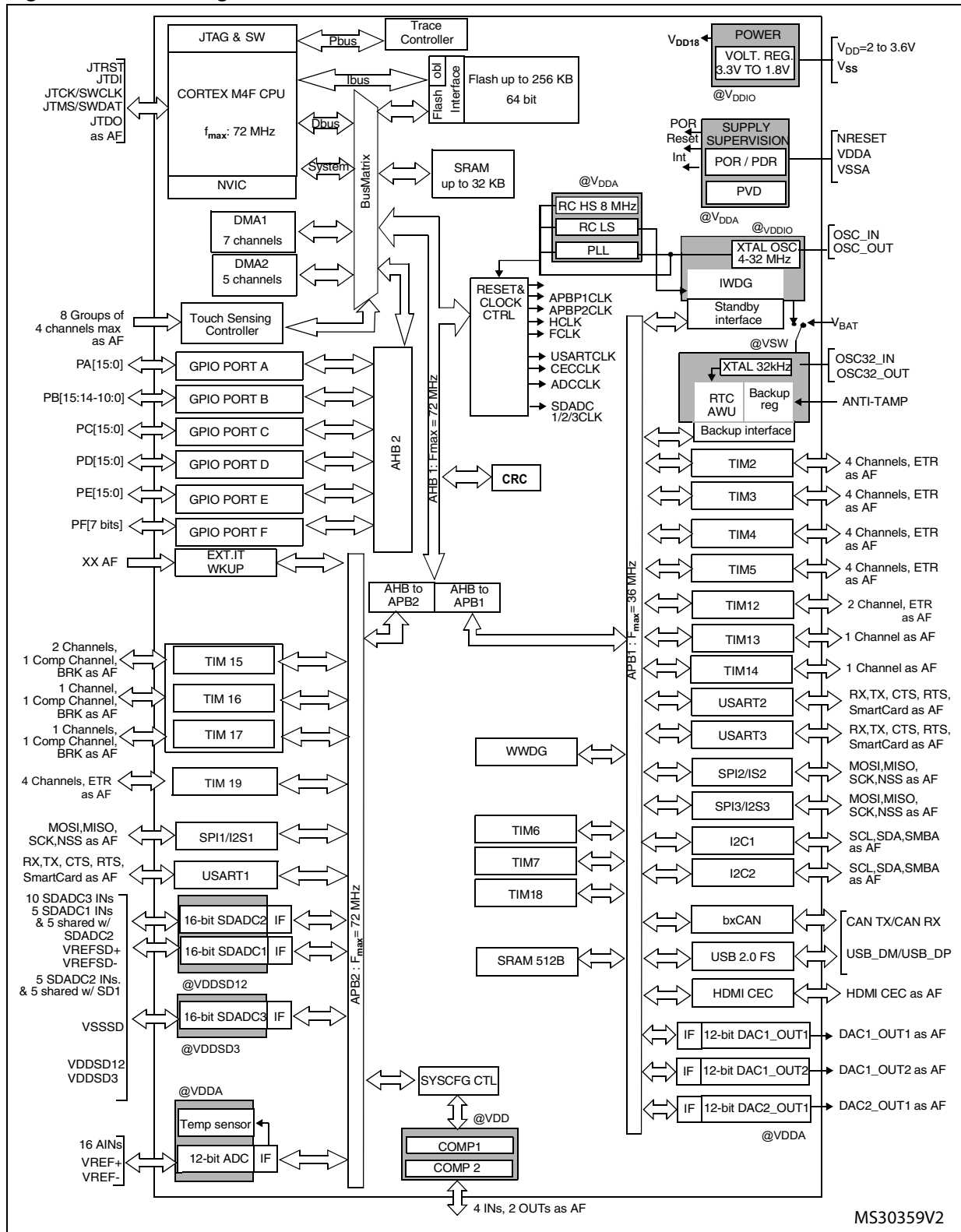
The STM32F37x family offers devices in five packages ranging from 48 pins to 100 pins. The set of included peripherals changes with the device chosen.

Table 2. Device overview

Peripheral		STM32F372Cx			STM32F372Rx			STM32F372Vx			STM32F373Cx			STM32F373Rx			STM32F373Vx		
Flash (Kbytes)		64	128	256	64	128	256	64	128	256	64	128	256	64	128	256	64	128	256
SRAM (Kbytes)		16	24	32	16	24	32	16	24	32	16	24	32	16	24	32	16	24	32
Timers	General purpose	9 (16-bit) 2 (32 bit)						9 (16-bit) 2 (32 bit)											
	Basic	3 (16-bit)						3 (16-bit)											
Comm. interfaces	SPI/I2S	3						3											
	I ² C	2						2											
	USART	3						3											
	CAN	1						1											
	USB	1						1											
GPIOs	Normal I/Os (TC, TTA)	36			52			84			36			52			84		
	5 volts Tolerant I/Os (FT, Ftf)	20			28			45			20			28			45		
12-bit ADCs		1						1											
16-bit ADCs Sigma-Delta		1 (SDADC1)						3											
12-bit DACs outputs		1 (DAC2)						3											
Analog comparator		1 (COMP1)						2											
Capacitive sensing channels		14			17			24			14			17			24		
Max. CPU frequency		72 MHz						72 MHz											
Main operating voltage		2.0 to 3.6 V						2.0 to 3.6 V											
16-bit SDADC operating voltage		2.2 to 3.6 V						2.2 to 3.6 V											
Operating temperature		Ambient operating temperature: –40 to 85 °C / –40 to 105 °C Junction temperature: –40 to 125 °C						Ambient operating temperature: –40 to 85 °C / –40 to 105 °C Junction temperature: –40 to 125 °C											
Packages		LQFP48			LQFP64			LQFP100, UFBGA100 ⁽¹⁾			LQFP48			LQFP64			LQFP100, UFBGA100 ⁽¹⁾		

1. UFBGA100 package available on 256-KB versions only.

Figure 1. Block diagram



1. AF: alternate function on I/O pins.
2. Example given for STM32F373xx device.



3 Functional overview

3.1 ARM® Cortex™-M4F core with embedded Flash and SRAM

The ARM Cortex-M4F processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M4F 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32F37x family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32F37x family.

3.2 Memory protection unit

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU can manage up to 8 protection areas that can all be further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

The Cortex-M4F processor is a high performance 32-bit processor designed for the microcontroller market. It offers significant benefits to developers, including:

- Outstanding processing performance combined with fast interrupt handling
- Enhanced system debug with extensive breakpoint and trace capabilities
- Efficient processor core, system and memories
- Ultralow power consumption with integrated sleep modes
- Platform security robustness with optional integrated memory protection unit (MPU).

With its embedded ARM core, the STM32F37x devices are compatible with all ARM development tools and software.

3.3 Embedded Flash memory

All STM32F37x devices feature up to 256 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

3.4 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.5 Embedded SRAM

All STM32F37x devices feature up to 32 Kbytes of embedded SRAM with hardware parity check. The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.6 Boot modes

At startup, Boot0 pin and Boot1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART2 (PD5/PD6) or USB (PA11/PA12) through DFU (device firmware upgrade).

3.7 Power management

3.7.1 Power supply schemes

- V_{DD} : external power supply for I/Os and the internal regulator. It is provided externally through V_{DD} pins, and can be 2.0 to 3.6 V.
- $V_{DDA} = 2.0$ to 3.6 V:
 - external analog power supplies for Reset blocks, RCs and PLL
 - supply voltage for 12-bit ADC, DACs and comparators (minimum voltage to be applied to V_{DDA} is 2.4 V when the 12-bit ADC and DAC are used).
- V_{DDSD12} and $V_{DDSD3} = 2.2$ to 3.6 V: supply voltages for SDADC1/2 and SDADC3 sigma delta ADCs. Independent from V_{DD}/V_{DDA} .
- $V_{BAT} = 1.65$ to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers when V_{DD} is not present.

3.7.2 Power supply supervisor

- The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, V_{POR}/PDR , without the need for an external reset circuit. The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD} .
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD} .

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.7.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR), and power-down.

- The MR mode is used in the nominal regulation mode (Run)
- The LPR mode is used in Stop mode.
- The power-down mode is used in Standby mode: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The voltage regulator is always enabled after reset. It is disabled in Standby mode.

3.7.4 Low-power modes

The STM32F37x supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the USARTs, the I2Cs, the CEC, the USB wakeup, and the RTC alarm.

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.8 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

3.9 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

Do not reconfigure GPIO pins which are not present on 48 and 64 pin packages to the analog mode. Additional current consumption in the range of tens of μA per pin can be observed if V_{DDA} is higher than V_{DDIO} .

3.10 Direct memory access (DMA)

The flexible 12-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The two DMAs can be used with the main peripherals: SPIs, I2Cs, USARTs, DACs, ADC, SDADCs, general-purpose timers.

3.11 Interrupts and events

3.11.1 Nested vectored interrupt controller (NVIC)

The STM32F37x devices embed a nested vectored interrupt controller (NVIC) able to handle up to 60 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.11.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 29 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 84 GPIOs can be connected to the 16 external interrupt lines.

3.12 12-bit analog-to-digital converter (ADC)

The 12-bit analog-to-digital converter is based on a successive approximation register (SAR) architecture. It has up to 16 external channels (AIN15:0) and 3 internal channels (temperature sensor, voltage reference, V_{BAT} voltage measurement) performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the timers (TIMx) can be internally connected to the ADC start and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

3.12.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode. See [Table 65: Temperature sensor calibration values on page 103](#).

3.12.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

3.12.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN18. As the V_{BAT} voltage may be higher than V_{DDA} , and thus outside the ADC input range, the V_{BAT} pin is internally connected to a divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.13 16-bit sigma delta analog-to-digital converters (SDADC)

Up to three 16-bit sigma-delta analog-to-digital converters are embedded in the STM32F37x. They have up to two separate supply voltages allowing the analog function voltage range to be independent from the STM32F37x power supply. They share up to 21 input pins which may be configured in any combination of single-ended (up to 21) or differential inputs (up to 11).

The conversion speed is up to 16.6 ksps for each SDADC when converting multiple channels and up to 50 ksps per SDADC if single channel conversion is used. There are two conversion modes: single conversion mode or continuous mode, capable of automatically scanning any number of channels. The data can be automatically stored in a system RAM buffer, reducing the software overhead.

A timer triggering system can be used in order to control the start of conversion of the three SDADCs and/or the 12-bit fast ADC. This timing control is very flexible, capable of triggering simultaneous conversions or inserting a programmable delay between the ADCs.

Up to two external reference pins (VREFSD+, VREFSD-) and an internal 1.2/1.8 V reference can be used in conjunction with a programmable gain (x0.5 to x32) in order to fine-tune the input voltage range of the SDADC.

3.14 Digital-to-analog converter (DAC)

The devices feature up to two 12-bit buffered DACs with three output channels that can be used to convert three digital signals into three analog voltage signal outputs. The internal structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital Interface supports the following features:

- Up to two DAC converters with three output channels:
 - DAC1 with two output channels
 - DAC2 with one output channel.
- 8-bit or 10-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- triangular-wave generation
- Dual DAC channel independent or simultaneous conversions (DAC1 only)
- DMA capability for each channel
- External triggers for conversion

3.15 Fast comparators (COMP)

The STM32F37x embeds up to 2 comparators with rail-to-rail inputs and high-speed output. The reference voltage can be internal or external (delivered by an I/O).

The threshold can be one of the following:

- DACs channel outputs
- External I/O
- Internal reference voltage (V_{REFINT}) or submultiple ($1/4 V_{REFINT}$, $1/2 V_{REFINT}$ and $3/4 V_{REFINT}$)

The comparators can be combined into a window comparator.

Both comparators can wake up the device from Stop mode and generate interrupts and breaks for the timers.

3.16 Touch sensing controller (TSC)

The devices provide a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect the presence of a finger near an electrode which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

Up to 24 touch sensing electrodes can be controlled by the TSC. The touch sensing I/Os are organized in 8 acquisition groups, with up to 4 I/Os in each group.

Table 3. Capacitive sensing GPIOs available on STM32F37x devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	5	TSC_G5_IO1	PB3
	TSC_G1_IO2	PA1		TSC_G5_IO2	PB4
	TSC_G1_IO3	PA2		TSC_G5_IO3	PB6
	TSC_G1_IO4	PA3		TSC_G5_IO4	PB7
2	TSC_G2_IO1	PA4	6	TSC_G6_IO1	PB14
	TSC_G2_IO2	PA5		TSC_G6_IO2	PB15
	TSC_G2_IO3	PA6		TSC_G6_IO3	PD8
	TSC_G2_IO4	PA7		TSC_G6_IO4	PD9
3	TSC_G3_IO1	PC4	7	TSC_G7_IO1	PE2
	TSC_G3_IO2	PC5		TSC_G7_IO2	PE3
	TSC_G3_IO3	PB0		TSC_G7_IO3	PE4
	TSC_G3_IO4	PB1		TSC_G7_IO4	PE5
4	TSC_G4_IO1	PA9	8	TSC_G8_IO1	PD12
	TSC_G4_IO2	PA10		TSC_G8_IO2	PD13
	TSC_G4_IO3	PA13		TSC_G8_IO3	PD14
	TSC_G4_IO4	PA14		TSC_G8_IO4	PD15

Table 4. No. of capacitive sensing channels available on STM32F37x devices

Analog I/O group	Number of capacitive sensing channels		
	STM32F37xCx	STM32F37xRx	STM32F37xVx
G1	3	3	3
G2	2	3	3
G3	1	3	3
G4	3	3	3
G5	3	3	3
G6	2	2	3
G7	0	0	3
G8	0	0	3
Number of capacitive sensing channels	14	17	24

3.17 Timers and watchdogs

The STM32F37x includes two 32-bit and nine 16-bit general-purpose timers, three basic timers, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare Channels	Complementary outputs
General-purpose	TIM2 TIM5	32-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	0
General-purpose	TIM3, TIM4, TIM19	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	0
General-purpose	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	0
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	0

Table 5. Timer feature comparison (continued)

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare Channels	Complementary outputs
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7, TIM18	16-bit	Up	Any integer between 1 and 65536	Yes	0	0

3.17.1 General-purpose timers (TIM2 to TIM5, TIM12 to TIM17, TIM19)

There are eleven synchronizable general-purpose timers embedded in the STM32F37x (see [Table 5](#) for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, 3, 4, 5 and 19

These five timers are full-featured general-purpose timers:

- TIM2 and TIM5 have 32-bit auto-reload up/downcounters and 32-bit prescalers
- TIM3, 4, and 19 have 16-bit auto-reload up/downcounters and 16-bit prescalers

These timers all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

The counters can be frozen in debug mode.

All have independent DMA request generation and support quadrature encoders.

- TIM12, 13, 14, 15, 16, 17

These six timers general-purpose timers with mid-range features:

They have 16-bit auto-reload upcounters and 16-bit prescalers.

- TIM12 has 2 channels
- TIM13 and TIM14 have 1 channel
- TIM15 has 2 channels and 1 complementary channel
- TIM16 and TIM17 have 1 channel and 1 complementary channel

All channels can be used for input capture/output compare, PWM or one-pulse mode output.

The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

The counters can be frozen in debug mode.

3.17.2 Basic timers (TIM6, TIM7, TIM18)

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

3.17.3 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.17.4 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB1 clock (PCLK1) derived from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.17.5 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.18 Real-time clock (RTC) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either from V_{DD} supply when present or through the V_{BAT} pin. The backup registers are thirty two 32-bit registers used to store 128 bytes of user application data.

They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28th, 29th (leap year), 30th and 31st day of the month.
- 2 programmable alarms with wake up from Stop and Standby mode capability.
- Periodic wakeup unit with programmable resolution and period.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- 3 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32

3.19 Inter-integrated circuit interface (I²C)

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes with 20 mA output drive. They support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 6. Comparison of I²C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I ² C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled

In addition, they provide hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeout verifications and ALERT protocol management. They also have a clock domain independent from the CPU clock, allowing the application to wake up the MCU from Stop mode on address match.

The I²C interfaces can be served by the DMA controller

Refer to [Table 7](#) for the differences between I2C1 and I2C2.

Table 7. STM32F37x I²C implementation

I ² C features ⁽¹⁾	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X
Independent clock	X	X
SMBus	X	X
Wakeup from STOP	X	X

1. X = supported.

3.20 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F37x embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

All USARTs interfaces are able to communicate at speeds of up to 9 Mbit/s.

They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode, Smart Card mode (ISO 7816 compliant), autobaudrate feature and have LIN Master/Slave capability. The USART interfaces can be served by the DMA controller.

Refer to [Table 8](#) for the features of USART1, USART2 and USART3.

Table 8. STM32F37x USART implementation

USART modes/features ⁽¹⁾	USART1	USART2	USART3
Hardware flow control for modem	X	X	X
Continuous communication using DMA	X	X	X
Multiprocessor communication	X	X	X
Synchronous mode	X	X	X
Smartcard mode	X	X	X
Single-wire half-duplex communication	X	X	X
IrDA SIR ENDEC block	X	X	X
LIN mode	X	X	X
Dual clock domain and wakeup from Stop mode	X	X	X
Receiver timeout interrupt	X	X	X
Modbus communication	X	X	X
Auto baud rate detection	X	X	X
Driver Enable	X	X	X

1. X = supported.

3.21 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I²S)

Up to three SPIs are able to communicate at up to 18 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The SPIs can be served by the DMA controller.

Three standard I²S interfaces (multiplexed with SPI1, SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I²S interfaces is/are configured in