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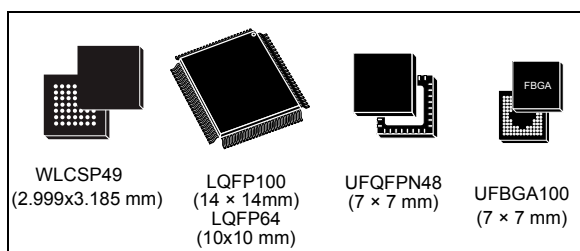


ARM<sup>®</sup> Cortex<sup>®</sup>-M4 32b MCU+FPU, 125 DMIPS, 512KB Flash, 128KB RAM, USB OTG FS, 11 TIMs, 1 ADC, 13 comm. interfaces

Datasheet - production data

## Features

- Dynamic Efficiency Line with BAM (Batch Acquisition Mode)
  - 1.7 V to 3.6 V power supply
  - -40°C to 85/105/125 °C temperature range
- Core: ARM<sup>®</sup> 32-bit Cortex<sup>®</sup>-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution from Flash memory, frequency up to 100 MHz, memory protection unit, 125 DMIPS/1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Memories
  - Up to 512 Kbytes of Flash memory
  - 128 Kbytes of SRAM
- Clock, reset and supply management
  - 1.7 V to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Power consumption
  - Run: 100 µA/MHz (peripheral off)
  - Stop (Flash in Stop mode, fast wakeup time): 42 µA Typ @ 25°C; 65 µA max @25 °C
  - Stop (Flash in Deep power down mode, slow wakeup time): down to 9 µA @ 25 °C; 28 µA max @25 °C
  - Standby: 1.8 µA @25 °C / 1.7 V without RTC; 11 µA @85 °C @1.7 V
  - V<sub>BAT</sub> supply for RTC: 1 µA @25 °C
- 1×12-bit, 2.4 MSPS A/D converter: up to 16 channels
- General-purpose DMA: 16-stream DMA controllers with FIFOs and burst support
- Up to 11 timers: up to six 16-bit, two 32-bit timers up to 100 MHz, each with up to four IC/OC/PWM or pulse counter and quadrature (incremental) encoder input, two watchdog timers (independent and window) and a SysTick timer



- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
  - Cortex<sup>®</sup>-M4 Embedded Trace Macrocell™
- Up to 81 I/O ports with interrupt capability
  - Up to 78 fast I/Os up to 100 MHz
  - Up to 77 5 V-tolerant I/Os
- Up to 13 communication interfaces
  - Up to 3 x I<sup>2</sup>C interfaces (SMBus/PMBus)
  - Up to 3 USARTs (2 x 12.5 Mbit/s, 1 x 6.25 Mbit/s), ISO 7816 interface, LIN, IrDA, modem control)
  - Up to 5 SPI/I<sup>2</sup>Ss (up to 50 Mbit/s, SPI or I<sup>2</sup>S audio protocol), SPI2 and SPI3 with muxed full-duplex I<sup>2</sup>S to achieve audio class accuracy via internal audio PLL or external clock
  - SDIO interface (SD/MMC/eMMC)
  - Advanced connectivity: USB 2.0 full-speed device/host/OTG controller with on-chip PHY
- CRC calculation unit
- 96-bit unique ID
- RTC: subsecond accuracy, hardware calendar
- All packages (WLCSP49, LQFP64/100, UFQFPN48, UFBGA100) are ECOPACK<sup>®</sup> 2

**Table 1. Device summary**

Reference	Part number
STM32F411xC	STM32F411CC, STM32F411RC, STM32F411VC
STM32F411xE	STM32F411CE, STM32F411RE, STM32F411VE

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# 1 Introduction

This datasheet provides the description of the STM32F411xC/xE line of microcontrollers.

The STM32F411xC/xE datasheet should be read in conjunction with RM0383 reference manual which is available from the STMicroelectronics website [www.st.com](http://www.st.com). It includes all information concerning Flash memory programming.

For information on the Cortex<sup>®</sup>-M4 core, please refer to the Cortex<sup>®</sup>-M4 programming manual (PM0214) available from [www.st.com](http://www.st.com).



## 2 Description

The STM32F411xC/xE devices are based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 100 MHz. The Cortex®-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F411xC/xE belongs to the STM32 Dynamic Efficiency™ product line (with products combining power efficiency, performance and integration) while adding a new innovative feature called Batch Acquisition Mode (BAM) allowing to save even more power consumption during data batching.

The STM32F411xC/xE incorporate high-speed embedded memories (up to 512 Kbytes of Flash memory, 128 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB bus and a 32-bit multi-AHB bus matrix.

All devices offer one 12-bit ADC, a low-power RTC, six general-purpose 16-bit timers including one PWM timer for motor control, two general-purpose 32-bit timers. They also feature standard and advanced communication interfaces.

- Up to three I<sup>2</sup>Cs
- Five SPIs
- Five I<sup>2</sup>Ss out of which two are full duplex. To achieve audio class accuracy, the I<sup>2</sup>S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Three USARTs
- SDIO interface
- USB 2.0 OTG full speed interface

Refer to [Table 2: STM32F411xC/xE features and peripheral counts](#) for the peripherals available for each part number.

The STM32F411xC/xE operate in the - 40 to + 125 °C temperature range from a 1.7 (PDR OFF) to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

These features make the STM32F411xC/xE microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile phone sensor hub

[Figure 3](#) shows the general block diagram of the devices.

Table 2. STM32F411xC/xE features and peripheral counts

Peripherals		STM32F411xC			STM32F411xE		
Flash memory in Kbytes		256			512		
SRAM in Kbytes	System	128					
Timers	General-purpose	7					
	Advanced-control	1					
Communication interfaces	SPI/ I <sup>2</sup> S	5/5 (2 full duplex)					
	I <sup>2</sup> C	3					
	USART	3					
	SDIO	1					
	USB OTG FS	1					
GPIOs		36	50	81	36	50	81
12-bit ADC		1					
Number of channels		10	16		10	16	
Maximum CPU frequency		100 MHz					
Operating voltage		1.7 to 3.6 V					
Operating temperatures		Ambient temperatures: - 40 to +85 °C / - 40 to + 105 °C/ - 40 to + 125 °C					
		Junction temperature: – 40 to + 130 °C					
Package		WLCSP49 UFQFPN48	LQFP64	UFBGA100 LQFP100	WLCSP49 UFQFPN48	LQFP64	UFBGA100 LQFP100

## 2.1 Compatibility with STM32F4 series

The STM32F411xC/xE are fully software and feature compatible with the STM32F4 series (STM32F42x, STM32F401, STM32F43x, STM32F41x, STM32F405 and STM32F407)

The STM32F411xC/xE can be used as drop-in replacement of the other STM32F4 products but some slight changes have to be done on the PCB board.

**Figure 1. Compatible board design for LQFP100 package**

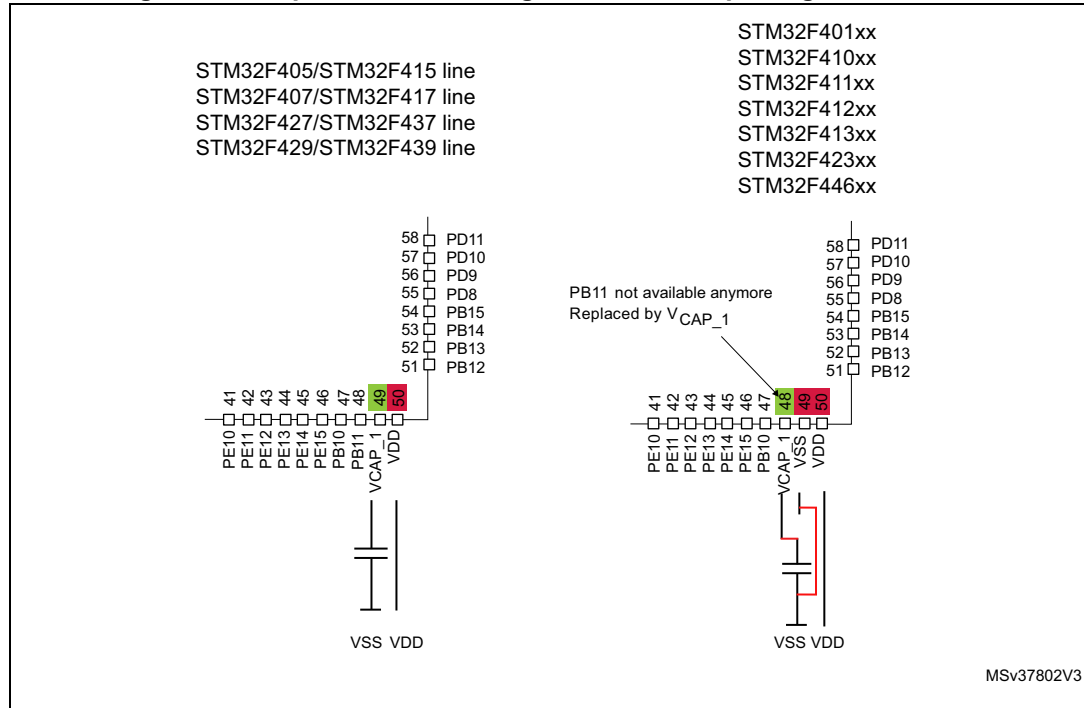


Figure 2. Compatible board design for LQFP64 package

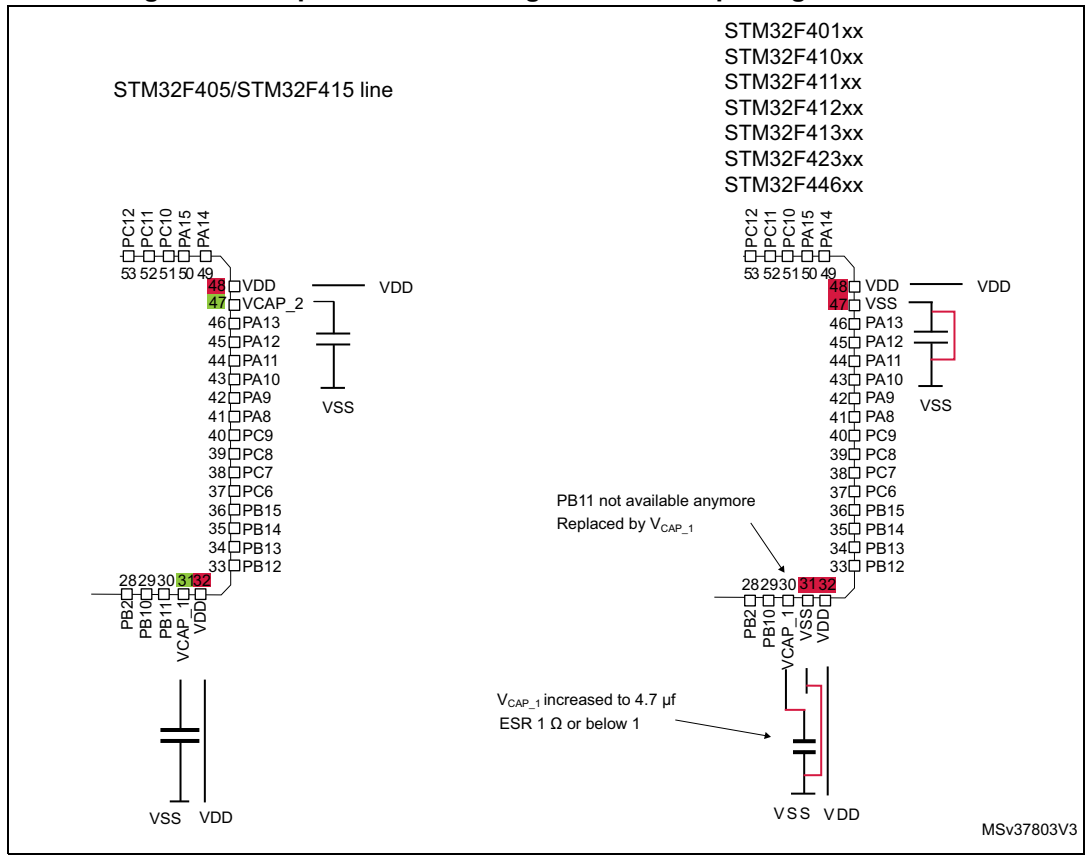
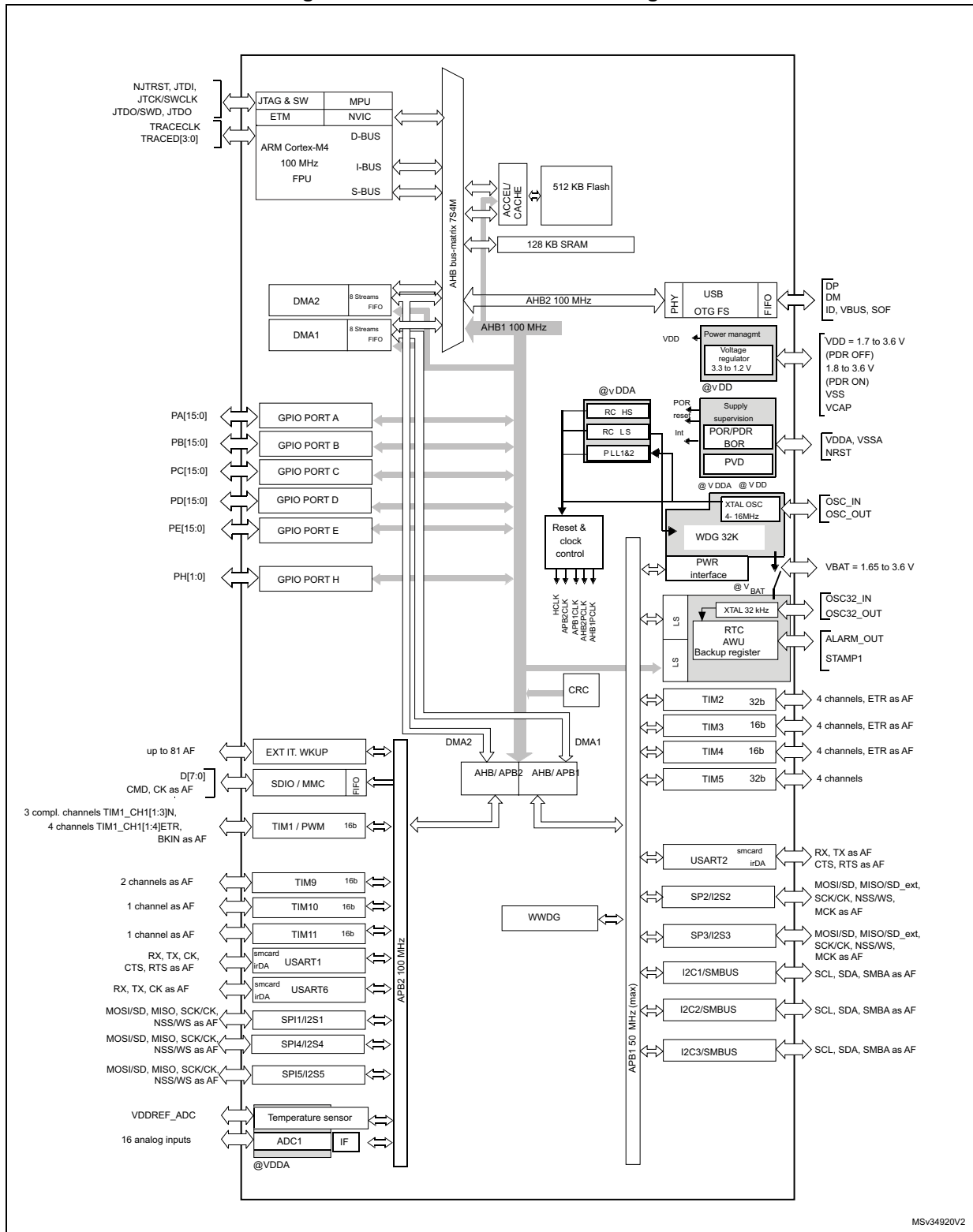


Figure 3. STM32F411xC/xE block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 100 MHz, while the timers connected to APB1 are clocked from TIMxCLK up to 100 MHz.





## 3 Functional overview

### 3.1 ARM<sup>®</sup> Cortex<sup>®</sup>-M4 with FPU core with embedded Flash and SRAM

The ARM<sup>®</sup> Cortex<sup>®</sup>-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM<sup>®</sup> Cortex<sup>®</sup>-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices. The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution. Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F411xC/xE devices are compatible with all ARM tools and software.

[Figure 3](#) shows the general block diagram of the STM32F411xC/xE.

*Note:* Cortex<sup>®</sup>-M4 with FPU is binary compatible with Cortex<sup>®</sup>-M3.

### 3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM<sup>®</sup> Cortex<sup>®</sup>-M4 with FPU processors. It balances the inherent performance advantage of the ARM<sup>®</sup> Cortex<sup>®</sup>-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 105 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the -bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 100 MHz.

### 3.3 Batch Acquisition mode (BAM)

The Batch acquisition mode allows enhanced power efficiency during data batching. It enables data acquisition through any communication peripherals directly to memory using the DMA in reduced power consumption as well as data processing while the rest of the system is in low-power mode (including the flash and ART). For example in an audio system, a smart combination of PDM audio sample acquisition and processing from the I2S directly to RAM (flash and ART™ stopped) with the DMA using BAM followed by some very short processing from flash allows to drastically reduce the power consumption of the application. A dedicated application note (AN4515) describes how to implement the BAM to allow the best power efficiency.

### 3.4 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

### 3.5 Embedded Flash memory

The devices embed up to 512 Kbytes of Flash memory available for storing programs and data.

To optimize the power consumption the Flash memory can also be switched off in Run or in Sleep mode (see [Section 3.18: Low-power modes](#)). Two modes are available: Flash in Stop mode or in DeepSleep mode (trade off between power saving and startup time, see [Table 34: Low-power mode wakeup timings\(1\)](#)). Before disabling the Flash memory, the code must be executed from the internal RAM.

#### One-time programmable bytes

A one-time programmable area is available with 16 OTP blocks of 32 bytes. Each block can be individually locked.

(Additional information can be found in the product reference manual.)

### 3.6 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

### 3.7 Embedded SRAM

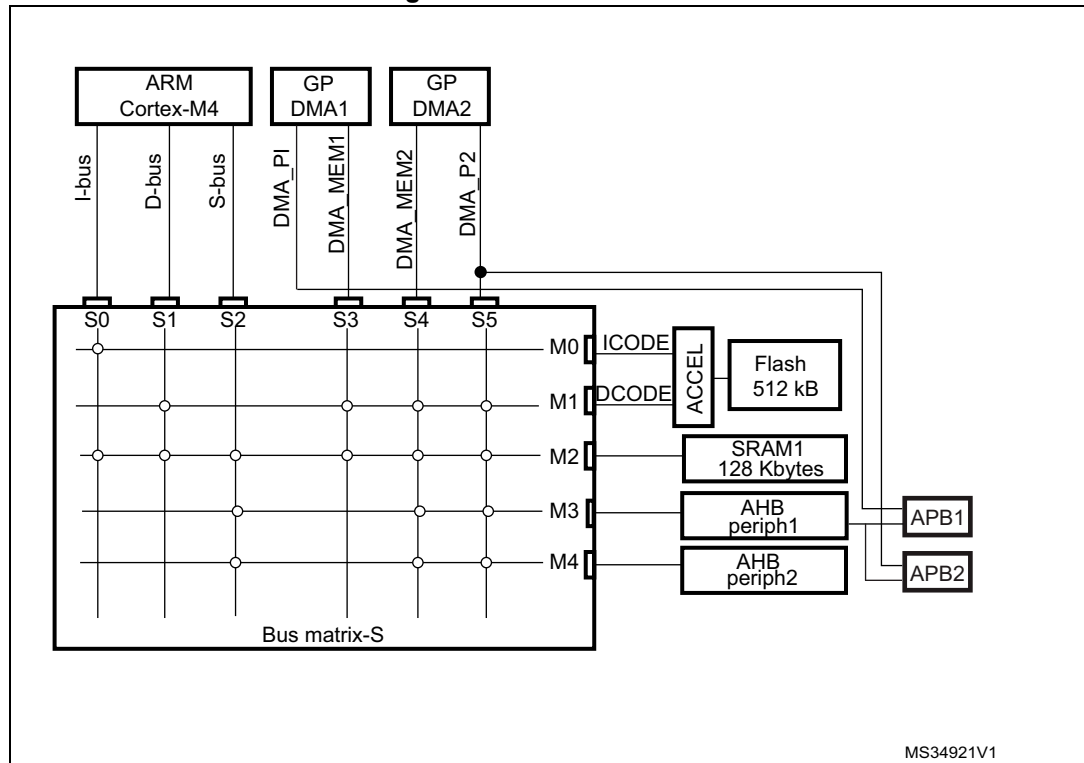
All devices embed:

- 128 Kbytes of system SRAM which can be accessed (read/write) at CPU clock speed with 0 wait states

### 3.8 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs) and the slaves (Flash memory, RAM, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 4. Multi-AHB matrix



### 3.9 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I<sup>2</sup>S
- I<sup>2</sup>C
- USART
- General-purpose, basic and advanced-control timers TIMx
- SD/SDIO/MMC/eMMC host interface
- ADC

### 3.10 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 62 maskable interrupt channels plus the 16 interrupt lines of the Cortex<sup>®</sup>-M4 with FPU.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

### 3.11 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 21 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 81 GPIOs can be connected to the 16 external interrupt lines.

### 3.12 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy at 25 °C. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 100 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the two AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the two AHB

buses is 100 MHz while the maximum frequency of the high-speed APB domains is 100 MHz. The maximum allowed frequency of the low-speed APB domain is 50 MHz.

The devices embed a dedicated PLL (PLL12S) which allows to achieve audio class performance. In this case, the I<sup>2</sup>S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

### 3.13 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The bootloader is located in system memory. It is used to reprogram the Flash memory by using USART1(PA9/10), USART2(PD5/6), USB OTG FS in device mode (PA11/12) through DFU (device firmware upgrade), I2C1(PB6/7), I2C2(PB10/3), I2C3(PA8/PB4), SPI1(PA4/5/6/7), SPI2(PB12/13/14/15) or SPI3(PA15, PC10/11/12).

For more detailed information on the bootloader, refer to Application Note: AN2606, *STM32™ microcontroller system memory boot mode*.

### 3.14 Power supply schemes

- VDD = 1.7 to 3.6 V: external power supply for I/Os with the internal supervisor (POR/PDR) disabled, provided externally through VDD pins. Requires the use of an external power supply supervisor connected to the VDD and NRST pins.
- V<sub>SSA</sub>, V<sub>DDA</sub> = 1.7 to 3.6 V: external analog power supplies for ADC, Reset blocks, RCs and PLL. V<sub>DDA</sub> and V<sub>SSA</sub> must be connected to V<sub>DD</sub> and V<sub>SS</sub>, respectively, with decoupling technique.
- V<sub>BAT</sub> = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V<sub>DD</sub> is not present.

Refer to [Figure 17: Power supply scheme](#) for more details.

### 3.15 Power supply supervisor

#### 3.15.1 Internal reset ON

This feature is available for  $V_{DD}$  operating voltage range 1.8 V to 3.6 V.

The internal power supply supervisor is enabled by holding PDR\_ON high.

The devices have an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes.

The devices remain in reset mode when  $V_{DD}$  is below a specified threshold,  $V_{POR/PDR}$  or  $V_{BOR}$ , without the need for an external reset circuit.

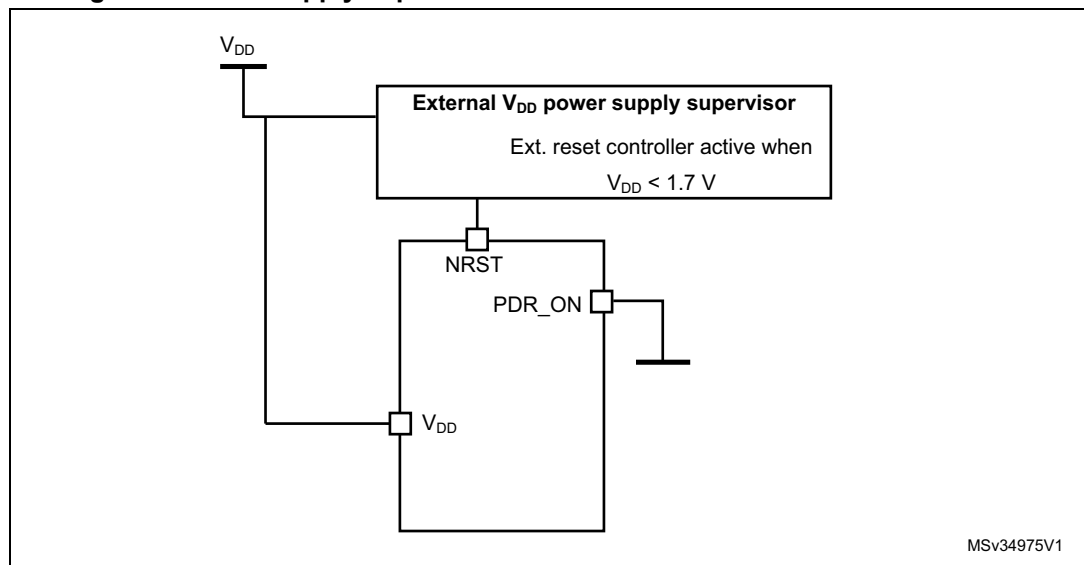
The devices also feature an embedded programmable voltage detector (PVD) that monitors the  $V_{DD}/V_{DDA}$  power supply and compares it to the  $V_{PVD}$  threshold. An interrupt can be generated when  $V_{DD}/V_{DDA}$  drops below the  $V_{PVD}$  threshold and/or when  $V_{DD}/V_{DDA}$  is higher than the  $V_{PVD}$  threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

#### 3.15.2 Internal reset OFF

This feature is available only on packages featuring the PDR\_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled by setting the PDR\_ON pin to low.

An external power supply supervisor should monitor  $V_{DD}$  and should set the device in reset mode when  $V_{DD}$  is below 1.7 V. NRST should be connected to this external power supply supervisor. Refer to [Figure 5: Power supply supervisor interconnection with internal reset OFF](#).

**Figure 5. Power supply supervisor interconnection with internal reset OFF<sup>(1)</sup>**



1. The PRD\_ON pin is only available on the WLCSP49 and UFBGA100 packages.

A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- $V_{BAT}$  functionality is no more available and VBAT pin should be connected to  $V_{DD}$ .

## 3.16 Voltage regulator

The regulator has four operating modes:

- Regulator ON
  - Main regulator mode (MR)
  - Low power regulator (LPR)
  - Power-down
- Regulator OFF

### 3.16.1 Regulator ON

On packages embedding the BYPASS\_REG pin, the regulator is enabled by holding BYPASS\_REG low. On all other packages, the regulator is always enabled.

There are three power modes configured by software when the regulator is ON:

- MR is used in the nominal regulation mode (With different voltage scaling in Run)  
In Main regulator mode (MR mode), different voltage scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption.
- LPR is used in the Stop modes  
The LP regulator mode is configured by software when entering Stop mode.
- Power-down is used in Standby mode.  
The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Depending on the package, one or two external ceramic capacitors should be connected on the  $V_{CAP\_1}$  and  $V_{CAP\_2}$  pins. The  $V_{CAP\_2}$  pin is only available for the LQFP100 and UFBGA100 packages.

All packages have the regulator ON feature.

### 3.16.2 Regulator OFF

The Regulator OFF is available only on the UFBGA100, which features the BYPASS\_REG pin. The regulator is disabled by holding BYPASS\_REG high. The regulator OFF mode allows to supply externally a V12 voltage source through  $V_{CAP\_1}$  and  $V_{CAP\_2}$  pins.

Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency. Refer to [Table 14: General operating conditions](#).

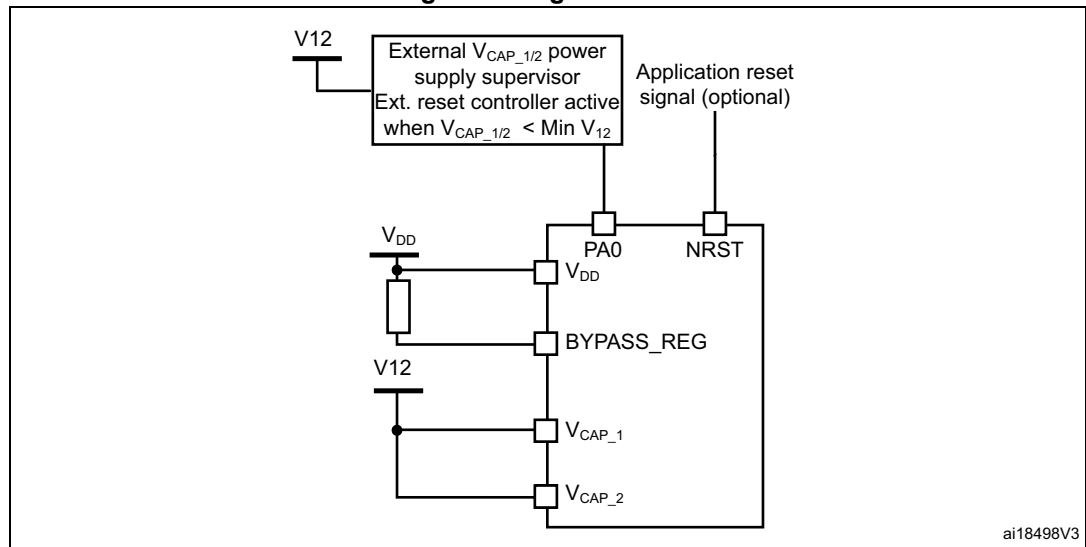
The two 2.2  $\mu\text{F}$   $V_{CAP}$  ceramic capacitors should be replaced by two 100 nF decoupling capacitors. Refer to [Figure 17: Power supply scheme](#).

When the regulator is OFF, there is no more internal monitoring on V12. An external power supply supervisor should be used to monitor the V12 of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V12 power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V12 logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.

Figure 6. Regulator OFF



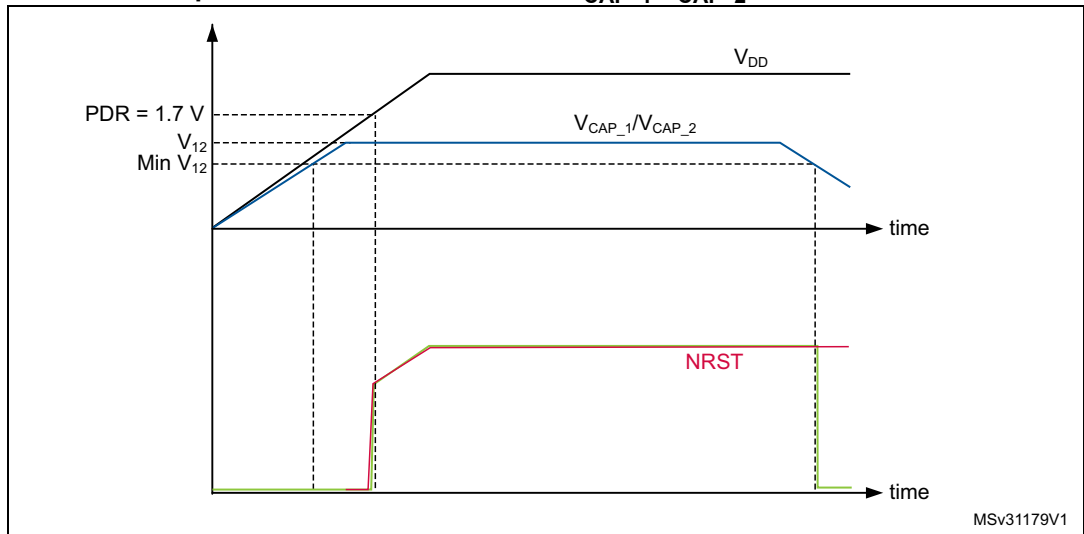
The following conditions must be respected:

- V<sub>DD</sub> should always be higher than V<sub>CAP\_1</sub> and V<sub>CAP\_2</sub> to avoid current injection between power domains.
- If the time for V<sub>CAP\_1</sub> and V<sub>CAP\_2</sub> to reach V<sub>12</sub> minimum value is faster than the time for V<sub>DD</sub> to reach 1.7 V, then PA0 should be kept low to cover both conditions: until V<sub>CAP\_1</sub> and V<sub>CAP\_2</sub> reach V<sub>12</sub> minimum value and until V<sub>DD</sub> reaches 1.7 V (see [Figure 7](#)).
- Otherwise, if the time for V<sub>CAP\_1</sub> and V<sub>CAP\_2</sub> to reach V<sub>12</sub> minimum value is slower than the time for V<sub>DD</sub> to reach 1.7 V, then PA0 could be asserted low externally (see [Figure 8](#)).
- If V<sub>CAP\_1</sub> and V<sub>CAP\_2</sub> go below V<sub>12</sub> minimum value and V<sub>DD</sub> is higher than 1.7 V, then a reset must be asserted on PA0 pin.

*Note:* The minimum value of V<sub>12</sub> depends on the maximum frequency targeted in the application

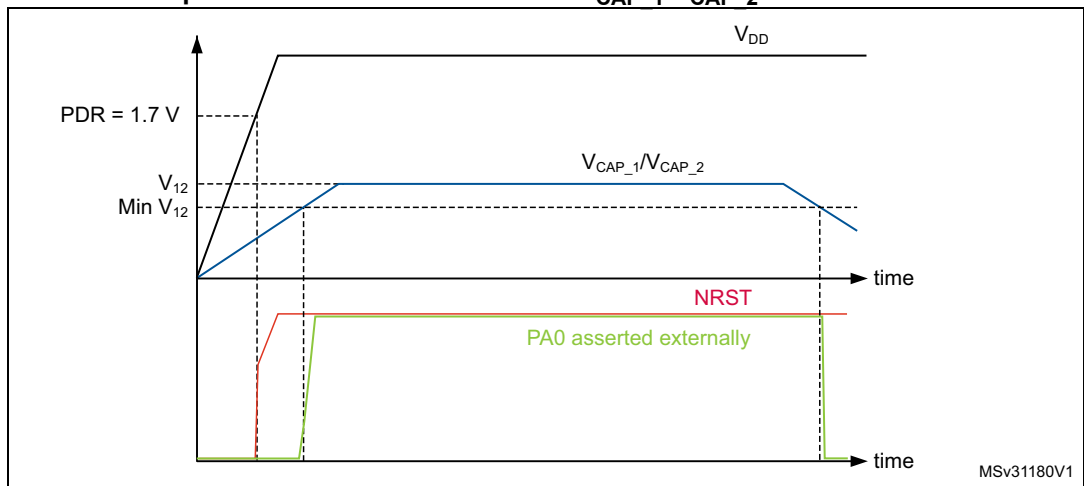


**Figure 7. Startup in regulator OFF: slow  $V_{DD}$  slope - power-down reset risen after  $V_{CAP\_1}/V_{CAP\_2}$  stabilization**



1. This figure is valid whatever the internal reset mode (ON or OFF).

**Figure 8. Startup in regulator OFF mode: fast  $V_{DD}$  slope - power-down reset risen before  $V_{CAP\_1}/V_{CAP\_2}$  stabilization**



1. This figure is valid whatever the internal reset mode (ON or OFF).

### 3.16.3 Regulator ON/OFF and internal power supply supervisor availability

Table 3. Regulator ON/OFF and internal power supply supervisor availability

Package	Regulator ON	Regulator OFF	Power supply supervisor ON	Power supply supervisor OFF
UFQFPN48	Yes	No	Yes	No
WLCSP49	Yes	No	Yes PDR_ON set to VDD	Yes PDR_ON external control <sup>(1)</sup>
LQFP64	Yes	No	Yes	No
LQFP100	Yes	No	Yes	No
UFBGA100	Yes BYPASS_REG set to VSS	Yes BYPASS_REG set to VDD	Yes PDR_ON set to VDD	Yes PDR_ON external control <sup>(1)</sup>

1. Refer to [Section 3.15: Power supply supervisor](#)

### 3.17 Real-time clock (RTC) and backup registers

The backup domain includes:

- The real-time clock (RTC)
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC features a reference clock detection, a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 μs to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The backup registers are 32-bit registers used to store 80 bytes of user application data when V<sub>DD</sub> power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see [Section 3.18: Low-power modes](#)).

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.