



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

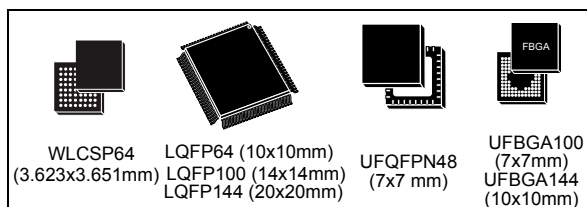


ARM[®]-Cortex[®]-M4 32b MCU+FPU, 125 DMIPS, 1MB Flash, 256KB RAM, USB OTG FS, 17 TIMs, 1 ADC, 17 comm. interfaces

Datasheet - production data

Features

- Dynamic Efficiency Line with BAM (Batch Acquisition Mode)
- Core: ARM[®] 32-bit Cortex[®]-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution from Flash memory, frequency up to 100 MHz, memory protection unit, 125 DMIPS/1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Memories
 - Up to 1 Mbyte of Flash memory
 - 256 Kbyte of SRAM
 - Flexible external static memory controller with up to 16-bit data bus: SRAM, PSRAM, NOR Flash memory
 - Dual mode Quad-SPI interface
- LCD parallel interface, 8080/6800 modes
- Clock, reset and supply management
 - 1.7 V to 3.6 V application supply and I/Os
 - POR, PDR, PVD and BOR
 - 4-to-26 MHz crystal oscillator
 - Internal 16 MHz factory-trimmed RC
 - 32 kHz oscillator for RTC with calibration
 - Internal 32 kHz RC with calibration
- Power consumption
 - Run: 112 µA/MHz (peripheral off)
 - Stop (Flash in Stop mode, fast wakeup time): 50 µA Typ @ 25 °C; 75 µA max @25 °C
 - Stop (Flash in Deep power down mode, slow wakeup time): down to 18 µA @ 25 °C; 40 µA max @25 °C
 - Standby: 2.4 µA @25 °C / 1.7 V without RTC; 12 µA @85 °C @1.7 V
 - V_{BAT} supply for RTC: 1 µA @25 °C
- 1×12-bit, 2.4 MSPS ADC: up to 16 channels
- 2x digital filters for sigma delta modulator, 4x PDM interfaces, stereo microphone support
- General-purpose DMA: 16-stream DMA



- Up to 17 timers: up to twelve 16-bit timers, two 32-bit timers up to 100 MHz each with up to four IC/OC/PWM or pulse counter and quadrature (incremental) encoder input, two watchdog timers (independent and window), one SysTick timer
- Debug mode
 - Serial wire debug (SWD) & JTAG
 - Cortex[®]-M4 Embedded Trace Macrocell™
- Up to 114 I/O ports with interrupt capability
 - Up to 109 fast I/Os up to 100 MHz
 - Up to 114 five V-tolerant I/Os
- Up to 17 communication interfaces
 - Up to 4x I²C interfaces (SMBus/PMBus)
 - Up to 4 USARTs (2 x 12.5 Mbit/s, 2 x 6.25 Mbit/s), ISO 7816 interface, LIN, IrDA, modem control)
 - Up to 5 SPI/I2Ss (up to 50 Mbit/s, SPI or I2S audio protocol), out of which 2 muxed full-duplex I2S interfaces
 - SDIO interface (SD/MMC/eMMC)
 - Advanced connectivity: USB 2.0 full-speed device/host/OTG controller with PHY
 - 2x CAN (2.0B Active)
- True random number generator
- CRC calculation unit
- 96-bit unique ID
- RTC: subsecond accuracy, hardware calendar
- All packages are ECOPACK[®]2

Table 1. Device summary

Reference	Part number
STM32F412xE	STM32F412CE, STM32F412RE, STM32F412VE, STM32F412ZE
STM32F412xG	STM32F412CG, STM32F412RG, STM32F412VG, STM32F412ZG

Contents

1	Introduction	12
2	Description	13
2.1	Compatibility with STM32F4 series	16
3	Functional overview	19
3.1	ARM® Cortex®-M4 with FPU core with embedded Flash and SRAM	19
3.2	Adaptive real-time memory accelerator (ART Accelerator™)	19
3.3	Batch Acquisition mode (BAM)	19
3.4	Memory protection unit	20
3.5	Embedded Flash memory	20
3.6	One-time programmable bytes	20
3.7	CRC (cyclic redundancy check) calculation unit	20
3.8	Embedded SRAM	21
3.9	Multi-AHB bus matrix	21
3.10	DMA controller (DMA)	21
3.11	Flexible static memory controller (FSMC)	22
3.12	Quad-SPI memory interface (QUAD-SPI)	22
3.13	Nested vectored interrupt controller (NVIC)	23
3.14	External interrupt/event controller (EXTI)	23
3.15	Clocks and startup	23
3.16	Boot modes	24
3.17	Power supply schemes	24
3.18	Power supply supervisor	26
3.18.1	Internal reset ON	26
3.18.2	Internal reset OFF	26
3.19	Voltage regulator	27
3.19.1	Regulator ON	27
3.19.2	Regulator OFF	28
3.19.3	Regulator ON/OFF and internal reset ON/OFF availability	31
3.20	Real-time clock (RTC) and backup registers	31
3.21	Low-power modes	32

3.22	V _{BAT} operation	32
3.23	Timers and watchdogs	33
3.23.1	Advanced-control timers (TIM1, TIM8)	35
3.23.2	General-purpose timers (TIMx)	35
3.23.3	Basic timer (TIM6, TIM7)	35
3.23.4	Independent watchdog	36
3.23.5	Window watchdog	36
3.23.6	SysTick timer	36
3.24	Inter-integrated circuit interface (I2C)	36
3.25	Universal synchronous/asynchronous receiver transmitters (USART)	37
3.26	Serial peripheral interface (SPI)	37
3.27	Inter-integrated sound (I ² S)	38
3.28	Audio PLL (PLLI2S)	38
3.29	Digital filter for sigma-delta modulators (DFSDM)	38
3.30	Secure digital input/output interface (SDIO)	40
3.31	Controller area network (bxCAN)	40
3.32	Universal serial bus on-the-go full-speed (USB_OTG_FS)	40
3.33	Random number generator (RNG)	41
3.34	General-purpose input/outputs (GPIOs)	41
3.35	Analog-to-digital converter (ADC)	41
3.36	Temperature sensor	41
3.37	Serial wire JTAG debug port (SWJ-DP)	41
3.38	Embedded Trace Macrocell™	42
4	Pinouts and pin description	43
5	Memory mapping	68
6	Electrical characteristics	72
6.1	Parameter conditions	72
6.1.1	Minimum and maximum values	72
6.1.2	Typical values	72
6.1.3	Typical curves	72
6.1.4	Loading capacitor	72
6.1.5	Pin input voltage	72

6.1.6	Power supply scheme	73
6.1.7	Current consumption measurement	74
6.2	Absolute maximum ratings	74
6.3	Operating conditions	76
6.3.1	General operating conditions	76
6.3.2	VCAP_1/VCAP_2 external capacitors	79
6.3.3	Operating conditions at power-up/power-down (regulator ON)	79
6.3.4	Operating conditions at power-up / power-down (regulator OFF)	80
6.3.5	Embedded reset and power control block characteristics	80
6.3.6	Supply current characteristics	81
6.3.7	Wakeup time from low-power modes	99
6.3.8	External clock source characteristics	101
6.3.9	Internal clock source characteristics	106
6.3.10	PLL characteristics	108
6.3.11	PLL spread spectrum clock generation (SSCG) characteristics	110
6.3.12	Memory characteristics	111
6.3.13	EMC characteristics	113
6.3.14	Absolute maximum ratings (electrical sensitivity)	115
6.3.15	I/O current injection characteristics	116
6.3.16	I/O port characteristics	117
6.3.17	NRST pin characteristics	122
6.3.18	TIM timer characteristics	123
6.3.19	Communications interfaces	124
6.3.20	12-bit ADC characteristics	136
6.3.21	Temperature sensor characteristics	142
6.3.22	V _{BAT} monitoring characteristics	143
6.3.23	Embedded reference voltage	143
6.3.24	DFSDM characteristics	144
6.3.25	FSMC characteristics	145
6.3.26	SD/SDIO MMC/eMMC card host interface (SDIO) characteristics	159
6.3.27	RTC characteristics	161
7	Package information	162
7.1	WLCSP64 package information	162
7.2	UFQFPN48 package information	165
7.3	LQFP64 package information	168

7.4	LQFP100 package information	171
7.5	LQFP144 package information	174
7.6	UFBGA100 package information	178
7.7	UFBGA144 package information	181
7.8	Thermal characteristics	184
7.8.1	Reference document	184
8	Part numbering	185
	Appendix A Recommendations when using the internal reset OFF	186
	Appendix B Application block diagrams	187
B.1	USB OTG full speed (FS) interface solutions	187
B.2	Sensor Hub application example.	189
B.3	Display application example	190
	Revision history	191

List of tables

Table 1.	Device summary	1
Table 2.	STM32F412xE/G features and peripheral counts	15
Table 3.	Embedded bootloader interfaces	24
Table 4.	Regulator ON/OFF and internal power supply supervisor availability.	31
Table 5.	Timer feature comparison.	34
Table 6.	Comparison of I2C analog and digital filters.	36
Table 7.	USART feature comparison	37
Table 8.	Legend/abbreviations used in the pinout table	48
Table 9.	STM32F412xE/G pin definition	49
Table 10.	STM32F412xE/G alternate functions	61
Table 11.	STM32F412xE/G register boundary addresses	69
Table 12.	Voltage characteristics	74
Table 13.	Current characteristics	75
Table 14.	Thermal characteristics.	75
Table 15.	General operating conditions	76
Table 16.	Features depending on the operating power supply range	78
Table 17.	VCAP_1/VCAP_2 operating conditions	79
Table 18.	Operating conditions at power-up / power-down (regulator ON)	79
Table 19.	Operating conditions at power-up / power-down (regulator OFF).	80
Table 20.	Embedded reset and power control block characteristics.	80
Table 21.	Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - $V_{DD} = 1.7\text{ V}$	82
Table 22.	Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - $V_{DD} = 3.6\text{ V}$	83
Table 23.	Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory- $V_{DD} = 1.7\text{ V}$	84
Table 24.	Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory - $V_{DD} = 3.6\text{ V}$	85
Table 25.	Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - $V_{DD} = 3.6\text{ V}$	86
Table 26.	Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - $V_{DD} = 1.7\text{ V}$	87
Table 27.	Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory - $V_{DD} = 3.6\text{ V}$	88
Table 28.	Typical and maximum current consumption in Sleep mode - $V_{DD} = 3.6\text{ V}$	89
Table 29.	Typical and maximum current consumption in Sleep mode - $V_{DD} = 1.7\text{ V}$	90
Table 30.	Typical and maximum current consumptions in Stop mode - $V_{DD} = 1.7\text{ V}$	91
Table 31.	Typical and maximum current consumption in Stop mode - $V_{DD} = 3.6\text{ V}$	92
Table 32.	Typical and maximum current consumption in Standby mode - $V_{DD} = 1.7\text{ V}$	92
Table 33.	Typical and maximum current consumption in Standby mode - $V_{DD} = 3.6\text{ V}$	92
Table 34.	Typical and maximum current consumptions in V_{BAT} mode.	93
Table 35.	Switching output I/O current consumption	96
Table 36.	Peripheral current consumption	97
Table 37.	Low-power mode wakeup timings ⁽¹⁾	100
Table 38.	High-speed external user clock characteristics.	102
Table 39.	Low-speed external user clock characteristics	102
Table 40.	HSE 4-26 MHz oscillator characteristics.	104
Table 41.	LSE oscillator characteristics ($f_{LSE} = 32.768\text{ kHz}$)	105

Table 42.	HSI oscillator characteristics	106
Table 43.	LSI oscillator characteristics	107
Table 44.	Main PLL characteristics	108
Table 45.	PLLI2S (audio PLL) characteristics	109
Table 46.	SSCG parameter constraints	110
Table 47.	Flash memory characteristics	111
Table 48.	Flash memory programming	112
Table 49.	Flash memory programming with V_{PP} voltage	113
Table 50.	Flash memory endurance and data retention	113
Table 51.	EMS characteristics for LQFP144 package	114
Table 52.	EMI characteristics for LQFP144	115
Table 53.	ESD absolute maximum ratings	115
Table 54.	Electrical sensitivities	116
Table 55.	I/O current injection susceptibility	117
Table 56.	I/O static characteristics	117
Table 57.	Output voltage characteristics	120
Table 58.	I/O AC characteristics	120
Table 59.	NRST pin characteristics	122
Table 60.	TIMx characteristics	123
Table 61.	I ² C characteristics	124
Table 62.	SCL frequency ($f_{PCLK1} = 50$ MHz, $V_{DD} = V_{DD_I2C} = 3.3$ V)	125
Table 63.	FMPI ² C characteristics	126
Table 64.	SPI dynamic characteristics	128
Table 65.	I ² S dynamic characteristics	131
Table 66.	QSPI dynamic characteristics in SDR mode	133
Table 67.	QSPI dynamic characteristics in DDR mode	133
Table 68.	USB OTG FS startup time	134
Table 69.	USB OTG FS DC electrical characteristics	134
Table 70.	USB OTG FS electrical characteristics	135
Table 71.	ADC characteristics	136
Table 72.	ADC accuracy at $f_{ADC} = 18$ MHz	137
Table 73.	ADC accuracy at $f_{ADC} = 30$ MHz	138
Table 74.	ADC accuracy at $f_{ADC} = 36$ MHz	138
Table 75.	ADC dynamic accuracy at $f_{ADC} = 18$ MHz - limited test conditions	138
Table 76.	ADC dynamic accuracy at $f_{ADC} = 36$ MHz - limited test conditions	138
Table 77.	Temperature sensor characteristics	142
Table 78.	Temperature sensor calibration values	142
Table 79.	V_{BAT} monitoring characteristics	143
Table 80.	Embedded internal reference voltage	143
Table 81.	Internal reference voltage calibration values	143
Table 82.	DFSDM characteristics	144
Table 83.	Asynchronous non-multiplexed SRAM/PSRAM/NOR - read timings	147
Table 84.	Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings	147
Table 85.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings	148
Table 86.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings	149
Table 87.	Asynchronous multiplexed PSRAM/NOR read timings	150
Table 88.	Asynchronous multiplexed PSRAM/NOR read-NWAIT timings	150
Table 89.	Asynchronous multiplexed PSRAM/NOR write timings	152
Table 90.	Asynchronous multiplexed PSRAM/NOR write-NWAIT timings	152

Table 91.	Synchronous multiplexed NOR/PSRAM read timings	154
Table 92.	Synchronous multiplexed PSRAM write timings	156
Table 93.	Synchronous non-multiplexed NOR/PSRAM read timings	157
Table 94.	Synchronous non-multiplexed PSRAM write timings	159
Table 95.	Dynamic characteristics: SD / MMC characteristics	160
Table 96.	Dynamic characteristics: eMMC characteristics VDD = 1.7 V to 1.9 V	161
Table 97.	RTC characteristics	161
Table 98.	WLCSP64 - 64-pin, 3.658 x 3.686 mm, 0.4 mm pitch wafer level chip scale package mechanical data	163
Table 99.	WLCSP64 recommended PCB design rules (0.4 mm pitch)	163
Table 100.	UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data	165
Table 101.	LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data	169
Table 102.	LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data	171
Table 103.	LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data	175
Table 104.	UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data	178
Table 105.	UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)	179
Table 106.	UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package mechanical data	181
Table 107.	UFBGA144 recommended PCB design rules (0.80 mm pitch BGA)	182
Table 108.	Package thermal characteristics	184
Table 109.	Ordering information scheme	185
Table 110.	Document revision history	191

List of figures

Figure 1.	Compatible board design for LQFP100 package	16
Figure 2.	Compatible board design for LQFP64 package	17
Figure 3.	Compatible board design for LQFP144 package	17
Figure 4.	STM32F412xE/G block diagram	18
Figure 5.	Multi-AHB matrix	21
Figure 6.	VDDUSB connected to an external independent power supply	25
Figure 7.	Power supply supervisor interconnection with internal reset OFF	27
Figure 8.	Regulator OFF	29
Figure 9.	Startup in regulator OFF: slow V_{DD} slope power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization	30
Figure 10.	Startup in regulator OFF mode: fast V_{DD} slope power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization	30
Figure 11.	STM32F412xE/G WLCSP64 pinout	43
Figure 12.	STM32F412xE/G UFQFPN48 pinout	43
Figure 13.	STM32F412xE/G LQFP64 pinout	44
Figure 14.	STM32F412xE/G LQFP100 pinout	45
Figure 15.	STM32F412xE/G LQFP144 pinout	46
Figure 16.	STM32F412xE/G UFBGA100 pinout	47
Figure 17.	STM32F412xE/G UFBGA144 pinout	48
Figure 18.	Memory map	68
Figure 19.	Pin loading conditions	72
Figure 20.	Input voltage measurement	72
Figure 21.	Power supply scheme	73
Figure 22.	Current consumption measurement scheme	74
Figure 23.	External capacitor C_{EXT}	79
Figure 24.	Typical V_{BAT} current consumption (LSE and RTC ON/LSE oscillator "low power" mode selection)	93
Figure 25.	Typical V_{BAT} current consumption (LSE and RTC ON/LSE oscillator "high drive" mode selection)	94
Figure 26.	Low-power mode wakeup	100
Figure 27.	High-speed external clock source AC timing diagram	103
Figure 28.	Low-speed external clock source AC timing diagram	103
Figure 29.	Typical application with an 8 MHz crystal	104
Figure 30.	Typical application with a 32.768 kHz crystal	105
Figure 31.	ACC_{HSI} versus temperature	106
Figure 32.	ACC_{LSI} versus temperature	107
Figure 33.	PLL output clock waveforms in center spread mode	111
Figure 34.	PLL output clock waveforms in down spread mode	111
Figure 35.	FT/TC I/O input characteristics	119
Figure 36.	I/O AC characteristics definition	122
Figure 37.	Recommended NRST pin protection	123
Figure 38.	I ² C bus AC waveforms and measurement circuit	125
Figure 39.	FMPI ² C timing diagram and measurement circuit	127
Figure 40.	SPI timing diagram - slave mode and CPHA = 0	129
Figure 41.	SPI timing diagram - slave mode and CPHA = 1 ⁽¹⁾	130
Figure 42.	SPI timing diagram - master mode ⁽¹⁾	130
Figure 43.	I ² S slave timing diagram (Philips protocol) ⁽¹⁾	132
Figure 44.	I ² S master timing diagram (Philips protocol) ⁽¹⁾	132

Figure 45.	USB OTG FS timings: definition of data signal rise and fall time	135
Figure 46.	ADC accuracy characteristics	139
Figure 47.	Typical connection diagram using the ADC	140
Figure 48.	Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})	141
Figure 49.	Power supply and reference decoupling (V_{REF+} connected to V_{DDA})	142
Figure 50.	Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms	146
Figure 51.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms	148
Figure 52.	Asynchronous multiplexed PSRAM/NOR read waveforms	149
Figure 53.	Asynchronous multiplexed PSRAM/NOR write waveforms	151
Figure 54.	Synchronous multiplexed NOR/PSRAM read timings	153
Figure 55.	Synchronous multiplexed PSRAM write timings	155
Figure 56.	Synchronous non-multiplexed NOR/PSRAM read timings	157
Figure 57.	Synchronous non-multiplexed PSRAM write timings	158
Figure 58.	SDIO high-speed mode	160
Figure 59.	SD default mode	160
Figure 60.	WLCSP64 - 64-pin, 3.658 x 3.686 mm, 0.4 mm pitch wafer level chip scale package outline	162
Figure 61.	WLCSP64 - 64-pin, 3.658 x 3.686 mm, 0.4 mm pitch wafer level chip scale recommended footprint	163
Figure 62.	WLCSP64 marking example (package top view)	164
Figure 63.	UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline	165
Figure 64.	UFQFPN48 recommended footprint	166
Figure 65.	UFQFPN48 marking example (package top view)	167
Figure 66.	LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline	168
Figure 67.	LQFP64 recommended footprint	170
Figure 68.	LQFP64 marking example (package top view)	170
Figure 69.	LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline	171
Figure 70.	LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint	172
Figure 71.	LQFP100 marking example (package top view)	173
Figure 72.	LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline	174
Figure 73.	LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package recommended footprint	176
Figure 74.	LQFP144 marking example (package top view)	177
Figure 75.	UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline	178
Figure 76.	UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint	179
Figure 77.	UFBGA100 marking example (package top view)	180
Figure 78.	UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package outline	181
Figure 79.	UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array recommended footprint	182
Figure 80.	UFBGA144 marking example (package top view)	183
Figure 81.	USB controller configured as peripheral-only and used in Full speed mode	187
Figure 82.	USB peripheral-only Full speed mode with direct connection for VBUS sense	187
Figure 83.	USB peripheral-only Full speed mode, VBUS detection using GPIO	188
Figure 84.	USB controller configured as host-only and used in full speed mode	188
Figure 85.	USB controller configured in dual mode and used in full speed mode	189
Figure 86.	Sensor Hub application example	189

Figure 87. Display application example 190

1 Introduction

This datasheet provides the description of the STM32F412xE/G microcontrollers.

For information on the Cortex[®]-M4 core, refer to the Cortex[®]-M4 programming manual (PM0214) available from www.st.com.



2 Description

The STM32F412xE/G devices are based on the high-performance ARM[®] Cortex[®]-M4 32-bit RISC core operating at a frequency of up to 100 MHz. Their Cortex[®]-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F412xE/G belong to the STM32 Dynamic Efficiency[™] product line (with products combining power efficiency, performance and integration) while adding a new innovative feature called Batch Acquisition Mode (BAM) allowing to save even more power consumption during data batching.

The STM32F412xE/G incorporate high-speed embedded memories (up to 1 Mbyte of Flash memory, 256 Kbyte of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses, three AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer one 12-bit ADC, a low-power RTC, twelve general-purpose 16-bit timers, two PWM timer for motor control and two general-purpose 32-bit timers.

They also feature standard and advanced communication interfaces.

- Up to four I²Cs, including one I²C supporting Fast-Mode Plus
- Five SPIs
- Five I²Ss out of which two are full duplex. To achieve audio class accuracy, the I²S peripherals can be clocked via a dedicate internal audio PLL or via an external clock to allow synchronization.
- Four USARTs
- An SDIO/MMC interface
- An USB 2.0 OTG full-speed interface
- Two CANs.

In addition, the STM32F412xE/G embed advanced peripherals:

- A flexible static memory control interface (FSMC)
- A Quad-SPI memory interface
- A digital filter for sigma modulator (DFSDM), two filters, up to four inputs, and support of microphone MEMs.

The STM32F412xE/G are offered in 7 packages ranging from 48 to 144 pins. The set of available peripherals depends on the selected package. Refer to [Table 2: STM32F412xE/G features and peripheral counts](#) for the peripherals available for each part number.

The STM32F412xE/G operates in the – 40 to + 105 °C temperature range from a 1.7 (PDR OFF) to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

These features make the STM32F412xE/G microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile phone sensor hub
- Wearable devices
- Connected objects
- Wifi modules

Figure 4 shows the general block diagram of the devices.

Table 2. STM32F412xE/G features and peripheral counts

Peripherals		STM32F412xE				STM32F412xG			
Flash memory (Kbyte)		512				1024			
SRAM (Kbyte)	System	256							
FSMC memory controller		-	1		-	1			
Quad-SPI memory interface		-	1		-	1			
Timers	General-purpose	10							
	Advanced-control	2							
	Basic	2							
Random number generator		1							
Comm. interfaces	SPI/ I ² S	5/5 (2 full duplex)							
	I ² C	3							
	I ² C FMP	1							
	USART	3	4		3	4			
	SDIO/MMC	1							
	USB/OTG FS Dual power rail	1 No		1 Yes		1 No		1 Yes	
	CAN	2							
Number of digital Filters for Sigma-delta modulator		2	2		2	2			
Number of channels		3	4		3	4			
LCD parallel interface Data bus size		-	8	16		-	8	16	
GPIOs		36	50	81	114	36	50	81	114
12-bit ADC Number of channels		1							
		10	16		10	16			
Maximum CPU frequency		100 MHz							
Operating voltage		1.7 to 3.6 V							
Operating temperatures		Ambient temperatures: -40 to +85 °C/-40 to +105 °C							
		Junction temperature: -40 to + 125 °C							
Package		UFQ FPN48	LQFP64 WLCSP64	UFBGA 100 LQFP100	UFBGA 144 LQFP144	UFQ FPN48	LQFP64 WLCSP 64	UFBGA 100 LQFP100	UFBGA 144 LQFP144

2.1 Compatibility with STM32F4 series

The STM32F412xE/G are fully software and feature compatible with the STM32F4 series (STM32F42x, STM32F401, STM32F43x, STM32F41x, STM32F405 and STM32F407)

The STM32F412xE/G can be used as drop-in replacement of the other STM32F4 products but some slight changes have to be done on the PCB board.

Figure 1. Compatible board design for LQFP100 package

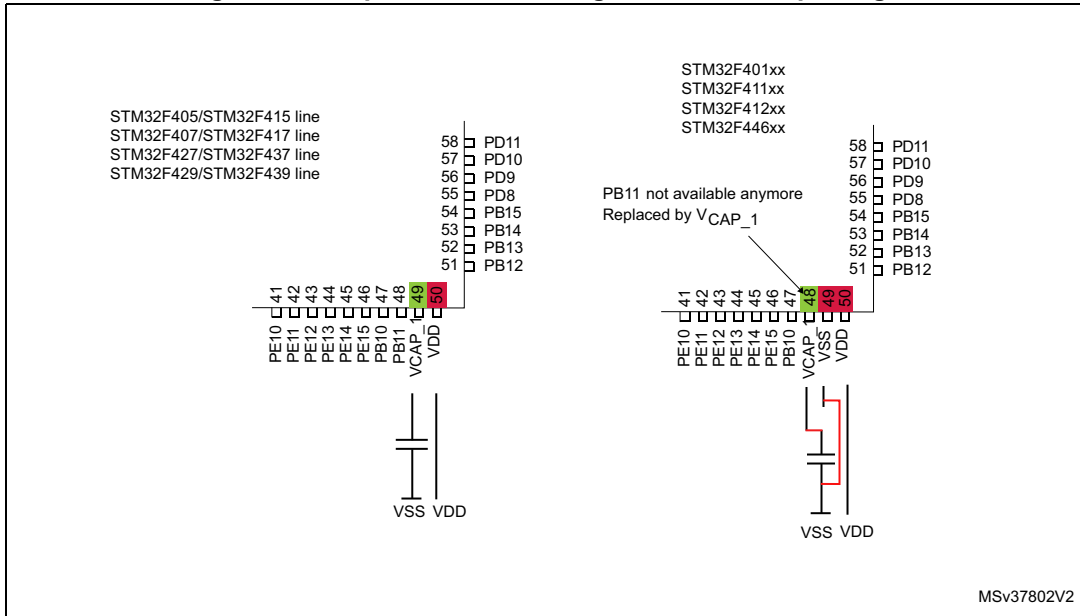


Figure 2. Compatible board design for LQFP64 package

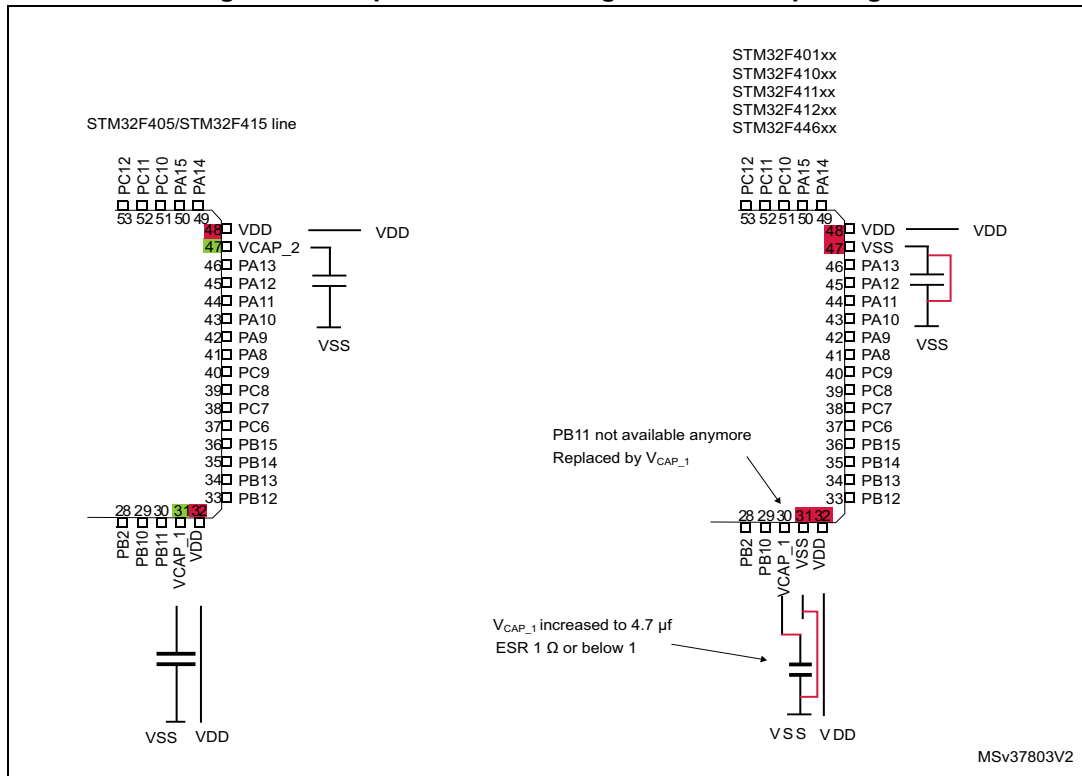


Figure 3. Compatible board design for LQFP144 package

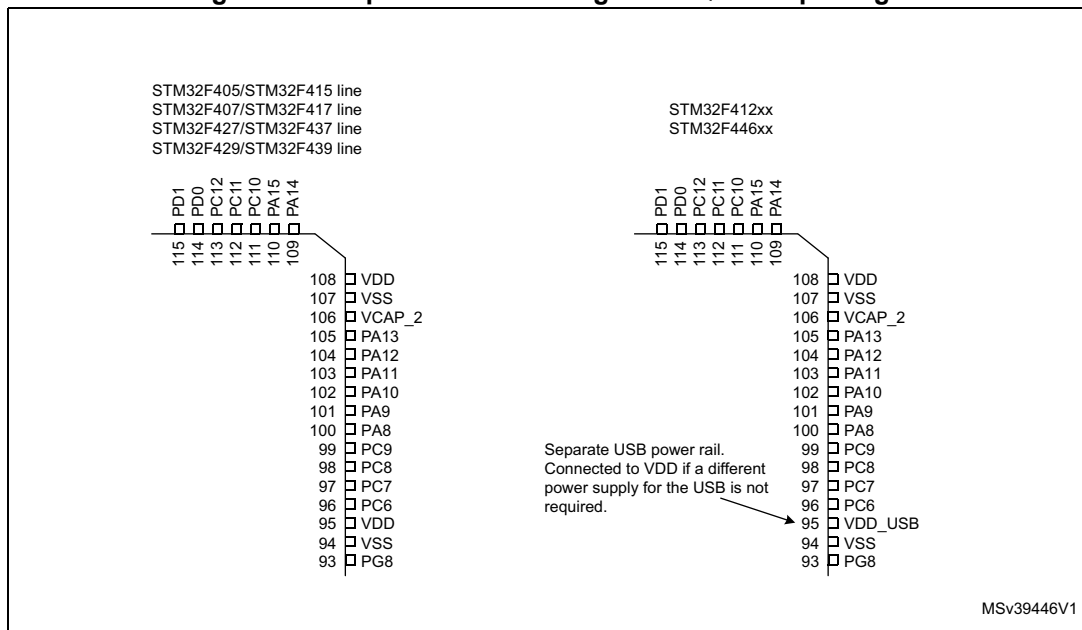
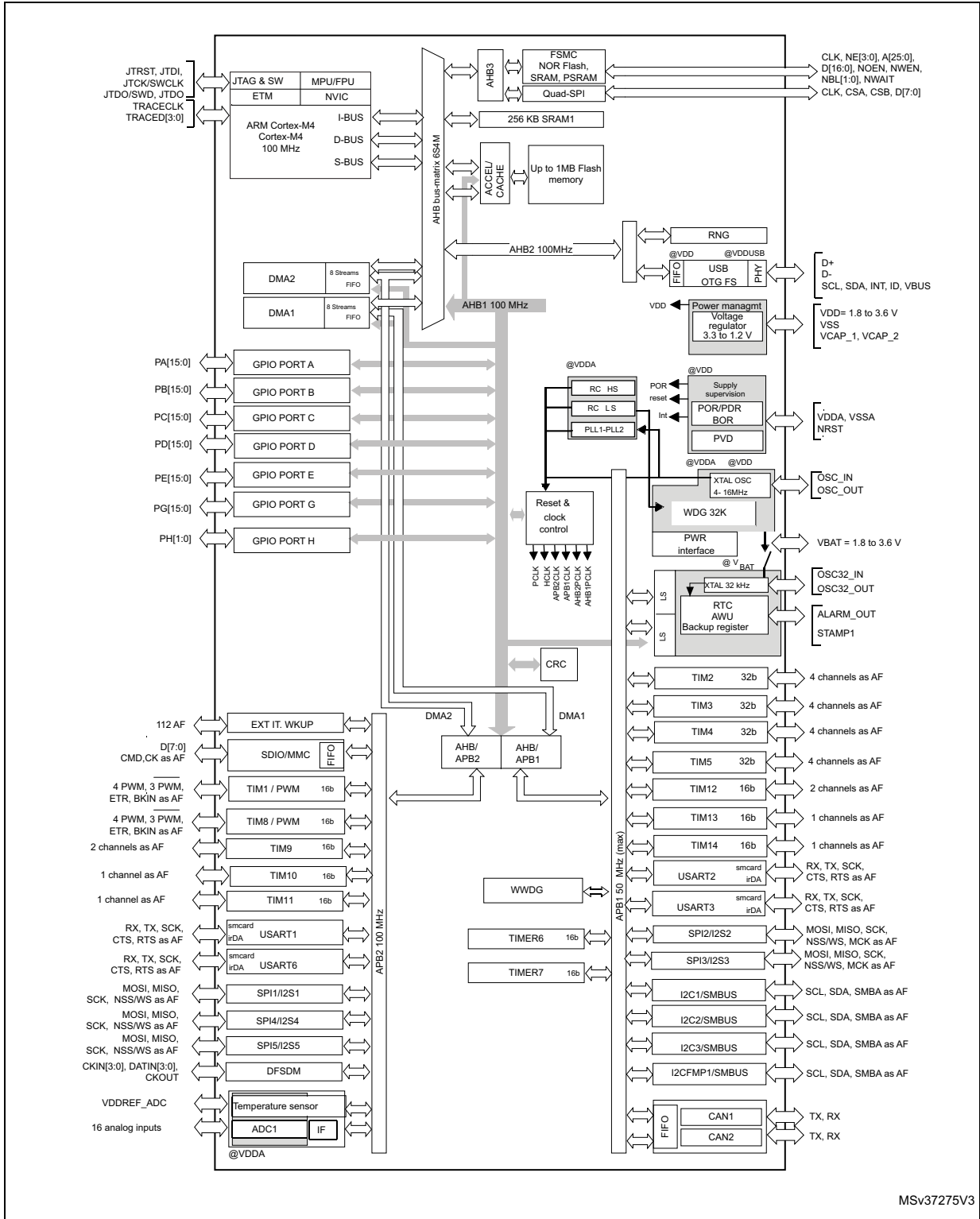


Figure 4. STM32F412xE/G block diagram



MSv37275V3

1. The timers connected to APB2 are clocked from TIMxCLK up to 100 MHz, while the timers connected to APB1 are clocked from TIMxCLK up to 50 MHz.

3 Functional overview

3.1 ARM[®] Cortex[®]-M4 with FPU core with embedded Flash and SRAM

The ARM[®] Cortex[®]-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM[®] Cortex[®]-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F412xE/G devices are compatible with all ARM tools and software.

Figure 4 shows the general block diagram of the STM32F412xE/G.

Note: Cortex[®]-M4 with FPU is binary compatible with Cortex[®]-M3.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM[®] Cortex[®]-M4 with FPU processors. It balances the inherent performance advantage of the ARM[®] Cortex[®]-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 125 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 100 MHz.

3.3 Batch Acquisition mode (BAM)

The Batch acquisition mode allows enhanced power efficiency during data batching. It enables data acquisition through any communication peripherals directly to memory using the DMA in reduced power consumption as well as data processing while the rest of the system is in low-power mode (including the flash and ART). For example in an audio system, a smart combination of PDM audio sample acquisition and processing from the DFSDM directly to RAM (flash and ART™ stopped) with the DMA using BAM followed by some very short processing from flash allows to drastically reduce the power consumption of the application. A dedicated application note (AN4515) describes how to implement the STM32F412xE/G BAM to allow the best power efficiency.

3.4 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 byte and the whole 4 Gbyte of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.5 Embedded Flash memory

The devices embed up to 1 Mbyte of Flash memory available for storing programs and data.

The Flash user area can be protected against reading by an entrusted code (Read Protection, RDP) with different protection levels.

The flash user sectors can also be individually protected against write operation.

Furthermore the proprietary readout protection (PCROP) can also individually protect the flash user sectors against D-bus read accesses.

(Additional information can be found in the product reference manual).

To optimize the power consumption the Flash memory can also be switched off in Run or in Sleep mode (see [Section 3.21: Low-power modes](#)).

Two modes are available: Flash in Stop mode or in DeepSleep mode (trade off between power saving and startup time).

Before disabling the Flash, the code must be executed from the internal RAM.

3.6 One-time programmable bytes

A one-time programmable area is available with 16 OTP blocks of 32 bytes. Each block can be individually locked

(Additional information can be found in the product reference manual)

3.7 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

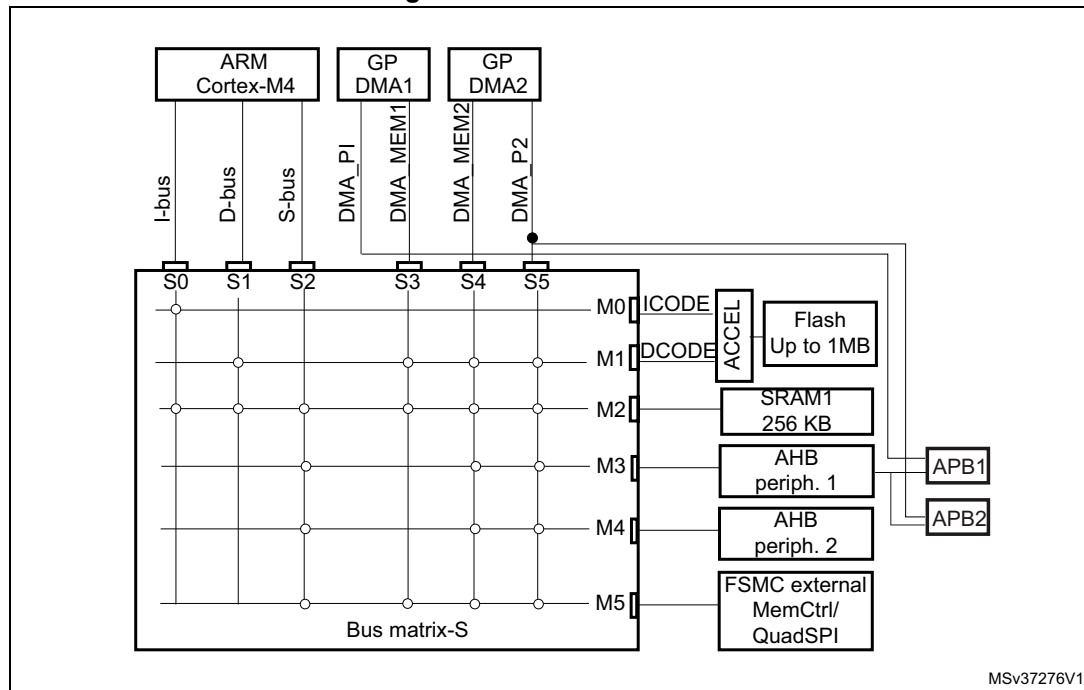
3.8 Embedded SRAM

All devices embed 256 Kbyte of system SRAM which can be accessed (read/write) at CPU clock speed with 0 wait states

3.9 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs) and the slaves (Flash memory, RAM, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 5. Multi-AHB matrix



3.10 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I²S
- I²C and I²CFMP
- USART
- General-purpose, basic and advanced-control timers TIMx
- SD/SDIO/MMC/eMMC host interface
- Quad-SPI
- ADC
- Digital Filter for sigma-delta modulator (DFSDM) with a separate stream for each filter.

3.11 Flexible static memory controller (FSMC)

The Flexible static memory controller (FSMC) includes a NOR/PSRAM memory controller. It features four Chip Select outputs supporting the following modes: SRAM, PSRAM and NOR Flash memory.

The main functions are:

- 8-, 16-bit data bus width
- Write FIFO
- Maximum FSMC_CLK frequency for synchronous accesses is 90 MHz.

LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

3.12 Quad-SPI memory interface (QUAD-SPI)

All devices embed a Quad-SPI memory interface, which is a specialized communication interface targeting single, dual or quad-SPI Flash memories. It can work in direct mode through registers, external Flash status register polling mode and memory mapped mode. Up to 256 Mbyte of external Flash memory are mapped. They can be accessed in 8, 16 or 32-bit mode. Code execution is also supported. The opcode and the frame format are fully programmable. Communication can be performed either in single data rate or dual data rate.

3.13 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 81 maskable interrupt channels plus the 16 interrupt lines of the Cortex[®]-M4 with FPU.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.14 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 21 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 114 GPIOs can be connected to the 16 external interrupt lines.

3.15 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy at 25 °C. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 100 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the three AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the three AHB buses and high-speed APB domains is 100 MHz. The maximum allowed frequency of the low-speed APB domain is 50 MHz.

The devices embed a dedicated PLL (PLL12S) which allows to achieve audio class performance. In this case, the I²S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

3.16 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash memory
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using one of the interface listed in the [Table 3](#) or the USB OTG FS in device mode through DFU (device firmware upgrade).

Table 3. Embedded bootloader interfaces

Package	USART1 PA9/ PA10	USART2 PD6/ PD5	USART3 PB11/ PB10	I2C1 PB6/ PB7	I2C2 PF0/ PF1	I2C3 PA8/ PB4	I2C FMP1 PB14/ PB15	SPI1 PA4/ PA5/ PA6/ PA7	SPI3 PA15/ PC10/ PC11/ PC12	SPI4 PE11/ PE12/ PE13/ PE14	CAN2 PB5/ PB13	USB PA11 /P12
UFQFPN48	Y	-	-	Y	-	Y	Y	Y	-	-	Y	Y
WLCSP64	Y	-	-	Y	-	Y	Y	Y	Y	-	Y	Y
LQFP64	Y	-	-	Y	-	Y	Y	Y	Y	-	Y	Y
LQFP100	Y	Y	-	Y	-	Y	Y	Y	Y	Y	Y	Y
LQFP144	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
UFBGA100	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y
UFBGA144	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y

For more detailed information on the bootloader, refer to Application Note: AN2606, *STM32™ microcontroller system memory boot mode*.

3.17 Power supply schemes

- $V_{DD} = 1.7$ to 3.6 V: external power supply for I/Os with the internal supervisor (POR/PDR) disabled, provided externally through V_{DD} pins. Requires the use of an external power supply supervisor connected to the V_{DD} and NRST pins.
- $V_{SSA}, V_{DDA} = 1.7$ to 3.6 V: external analog power supplies for ADC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively, with decoupling technique.

Note: The V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to [Section 3.18.2: Internal reset OFF](#)). Refer to [Table 4: Regulator ON/OFF and internal power supply supervisor availability](#) to identify the packages supporting this option.

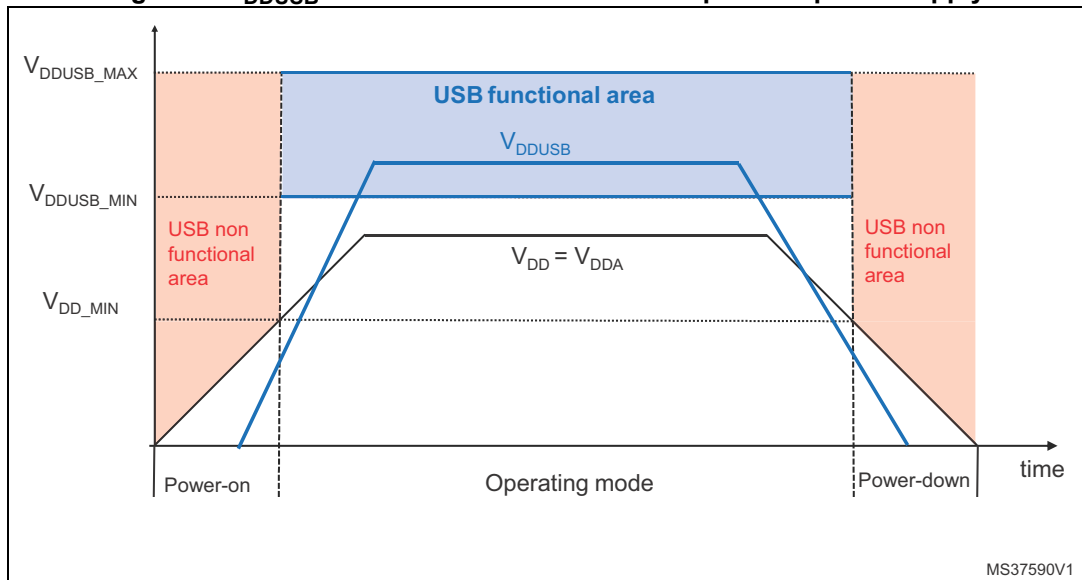
- $V_{BAT} = 1.65$ to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
- V_{DDUSB} can be connected either to V_{DD} or an external independent power supply (3.0 to 3.6 V) for USB transceivers.
For example, when device is powered at 1.8 V, an independent power supply 3.3V can be connected to V_{DDUSB} . When the V_{DDUSB} is connected to a separated power supply,

it is independent from V_{DD} or V_{DDA} but it must be the last supply to be provided and the first to disappear.

The following conditions V_{DDUSB} must be respected:

- During power-on phase ($V_{DD} < V_{DD_MIN}$), V_{DDUSB} should be always lower than V_{DD}
- During power-down phase ($V_{DD} < V_{DD_MIN}$), V_{DDUSB} should be always lower than V_{DD}
- V_{DDUSB} rising and falling time rate specifications must be respected.
- In operating mode phase, V_{DDUSB} could be lower or higher than V_{DD} :
 - If USB is used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DDUSB_MIN} and V_{DDUSB_MAX} .
 - If USB is not used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DD_MIN} and V_{DD_MAX} .

Figure 6. V_{DDUSB} connected to an external independent power supply



MS37590V1