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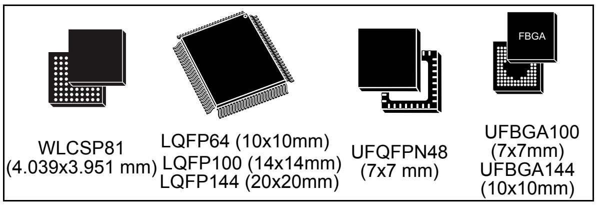
STM32F413xG STM32F413xH

ARM®-Cortex®-M4 32b MCU+FPU, 125 DMIPS, up to 1.5MB Flash, 320KB RAM, USB OTG FS, 1 ADC, 2 DACs, 2 DFSDMs

Datasheet - production data

Features

- Dynamic Efficiency Line with eBAM (enhanced Batch Acquisition Mode)
  - 1.7 V to 3.6 V power supply
  - -40 °C to 85/105/125 °C temperature range
- Core: ARM® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution from Flash memory, frequency up to 100 MHz, memory protection unit, 125 DMIPS/ 1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Memories
  - Up to 1.5 Mbytes of Flash memory
  - 320 Kbytes of SRAM
  - Flexible external static memory controller with up to 16-bit data bus: SRAM, PSRAM, NOR Flash memory
  - Dual mode Quad-SPI interface
- LCD parallel interface, 8080/6800 modes
- Clock, reset and supply management
  - 1.7 to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Power consumption
  - Run: 112 µA/MHz (peripheral off)
  - Stop (Flash in Stop mode, fast wakeup time): 42 µA Typ.; 80 µA max @25 °C
  - Stop (Flash in Deep power down mode, slow wakeup time): 15 µA Typ.; 46 µA max @25 °C
  - Standby without RTC: 1.1 µA Typ.; 14.7 µA max at @85 °C
  - V_{BAT} supply for RTC: 1 µA @25 °C
- 2x12-bit D/A converters
- 1×12-bit, 2.4 MSPS ADC: up to 16 channels
- 6x digital filters for sigma delta modulator, 12x PDM interfaces, with stereo microphone and sound source localization support
- General-purpose DMA: 16-stream DMA



- Up to 18 timers: up to twelve 16-bit timers, two 32-bit timers up to 100 MHz each with up to four IC/OC/PWM or pulse counter and quadrature (incremental) encoder input, two watchdog timers (independent and window), one SysTick timer, and a low-power timer
- Debug mode
  - Serial wire debug (SWD) & JTAG
  - Cortex®-M4 Embedded Trace Macrocell™
- Up to 114 I/O ports with interrupt capability
  - Up to 109 fast I/Os up to 100 MHz
  - Up to 114 five V-tolerant I/Os
- Up to 24 communication interfaces
  - Up to 4x I^2C interfaces (SMBus/PMBus)
  - Up to 10 UARTS: 4 USARTs / 6 UARTs (2 x 12.5 Mbit/s, 2 x 6.25 Mbit/s), ISO 7816 interface, LIN, IrDA, modem control)
  - Up to 5 SPI/I2Ss (up to 50 Mbit/s, SPI or I2S audio protocol), out of which 2 muxed full-duplex I2S interfaces
  - SDIO interface (SD/MMC/eMMC)
  - Advanced connectivity: USB 2.0 full-speed device/host/OTG controller with PHY
  - 3x CAN (2.0B Active)
  - 1xSAI
- True random number generator
- CRC calculation unit
- 96-bit unique ID
- RTC: subsecond accuracy, hardware calendar
- All packages are ECOPACK®2

Table 1. Device summary

Reference	Part number
STM32F413xH	STM32F413CH STM32F413MH STM32F413RH STM32F413VH STM32F413ZH
STM32F413xG	STM32F413CG STM32F413MG STM32F413RG STM32F413VG STM32F413ZG

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List of figures

1 Introduction

This datasheet provides the description of the STM32F413xG/H microcontrollers.

For information on the Cortex®-M4 core, please refer to the Cortex®-M4 programming manual (PM0214) available from www.st.com.

2 Description

The STM32F413xG/H devices are based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 100 MHz. Their Cortex®-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F413xG/H devices belong to the STM32F4 access product lines (with products combining power efficiency, performance and integration) while adding a new innovative feature called Batch Acquisition Mode (BAM) allowing to save even more power consumption during data batching.

The STM32F413xG/H devices incorporate high-speed embedded memories (up to 1.5 Mbytes of Flash memory, 320 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses, three AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer a 12-bit ADC, two 12-bit DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timer for motor control, two general-purpose 32-bit timers and a low power timer.

They also feature standard and advanced communication interfaces.

- Up to four I^2Cs, including one I^2C supporting Fast-Mode Plus
- Five SPIs
- Five I^2Ss out of which two are full duplex. To achieve audio class accuracy, the I^2S peripherals can be clocked via a dedicate internal audio PLL or via an external clock to allow synchronization.
- Four USARTs and six UARTs
- An SDIO/MMC interface
- An USB 2.0 OTG full-speed interface
- Three CANs
- An SAI.

In addition, the STM32F413xG/H devices embed advanced peripherals:

- A flexible static memory control interface (FSMC)
- A Quad-SPI memory interface
- Two digital filter for sigma modulator (DFSDM) supporting microphone MEMs and sound source localization, one with two filters and up to four inputs, and the second one with four filters and up to eight inputs

They are offered in 7 packages ranging from 48 to 144 pins. The set of available peripherals depends on the selected package. Refer to *Table 2: STM32F413xG/H features and peripheral counts* for the peripherals available for each part number.

The STM32F413xG/H operate in the – 40 to + 125 °C temperature range from a 1.7 (PDR OFF) to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

These features make the STM32F413xG/H microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile phone sensor hub
- Wearable devices
- Connected objects
- Wifi modules

Figure 4 shows the general block diagram of the devices.

Table 2. STM32F413xG/H features and peripheral counts

Peripherals		STM32F413xG					STM32F413xH				
Flash memory (Kbyte)		1024					1536				
SRAM (Kbyte)	System	320 (256 + 64)					320 (256 + 64)				
Quad-SPI memory interface		-	1				-	1			
FSMC memory controller		-	1(1)	1(1)	1(1)	1	-	1(1)	1(1)	1(1)	1
FSMC LCD parallel interface Data bus size		-	8	16			-	8	16		
Timers	General-purpose	10(2)	10	10(3)	10		10(2)	10	10(3)	10	
	Advanced-control	2(4)	2				2(4)	2			
	Basic	2					2				
	Low-power timer	1					1				
Random number generator		1					1				
Comm. interfaces	SPI/ I^2S	5/5 (2 full duplex)					5/5 (2 full duplex)				
	I^2C	3					3				
	I^2CFMP	1					1				
	USART/ UART	3/3	4/3		4/6		3/3	4/3		4/6	
	SDIO/MMC	1					1				
	USB/OTG FS Dual power rail	1 No		1 Yes	1 No	1 Yes	1 No		1 Yes	1 No	1 Yes
	CAN	3					3				
	SAI	1					1				
Number of digital Filters for Sigma-delta modulator		6					6				
Number of channels		7	11	12			7	11	12		
GPIOs		36	50	60	81	114	36	50	60	81	114
12-bit ADC		1					1				
Number of channels		10	16				10	16			
12-bit DAC		Yes					Yes				
Number of channels		2					2				
Maximum CPU frequency		100 MHz					100 MHz				
Operating voltage		1.7 to 3.6 V					1.7 to 3.6 V				
Operating temperatures		Ambient temperatures: – 40 to +85 °C / – 40 to +105 °C / – 40 to +125 °C					Ambient temperatures: – 40 to +85 °C / – 40 to +105 °C / – 40 to +125 °C				
		Junction temperature: –40 to + 130 °C					Junction temperature: –40 to + 130 °C				
Package		UFQFPN 48	LQFP 64	WLCSP 81	UFBGA/ LQFP100	UFBGA/ LQFP144	UFQFPN 48	LQFP64	WLCSP 81	UFBGA/ LQFP100	UFBGA/ LQFP144

1. 64 pins package: support only 8 bits multiplexed mode interface
   81 pins package: support 1 external memory of up to 64KB in multiplexed mode
   100 pins: support 2 external memories of up to 64MB in multiplexed mode
   Refer to *Table 11: FSMC pin definition* for more detailed information
2. 48 pins packages: TIM3 and TIM4: ETR pin not available.
3. 81 pins packages: TIM4: ETR pin not available.
4. 48 pins packages: TIM8:CH1, CH2, CH3 and CH4 pins not available.

2.1 Compatibility with STM32F4 series

The STM32F413xG/H are fully software and feature compatible with the STM32F4 series (STM32F42x, STM32F401, STM32F43x, STM32F41x, STM32F405 and STM32F407)

The STM32F413xG/H can be used as drop-in replacement of the other STM32F4 products but some slight changes have to be done on the PCB board.

Figure 1. Compatible board design for LQFP100 package

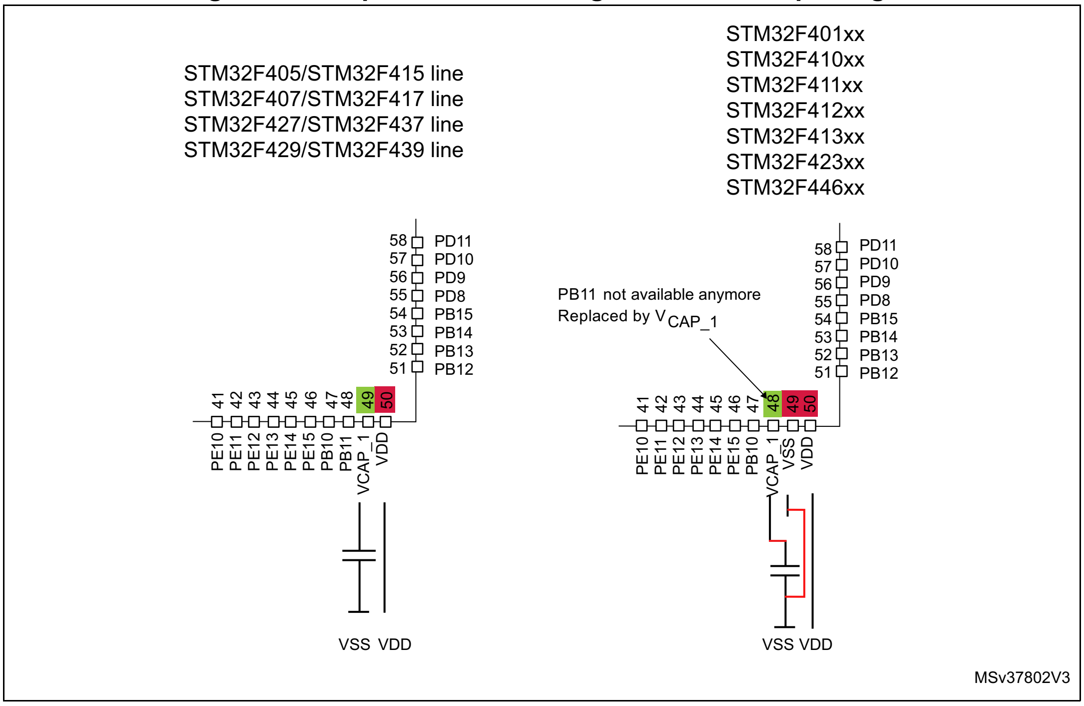


Figure 2. Compatible board design for LQFP64 package

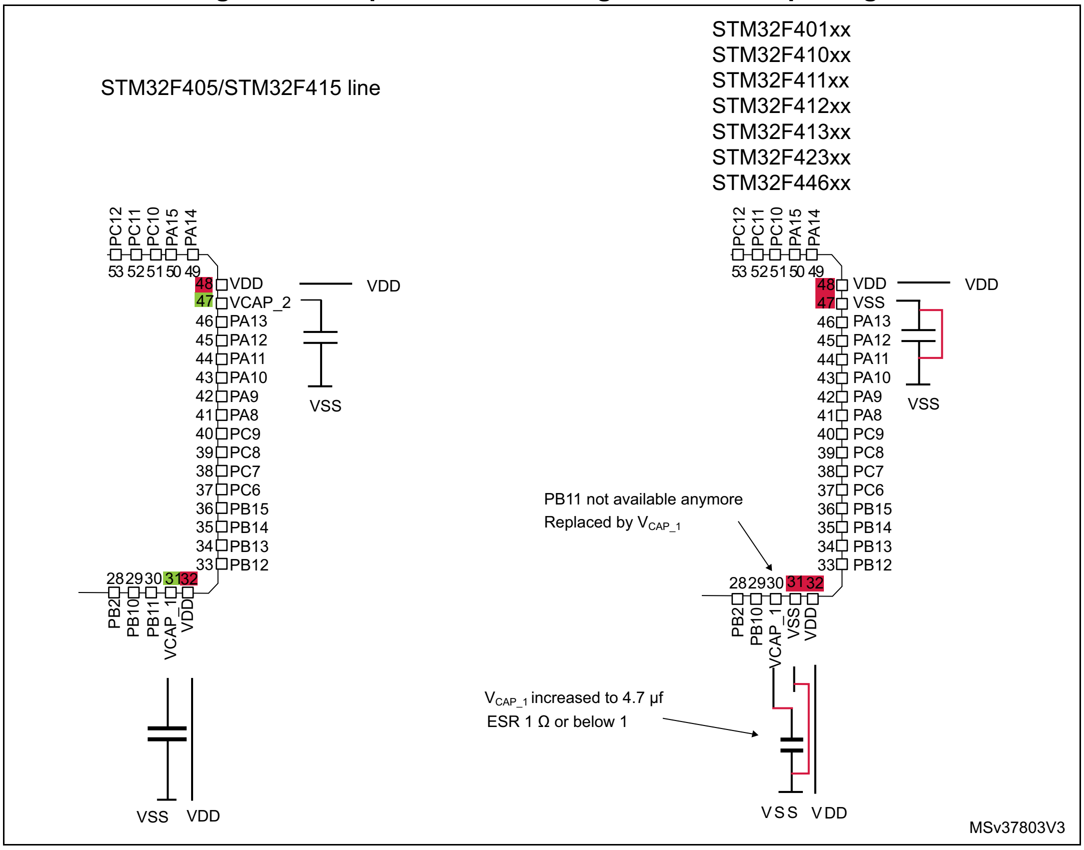


Figure 3. Compatible board design for LQFP144 package

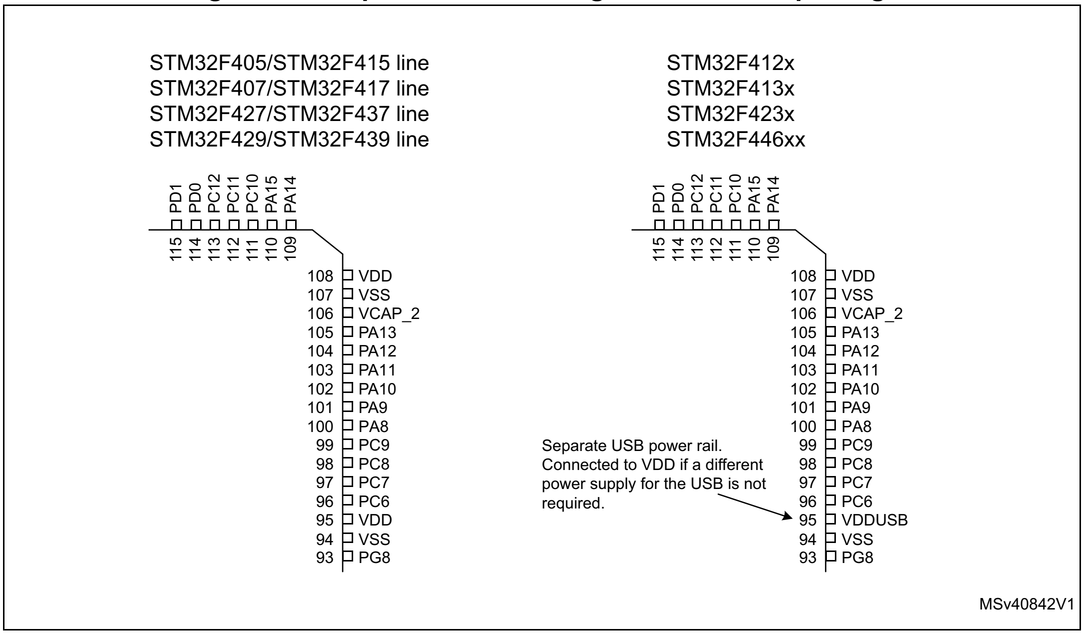
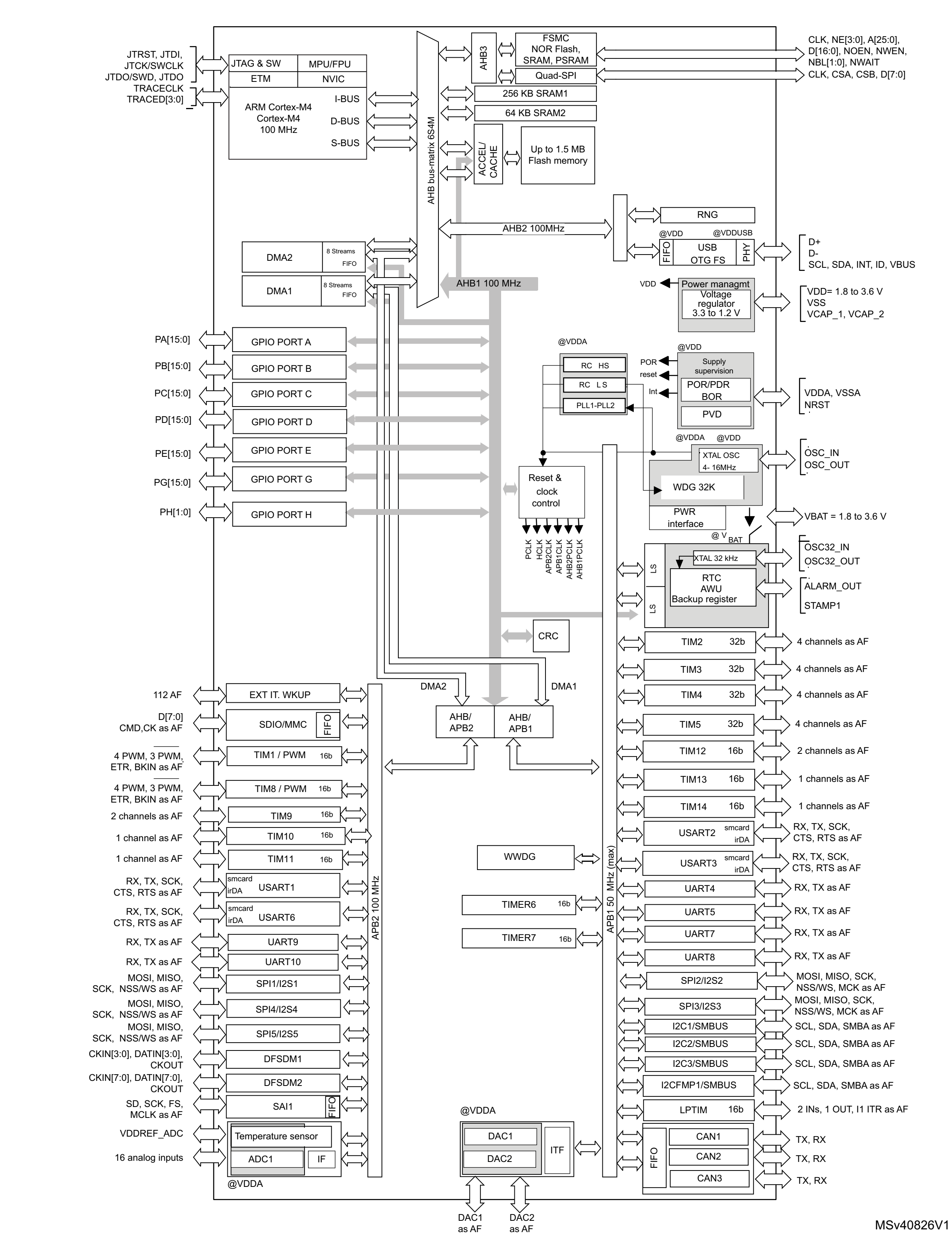


Figure 4. STM32F413xG/H block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 100 MHz, while the timers connected to APB1 are clocked from TIMxCLK up to 50 MHz.

3 Functional overview

3.1 ARM® Cortex®-M4 with FPU core with embedded Flash and SRAM

The ARM® Cortex®-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F413xG/H devices are compatible with all ARM tools and software.

Figure 4 shows the general block diagram of the STM32F413xG/H.

Note: *Cortex®-M4 with FPU is binary compatible with Cortex®-M3.*

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 with FPU processors. It balances the inherent performance advantage of the ARM® Cortex®-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 125 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 100 MHz.

3.3 Enhanced Batch Acquisition mode (eBAM)

The Batch acquisition mode allows enhanced power efficiency during data batching. It enables data acquisition through any communication peripherals directly to memory using the DMA in reduced power consumption as well as data processing while the rest of the system is in low-power mode (including the Flash and ART). For example in an audio system, a smart combination of PDM audio sample acquisition and processing from the DFSDM directly to RAM (Flash and ART™ stopped) with the DMA using BAM followed by some very short processing from Flash allows to drastically reduce the power consumption of the application.

The BAM has been enhanced by adding SRAM2 that allows SRAM code to be executed through the Ibus and Dbus, thus improving code execution performance.

A dedicated application note (AN4515) describes how to implement the STM32F413xG/H BAM to allow the best power efficiency.

3.4 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 byte and the whole 4 Gbyte of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.5 Embedded Flash memory

The devices embed up to 1.5 Mbytes of Flash memory available for storing programs and data, plus 512 bytes of one-time programmable (OTP) memory organized in 16 blocks of 32 bytes, each which can be independently locked.

The user Flash memory area can be protected against read operations by an entrusted code (read protection or RDP). Different protection levels are available. The user Flash memory is divided into sectors, which can be individually protected against write operation. Flash sectors can also be protected individually against D-bus read accesses by using the proprietary readout protection (PCROP).

Refer to the product line reference manual for additional information on OTP area and protection features.

To optimize the power consumption the Flash memory can also be switched off in Run or in Sleep mode (see *Section 3.20: Low-power modes*).

Two modes are available: Flash in Stop mode or in DeepSleep mode (trade off between power saving and startup time.

Before disabling the Flash, the code must be executed from the internal RAM.

3.6 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

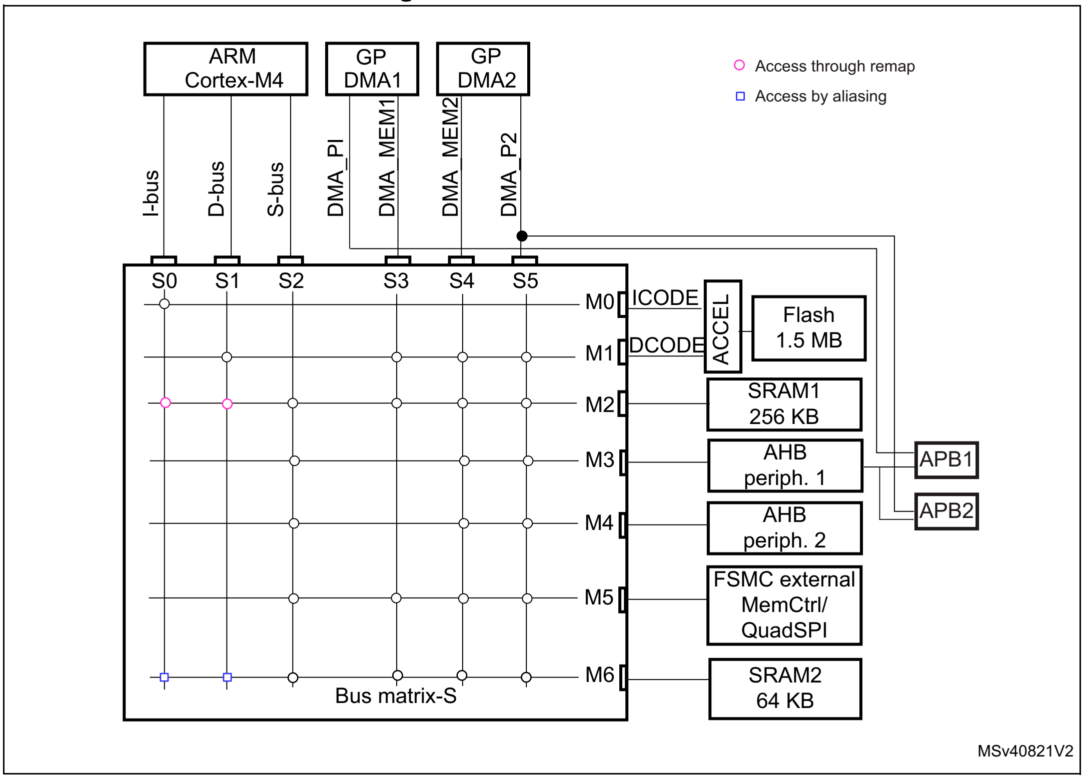
3.7 Embedded SRAM

All devices embed 320 Kbytes of system SRAM which can be accessed (read/write) at CPU clock speed with 0 wait states.

3.8 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs) and the slaves (Flash memory, RAM, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 5. Multi-AHB matrix



CPU can access SRAM1 memory via S-bus, when SRAM1 is mapped at the address range: 0x2000 0000 to 0x2003 FFFF.

CPU can access SRAM2 memory via S-bus, when SRAM2 is mapped at the address range: 0x2004 0000 to 0x2004 FFFF.

CPU can access SRAM1 memory via I-bus and D-bus, when SRAM1 is remapped at address 0x0000 0000 either by booting from RAM memory or by the remap mode.

CPU can access SRAM2 memory via I-bus and D-bus, when SRAM2 is mapped at the address range: 0x1000 0000 to 0x1000 FFFF.

Performance boosts up, when the CPU access SRAM memory via the I-bus.

3.9 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I^2S
- I^2C and I^2CFMP
- USART
- General-purpose, basic and advanced-control timers TIMx
- SD/SDIO/MMC/eMMC host interface
- Quad-SPI
- ADC
- DAC
- Digital Filter for sigma-delta modulator (DFSDM) with a separate stream for each filter
- SAI.

3.10 Flexible static memory controller (FSMC)

The Flexible static memory controller (FSMC) includes a NOR/PSRAM memory controller. It features four Chip Select outputs supporting the following modes: SRAM, PSRAM and NOR Flash memory.

The main functions are:

- 8-,16-bit data bus width
- Write FIFO
- Maximum FSMC_CLK frequency for synchronous accesses is 90 MHz.

LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

3.11 Quad-SPI memory interface (QUAD-SPI)

All devices embed a Quad-SPI memory interface, which is a specialized communication interface targeting single, dual or quad-SPI Flash memories. It can work in direct mode through registers, external Flash status register polling mode and memory mapped mode. Up to 256 Mbyte of external Flash memory are mapped. They can be accessed in 8, 16 or 32-bit mode. Code execution is also supported. The opcode and the frame format are fully programmable. Communication can be performed either in single data rate or dual data rate.

3.12 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 102 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.13 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 24 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 114 GPIOs can be connected to the 16 external interrupt lines.

3.14 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy at 25 °C. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 100 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the three AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the three AHB buses and high-speed APB domains is 100 MHz. The maximum allowed frequency of the low-speed APB domain is 50 MHz.

The devices embed a dedicated PLL (PLLI2S) which allows to achieve audio class performance. In this case, the I^2S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

3.15 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash memory
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using one of the interface listed in the *Table 3* or the USB OTG FS in device mode through DFU (device firmware upgrade).

Table 3. Embedded bootloader interfaces

Package	USART1 PA9/ PA10	USART2 PD6/ PD5	USART3 PB11/ PB10	I2C1 PB6/ PB7	I2C2 PF0/ PF1	I2C3 PA8/ PB4	I2C FMP1 PB14/ PB15	SPI1 PA4/ PA5/ PA6/ PA7	SPI3 PA15/ PC10/ PC11/ PC12	SPI4 PE11/ PE12/ PE13/ PE14	CAN2 PB5/ PB13	USB PA11 /P12
UFQFPN48	Y	-	-	Y	-	Y	Y	Y	-	-	Y	Y
LQFP64	Y	-	-	Y	-	Y	Y	Y	Y	-	Y	Y
WLCSP81	Y	-	-	Y	-	Y	Y	Y	Y	Y	Y	Y
LQFP100	Y	Y	-	Y	-	Y	Y	Y	Y	Y	Y	Y
LQFP144	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
UFBGA100	Y	Y	Y	Y	-	Y	Y	Y	Y	Y	Y	Y
UFBGA144	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y

For more detailed information on the bootloader, refer to Application Note: AN2606, *STM32™ microcontroller system memory boot mode*.

3.16 Power supply schemes

- V_{DD} = 1.7 to 3.6 V: external power supply for I/Os with the internal supervisor (POR/PDR) disabled, provided externally through V_{DD} pins. Requires the use of an external power supply supervisor connected to the V_{DD} and NRST pins.
- V_{SSA}, V_{DDA} = 1.7 to 3.6 V: external analog power supplies for ADC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively, with decoupling technique.

Note: The V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to Section 3.17.2: Internal reset OFF). Refer to Table 4: Regulator ON/OFF and internal power supply supervisor availability to identify the packages supporting this option.

- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
- V_{DDUSB} can be connected either to VDD or an external independent power supply (3.0 to 3.6 V) for USB transceivers.

  For example, when device is powered at 1.8 V, an independent power supply 3.3V can be connected to V_{DDUSB}. When the V_{DDUSB} is connected to a separated power supply, it is independent from V_{DD} or V_{DDA} but it must be the last supply to be provided and the first to disappear.

The following conditions VDDUSB must be respected:

- During power-on phase ($V_{DD} < V_{DD\_MIN}$), V_{DDUSB} should be always lower than V_{DD}
- During power-down phase ($V_{DD} < V_{DD\_MIN}$), V_{DDUSB} should be always lower than V_{DD}
- V_{DDUSB} rising and falling time rate specifications must be respected.
- In operating mode phase, V_{DDUSB} could be lower or higher than VDD:
  - If USB is used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DDUSB_MIN} and V_{DDUSB_MAX}.
  - If USB is not used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DD_MIN} and V_{DD_MAX}.