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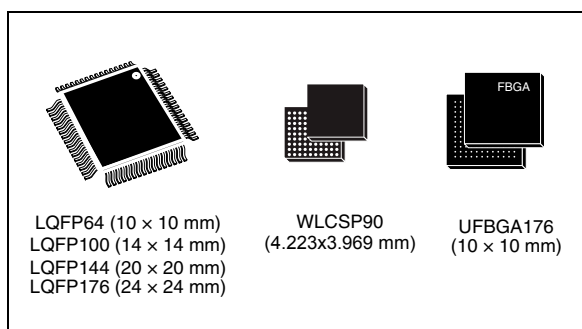


ARM Cortex-M4 32b MCU+FPU, 210DMIPS, up to 1MB Flash/192+4KB RAM, crypto, USB OTG HS/FS, Ethernet, 17 TIMs, 3 ADCs, 15 comm. interfaces & camera

Datasheet - production data

Features

- Core: ARM® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution from Flash memory, frequency up to 168 MHz, memory protection unit, 210 DMIPS/1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Memories
 - Up to 1 Mbyte of Flash memory
 - Up to 192+4 Kbytes of SRAM including 64-Kbyte of CCM (core coupled memory) data RAM
 - Flexible static memory controller supporting Compact Flash, SRAM, PSRAM, NOR and NAND memories
 - LCD parallel interface, 8080/6800 modes
 - Clock, reset and supply management
 - 1.8 V to 3.6 V application supply and I/Os
 - POR, PDR, PVD and BOR
 - 4-to-26 MHz crystal oscillator
 - Internal 16 MHz factory-trimmed RC (1% accuracy)
 - 32 kHz oscillator for RTC with calibration
 - Internal 32 kHz RC with calibration
 - Low-power operation
 - Sleep, Stop and Standby modes
 - V_{BAT} supply for RTC, 20×32 bit backup registers + optional 4 KB backup SRAM
 - 3×12-bit, 2.4 MSPS A/D converters: up to 24 channels and 7.2 MSPS in triple interleaved mode
 - 2×12-bit D/A converters
 - General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Up to 17 timers: up to twelve 16-bit and two 32-bit timers up to 168 MHz, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
- Debug mode
 - Serial wire debug (SWD) & JTAG interfaces
 - Cortex-M4 Embedded Trace Macrocell™
- Up to 140 I/O ports with interrupt capability
 - Up to 136 fast I/Os up to 84 MHz
 - Up to 138 5 V-tolerant I/Os
- Up to 15 communication interfaces
 - Up to 3 × I²C interfaces (SMBus/PMBus)
 - Up to 4 USARTs/2 UARTs (10.5 Mbit/s, ISO 7816 interface, LIN, IrDA, modem control)
 - Up to 3 SPIs (42 Mbits/s), 2 with muxed full-duplex I²S to achieve audio class accuracy via internal audio PLL or external clock
 - 2 × CAN interfaces (2.0B Active)
 - SDIO interface
- Advanced connectivity
 - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
 - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
 - 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII



- 8- to 14-bit parallel camera interface up to 54 Mbytes/s
- Cryptographic acceleration: hardware acceleration for AES 128, 192, 256, Triple DES, HASH (MD5, SHA-1), and HMAC
- True random number generator
- CRC calculation unit
- 96-bit unique ID
- RTC: subsecond accuracy, hardware calendar

Table 1. Device summary

Reference	Part number
STM32F415xx	STM32F415RG, STM32F415VG, STM32F415ZG, STM32F415OG
STM32F417xx	STM32F417VG, STM32F417IG, STM32F417ZG, STM32F417VE, STM32F417ZE, STM32F417IE

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1 Introduction

This datasheet provides the description of the STM32F415xx and STM32F417xx lines of microcontrollers. For more details on the whole STMicroelectronics STM32™ family, please refer to [Section 2.1: Full compatibility throughout the family](#).

The STM32F415xx and STM32F417xx datasheet should be read in conjunction with the STM32F4xx reference manual which is available from the STMicroelectronics website www.st.com.

For information on the Cortex®-M4 core, please refer to the Cortex®-M4 programming manual (PM0214) available from www.st.com.

2 Description

The STM32F415xx and STM32F417xx family is based on the high-performance ARM[®] Cortex[®]-M4 32-bit RISC core operating at a frequency of up to 168 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F415xx and STM32F417xx family incorporates high-speed embedded memories (Flash memory up to 1 Mbyte, up to 192 Kbytes of SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, three AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers, a true random number generator (RNG), and a cryptographic acceleration cell. They also feature standard and advanced communication interfaces.

- Up to three I²Cs
- Three SPIs, two I²Ss full duplex. To achieve audio class accuracy, the I2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus two UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI),
- Two CANs
- An SDIO/MMC interface
- Ethernet and the camera interface available on STM32F417xx devices only.

New advanced peripherals include an SDIO, an enhanced flexible static memory control (FSMC) interface (for devices offered in packages of 100 pins and more), a camera interface for CMOS sensors and a cryptographic acceleration cell. Refer to [Table 2: STM32F415xx and STM32F417xx: features and peripheral counts](#) for the list of peripherals available on each part number.

The STM32F415xx and STM32F417xx family operates in the –40 to +105 °C temperature range from a 1.8 to 3.6 V power supply. The supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor: refer to [Section : Internal reset OFF](#). A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F415xx and STM32F417xx family offers devices in various packages ranging from 64 pins to 176 pins. The set of included peripherals changes with the device chosen.

These features make the STM32F415xx and STM32F417xx microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances



Figure 5 shows the general block diagram of the device family.

Table 2. STM32F415xx and STM32F417xx: features and peripheral counts

Peripherals		STM32F415RG	STM32F415OG	STM32F415VG	STM32F415ZG	STM32F417Vx		STM32F417Zx		STM32F417Ix	
Flash memory in Kbytes		1024				512	1024	512	1024	512	1024
SRAM in Kbytes	System	192(112+16+64)									
	Backup	4									
FSMC memory controller		No	Yes ⁽¹⁾								
Ethernet		No				Yes					
Timers	General-purpose	10									
	Advanced-control	2									
	Basic	2									
	IWDG	Yes									
	WWDG	Yes									
	RTC	Yes									
Random number generator		Yes									
Communication interfaces	SPI / I ² S	3/2 (full duplex) ⁽²⁾									
	I ² C	3									
	USART/UART	4/2									
	USB OTG FS	Yes									
	USB OTG HS	Yes									
	CAN	2									
	SDIO	Yes									
Camera interface		No				Yes					
Cryptography		Yes									


Table 2. STM32F415xx and STM32F417xx: features and peripheral counts

Peripherals	STM32F415RG	STM32F415OG	STM32F415VG	STM32F415ZG	STM32F417Vx	STM32F417Zx	STM32F417Ix
GPIOs	51	72	82	114	82	114	140
12-bit ADC	3						
Number of channels	16	13	16	24	16	24	24
12-bit DAC	Yes						
Number of channels	2						
Maximum CPU frequency	168 MHz						
Operating voltage	1.8 to 3.6 V ⁽³⁾						
Operating temperatures	Ambient temperatures: –40 to +85 °C / –40 to +105 °C						
	Junction temperature: –40 to + 125 °C						
Package	LQFP64	WLCSP90	LQFP100	LQFP144	LQFP100	LQFP144	UFBGA176 LQFP176

1. For the LQFP100 and WLCSP90 packages, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to [Section : Internal reset OFF](#)).

2.1 Full compatibility throughout the family

The STM32F415xx and STM32F417xx are part of the STM32F4 family. They are fully pin-to-pin, software and feature compatible with the STM32F2xx devices, allowing the user to try different memory densities, peripherals, and performances (FPU, higher frequency) for a greater degree of freedom during the development cycle.

The STM32F415xx and STM32F417xx devices maintain a close compatibility with the whole STM32F10xxx family. All functional pins are pin-to-pin compatible. The STM32F415xx and STM32F417xx, however, are not drop-in replacements for the STM32F10xxx devices: the two families do not have the same power scheme, and so their power pins are different. Nonetheless, transition from the STM32F10xxx to the STM32F41xxx family remains simple as only a few pins are impacted.

Figure 4, Figure 3, Figure 2, and Figure 1 give compatible board designs between the STM32F41xxx, STM32F2, and STM32F10xxx families.

Figure 1. Compatible board design between STM32F10xx/STM32F41xxx for LQFP64

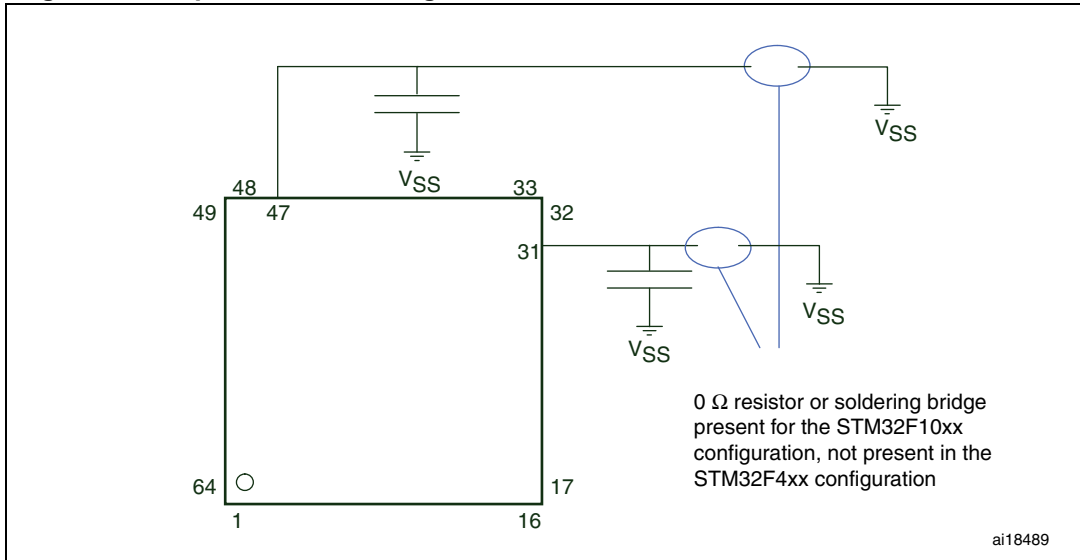


Figure 2. Compatible board design STM32F10xx/STM32F2/STM32F41xxx for LQFP100 package

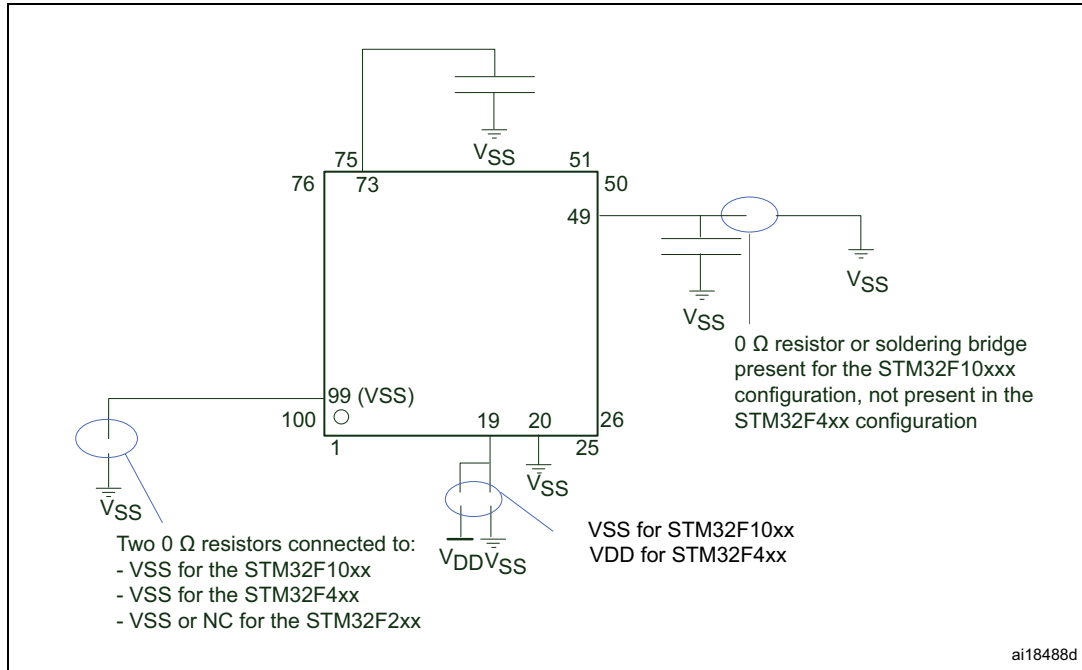


Figure 3. Compatible board design between STM32F10xx/STM32F2/STM32F41xxx for LQFP144 package

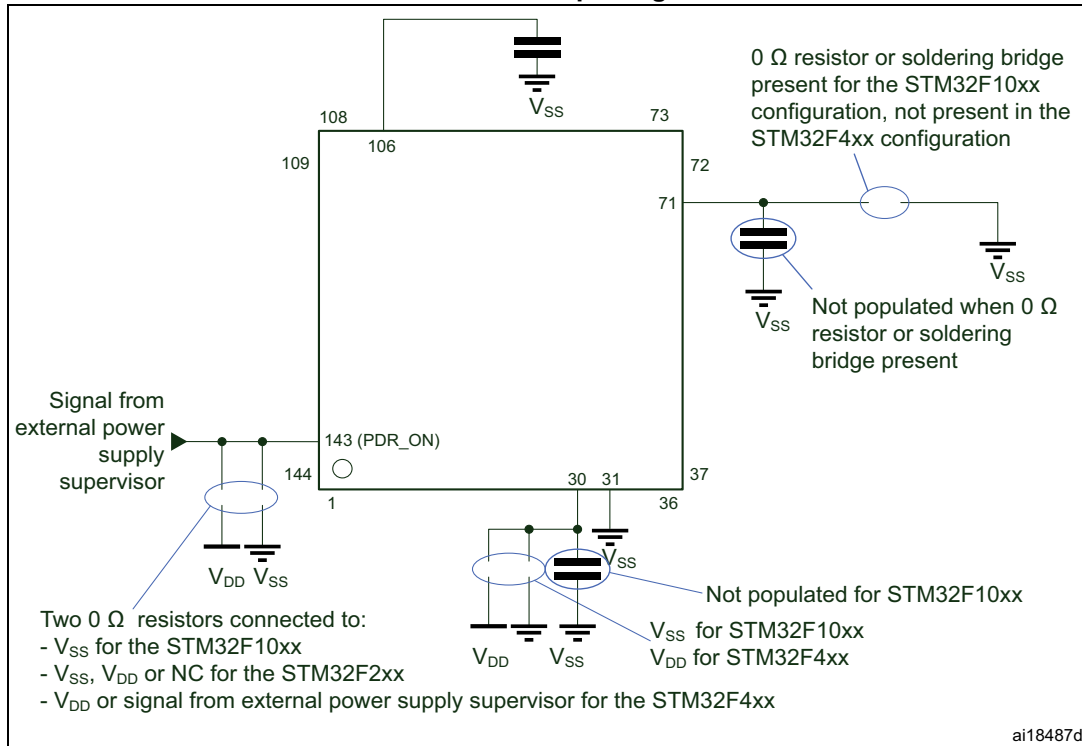
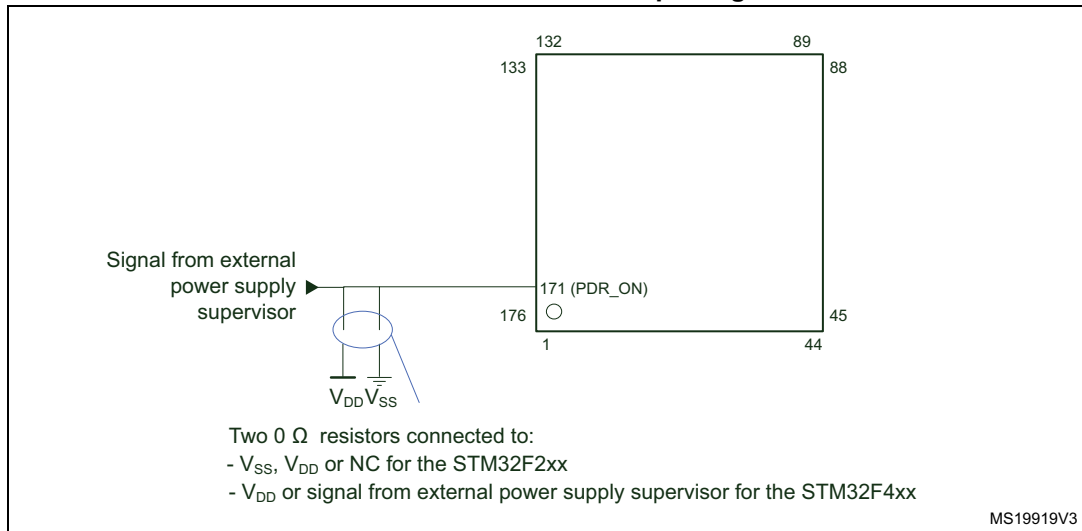
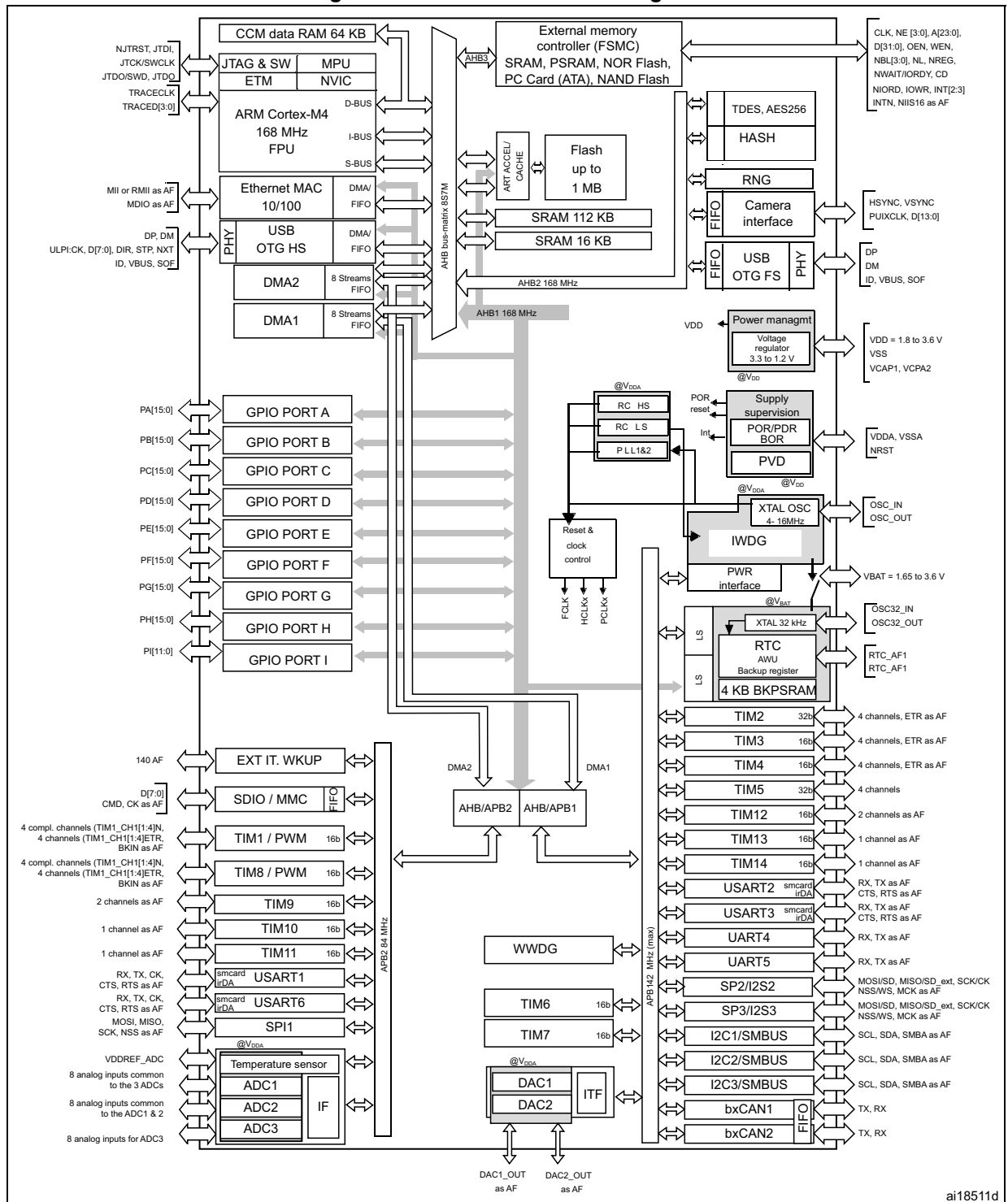


Figure 4. Compatible board design between STM32F2 and STM32F41xxx for LQFP176 and BGA176 packages



2.2 Device overview

Figure 5. STM32F41xxx block diagram



1. The camera interface and ethernet are available only on STM32F417xx devices.

2.2.1 ARM[®] Cortex[®]-M4 core with FPU and embedded Flash and SRAM

The ARM Cortex-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M4 32-bit RISC processor with FPU features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F415xx and STM32F417xx family is compatible with all ARM tools and software.

[Figure 5](#) shows the general block diagram of the STM32F41xxx family.

Note: Cortex-M4 with FPU is binary compatible with Cortex-M3.

2.2.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM[®] Cortex[®]-M4 with FPU processors. It balances the inherent performance advantage of the ARM Cortex-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 210 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 168 MHz.

2.2.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.2.4 Embedded Flash memory

The STM32F41xxx devices embed a Flash memory of 512 Kbytes or 1 Mbytes available for storing programs and data.

2.2.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.2.6 Embedded SRAM

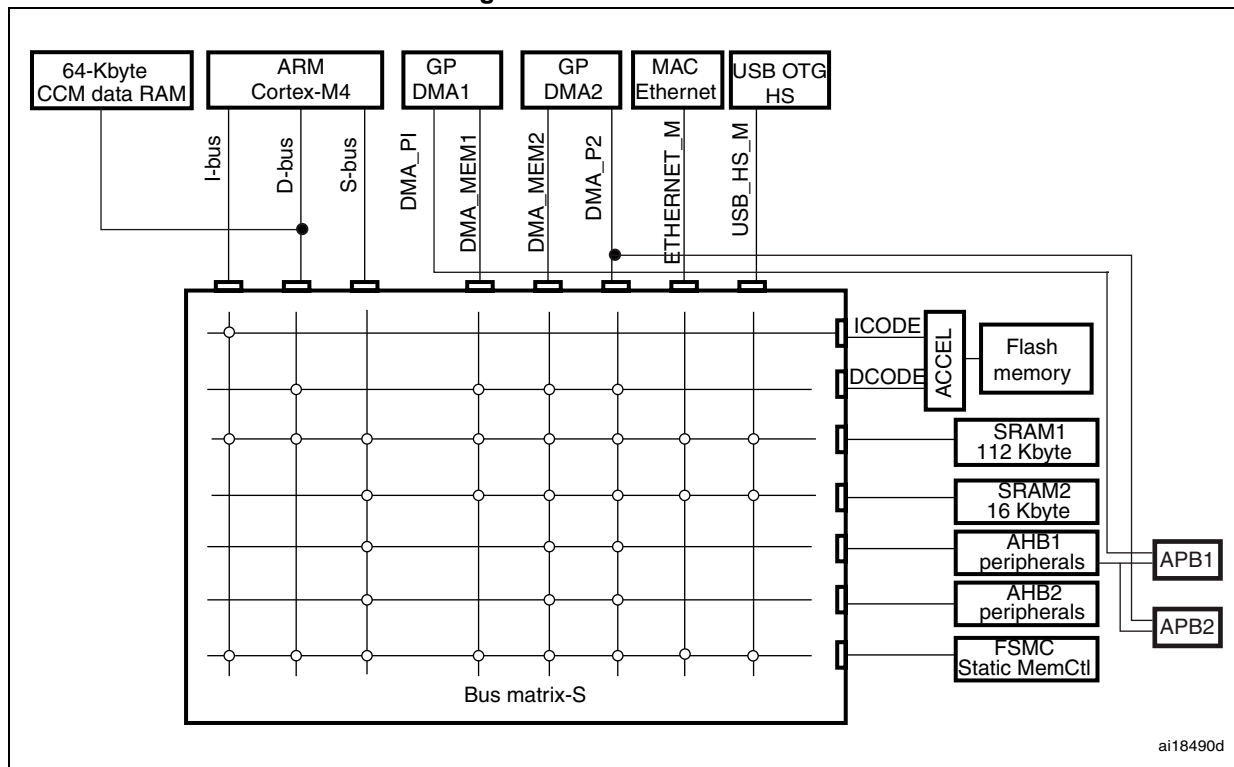
All STM32F41xxx products embed:

- Up to 192 Kbytes of system SRAM including 64 Kbytes of CCM (core coupled memory) data RAM
RAM memory is accessed (read/write) at CPU clock speed with 0 wait states.
- 4 Kbytes of backup SRAM
This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or VBAT mode.

2.2.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS) and the slaves (Flash memory, RAM, FSMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 6. Multi-AHB matrix



2.2.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I²S
- I²C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDIO
- Cryptographic acceleration
- Camera interface (DCMI)
- ADC.

2.2.9 Flexible static memory controller (FSMC)

The FSMC is embedded in the STM32F415xx and STM32F417xx family. It has four Chip Select outputs supporting the following modes: PCCard/Compact Flash, SRAM, PSRAM, NOR Flash and NAND Flash.

Functionality overview:

- Write FIFO
- Maximum FSMC_CLK frequency for synchronous accesses is 60 MHz.

LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

2.2.10 Nested vectored interrupt controller (NVIC)

The STM32F415xx and STM32F417xx embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 82 maskable interrupt channels plus the 16 interrupt lines of the Cortex[®]-M4 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

2.2.11 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 140 GPIOs can be connected to the 16 external interrupt lines.

2.2.12 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy over the full temperature range. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 168 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the three AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the three AHB buses is 168 MHz while the maximum frequency of the high-speed APB domains is 84 MHz. The maximum allowed frequency of the low-speed APB domain is 42 MHz.

The devices embed a dedicated PLL (PLLI2S) which allows to achieve audio class performance. In this case, the I²S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

2.2.13 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART3 (PC10/PC11 or PB10/PB11), CAN2 (PB5/PB13), USB OTG FS in Device mode (PA11/PA12) through DFU (device firmware upgrade).

2.2.14 Power supply schemes

- $V_{DD} = 1.8$ to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins.
- $V_{SSA}, V_{DDA} = 1.8$ to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.
- $V_{BAT} = 1.65$ to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Refer to [Figure 21: Power supply scheme](#) for more details.