



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

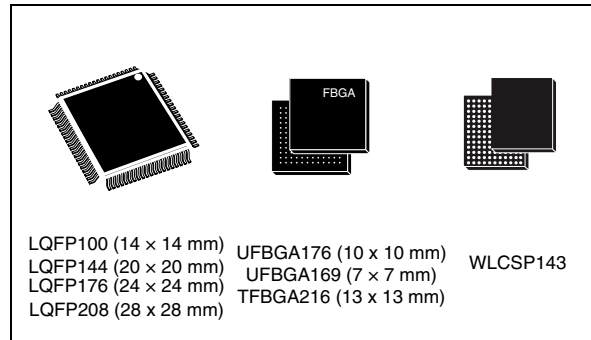


ARM Cortex-M4 32b MCU+FPU, 225DMIPS, up to 2MB Flash/256+4KB RAM, USB OTG HS/FS, Ethernet, 17 TIMs, 3 ADCs, 20 comm. interfaces, camera & LCD-TFT

Datasheet - production data

Features

- Core: ARM® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution from Flash memory, frequency up to 180 MHz, MPU, 225 DMIPS/1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Memories
 - Up to 2 MB of Flash memory organized into two banks allowing read-while-write
 - Up to 256+4 KB of SRAM including 64-KB of CCM (core coupled memory) data RAM
 - Flexible external memory controller with up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPDDR SDRAM, Compact Flash/NOR/NAND memories
- LCD parallel interface, 8080/6800 modes
- LCD-TFT controller up to XGA resolution with dedicated Chrom-ART Accelerator™ for enhanced graphic content creation (DMA2D)
- Clock, reset and supply management
 - 1.7 V to 3.6 V application supply and I/Os
 - POR, PDR, PVD and BOR
 - 4-to-26 MHz crystal oscillator
 - Internal 16 MHz factory-trimmed RC (1% accuracy)
 - 32 kHz oscillator for RTC with calibration
 - Internal 32 kHz RC with calibration
- Low power
 - Sleep, Stop and Standby modes
 - V_{BAT} supply for RTC, 20×32 bit backup registers + optional 4 KB backup SRAM
- 3×12-bit, 2.4 MSPS ADC: up to 24 channels and 7.2 MSPS in triple interleaved mode
- 2×12-bit D/A converters
- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Up to 17 timers: up to twelve 16-bit and two 32-bit timers up to 180 MHz, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
- Debug mode
 - SWD & JTAG interfaces
 - Cortex-M4 Trace Macrocell™



- Up to 168 I/O ports with interrupt capability
 - Up to 164 fast I/Os up to 90 MHz
 - Up to 166 5 V-tolerant I/Os
- Up to 21 communication interfaces
 - Up to 3 × I²C interfaces (SMBus/PMBus)
 - Up to 4 USARTs/4 UARTs (11.25 Mbit/s, ISO7816 interface, LIN, IrDA, modem control)
 - Up to 6 SPIs (45 Mbits/s), 2 with muxed full-duplex I²S for audio class accuracy via internal audio PLL or external clock
 - 1 × SAI (serial audio interface)
 - 2 × CAN (2.0B Active) and SDIO interface
- Advanced connectivity
 - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
 - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
 - 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII
- 8- to 14-bit parallel camera interface up to 54 Mbytes/s
- True random number generator
- CRC calculation unit
- RTC: subsecond accuracy, hardware calendar
- 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM32F427xx	STM32F427VG, STM32F427ZG, STM32F427IG, STM32F427AG, STM32F427VI, STM32F427ZI, STM32F427II, STM32F427AI
STM32F429xx	STM32F429VG, STM32F429ZG, STM32F429IG, STM32F429BG, STM32F429NG, STM32F429AG, STM32F429VI, STM32F429ZI, STM32F429II,, STM32F429BI, STM32F429NI, STM32F429AI, STM32F429VE, STM32F429ZE, STM32F429IE, STM32F429BE, STM32F429NE

Contents

1	Introduction	13
2	Description	14
2.1	Full compatibility throughout the family	17
3	Functional overview	20
3.1	ARM® Cortex®-M4 with FPU and embedded Flash and SRAM	20
3.2	Adaptive real-time memory accelerator (ART Accelerator™)	20
3.3	Memory protection unit	20
3.4	Embedded Flash memory	21
3.5	CRC (cyclic redundancy check) calculation unit	21
3.6	Embedded SRAM	21
3.7	Multi-AHB bus matrix	21
3.8	DMA controller (DMA)	22
3.9	Flexible memory controller (FMC)	23
3.10	LCD-TFT controller (available only on STM32F429xx)	23
3.11	Chrom-ART Accelerator™ (DMA2D)	24
3.12	Nested vectored interrupt controller (NVIC)	24
3.13	External interrupt/event controller (EXTI)	24
3.14	Clocks and startup	24
3.15	Boot modes	25
3.16	Power supply schemes	25
3.17	Power supply supervisor	25
3.17.1	Internal reset ON	25
3.17.2	Internal reset OFF	26
3.18	Voltage regulator	27
3.18.1	Regulator ON	27
3.18.2	Regulator OFF	28
3.18.3	Regulator ON/OFF and internal reset ON/OFF availability	31
3.19	Real-time clock (RTC), backup SRAM and backup registers	31
3.20	Low-power modes	32
3.21	V _{BAT} operation	33

3.22	Timers and watchdogs	33
3.22.1	Advanced-control timers (TIM1, TIM8)	35
3.22.2	General-purpose timers (TIMx)	35
3.22.3	Basic timers TIM6 and TIM7	35
3.22.4	Independent watchdog	36
3.22.5	Window watchdog	36
3.22.6	SysTick timer	36
3.23	Inter-integrated circuit interface (I ² C)	36
3.24	Universal synchronous/asynchronous receiver transmitters (USART)	36
3.25	Serial peripheral interface (SPI)	37
3.26	Inter-integrated sound (I ² S)	38
3.27	Serial Audio interface (SAI1)	38
3.28	Audio PLL (PLLI2S)	38
3.29	Audio and LCD PLL(PLLSAI)	38
3.30	Secure digital input/output interface (SDIO)	39
3.31	Ethernet MAC interface with dedicated DMA and IEEE 1588 support	39
3.32	Controller area network (bxCAN)	39
3.33	Universal serial bus on-the-go full-speed (OTG_FS)	40
3.34	Universal serial bus on-the-go high-speed (OTG_HS)	40
3.35	Digital camera interface (DCMI)	41
3.36	Random number generator (RNG)	41
3.37	General-purpose input/outputs (GPIOs)	41
3.38	Analog-to-digital converters (ADCs)	41
3.39	Temperature sensor	42
3.40	Digital-to-analog converter (DAC)	42
3.41	Serial wire JTAG debug port (SWJ-DP)	42
3.42	Embedded Trace Macrocell™	43
4	Pinouts and pin description	44
5	Memory mapping	85
6	Electrical characteristics	90
6.1	Parameter conditions	90
6.1.1	Minimum and maximum values	90

6.1.2	Typical values	90
6.1.3	Typical curves	90
6.1.4	Loading capacitor	90
6.1.5	Pin input voltage	90
6.1.6	Power supply scheme	91
6.1.7	Current consumption measurement	92
6.2	Absolute maximum ratings	92
6.3	Operating conditions	94
6.3.1	General operating conditions	94
6.3.2	VCAP1/VCAP2 external capacitor	96
6.3.3	Operating conditions at power-up / power-down (regulator ON)	97
6.3.4	Operating conditions at power-up / power-down (regulator OFF)	97
6.3.5	Reset and power control block characteristics	98
6.3.6	Over-drive switching characteristics	99
6.3.7	Supply current characteristics	100
6.3.8	Wakeup time from low-power modes	116
6.3.9	External clock source characteristics	117
6.3.10	Internal clock source characteristics	121
6.3.11	PLL characteristics	123
6.3.12	PLL spread spectrum clock generation (SSCG) characteristics	126
6.3.13	Memory characteristics	128
6.3.14	EMC characteristics	130
6.3.15	Absolute maximum ratings (electrical sensitivity)	132
6.3.16	I/O current injection characteristics	133
6.3.17	I/O port characteristics	134
6.3.18	NRST pin characteristics	140
6.3.19	TIM timer characteristics	141
6.3.20	Communications interfaces	141
6.3.21	12-bit ADC characteristics	156
6.3.22	Temperature sensor characteristics	162
6.3.23	V _{BAT} monitoring characteristics	163
6.3.24	Reference voltage	163
6.3.25	DAC electrical characteristics	164
6.3.26	FMC characteristics	167
6.3.27	Camera interface (DCMI) timing specifications	192
6.3.28	LCD-TFT controller (LTDC) characteristics	192
6.3.29	SD/SDIO MMC card host interface (SDIO) characteristics	195

	6.3.30	RTC characteristics	196
7		Package information	197
	7.1	LQFP100 package information	197
	7.2	WLCSP143 package information	201
	7.3	LQFP144 package information	204
	7.4	LQFP176 package information	208
	7.5	LQFP208 package information	212
	7.6	UFBGA169 package information	216
	7.7	UFBGA176+25 package information	219
	7.8	TFBGA216 package information	222
	7.9	Thermal characteristics	224
8		Part numbering	225
		Appendix A Recommendations when using internal reset OFF	226
	A.1	Operating conditions	226
		Appendix B Application block diagrams	227
	B.1	USB OTG full speed (FS) interface solutions	227
	B.2	USB OTG high speed (HS) interface solutions	229
	B.3	Ethernet interface solutions	230
9		Revision history	232

List of tables

Table 1.	Device summary	2
Table 2.	STM32F427xx and STM32F429xx features and peripheral counts	15
Table 3.	Voltage regulator configuration mode versus device operating mode	28
Table 4.	Regulator ON/OFF and internal reset ON/OFF availability	31
Table 5.	Voltage regulator modes in stop mode	32
Table 6.	Timer feature comparison	34
Table 7.	Comparison of I2C analog and digital filters	36
Table 8.	USART feature comparison	37
Table 9.	Legend/abbreviations used in the pinout table	52
Table 10.	STM32F427xx and STM32F429xx pin and ball definitions	52
Table 11.	FMC pin definition	71
Table 12.	STM32F427xx and STM32F429xx alternate function mapping	74
Table 13.	STM32F427xx and STM32F429xx register boundary addresses	86
Table 14.	Voltage characteristics	92
Table 15.	Current characteristics	93
Table 16.	Thermal characteristics	93
Table 17.	General operating conditions	94
Table 18.	Limitations depending on the operating power supply range	96
Table 19.	VCAP1/VCAP2 operating conditions	96
Table 20.	Operating conditions at power-up / power-down (regulator ON)	97
Table 21.	Operating conditions at power-up / power-down (regulator OFF)	97
Table 22.	reset and power control block characteristics	98
Table 23.	Over-drive switching characteristics	99
Table 24.	Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM	101
Table 25.	Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)	102
Table 26.	Typical and maximum current consumption in Sleep mode	103
Table 27.	Typical and maximum current consumptions in Stop mode	104
Table 28.	Typical and maximum current consumptions in Standby mode	105
Table 29.	Typical and maximum current consumptions in V _{BAT} mode	105
Table 30.	Typical current consumption in Run mode, code with data processing running from Flash memory or RAM, regulator ON (ART accelerator enabled except prefetch), VDD=1.7 V	107
Table 31.	Typical current consumption in Run mode, code with data processing running from Flash memory, regulator OFF (ART accelerator enabled except prefetch)	108
Table 32.	Typical current consumption in Sleep mode, regulator ON, VDD=1.7 V	109
Table 33.	Typical current consumption in Sleep mode, regulator OFF	110
Table 34.	Switching output I/O current consumption	112
Table 35.	Peripheral current consumption	113
Table 36.	Low-power mode wakeup timings	116
Table 37.	High-speed external user clock characteristics	117
Table 38.	Low-speed external user clock characteristics	118
Table 39.	HSE 4-26 MHz oscillator characteristics	119
Table 40.	LSE oscillator characteristics (f _{LSE} = 32.768 kHz)	120
Table 41.	HSI oscillator characteristics	121
Table 42.	LSI oscillator characteristics	122
Table 43.	Main PLL characteristics	123

Table 44.	PLLI2S (audio PLL) characteristics	124
Table 45.	PLLISAI (audio and LCD-TFT PLL) characteristics	125
Table 46.	SSCG parameters constraint	126
Table 47.	Flash memory characteristics	128
Table 48.	Flash memory programming	128
Table 49.	Flash memory programming with V_{PP}	129
Table 50.	Flash memory endurance and data retention	130
Table 51.	EMS characteristics	130
Table 52.	EMI characteristics	131
Table 53.	ESD absolute maximum ratings	132
Table 54.	Electrical sensitivities	132
Table 55.	I/O current injection susceptibility	133
Table 56.	I/O static characteristics	134
Table 57.	Output voltage characteristics	137
Table 58.	I/O AC characteristics	138
Table 59.	NRST pin characteristics	140
Table 60.	TIMx characteristics	141
Table 61.	I2C analog filter characteristics	142
Table 62.	SPI dynamic characteristics	142
Table 63.	I ² S dynamic characteristics	145
Table 64.	SAI characteristics	147
Table 65.	USB OTG full speed startup time	149
Table 66.	USB OTG full speed DC electrical characteristics	149
Table 67.	USB OTG full speed electrical characteristics	150
Table 68.	USB HS DC electrical characteristics	150
Table 69.	USB HS clock timing parameters	151
Table 70.	Dynamic characteristics: USB ULPI	152
Table 71.	Dynamics characteristics: Ethernet MAC signals for SMI	153
Table 72.	Dynamics characteristics: Ethernet MAC signals for RMII	154
Table 73.	Dynamics characteristics: Ethernet MAC signals for MII	155
Table 74.	ADC characteristics	156
Table 75.	ADC static accuracy at $f_{ADC} = 18$ MHz	157
Table 76.	ADC static accuracy at $f_{ADC} = 30$ MHz	158
Table 77.	ADC static accuracy at $f_{ADC} = 36$ MHz	158
Table 78.	ADC dynamic accuracy at $f_{ADC} = 18$ MHz - limited test conditions	158
Table 79.	ADC dynamic accuracy at $f_{ADC} = 36$ MHz - limited test conditions	158
Table 80.	Temperature sensor characteristics	162
Table 81.	Temperature sensor calibration values	162
Table 82.	V_{BAT} monitoring characteristics	163
Table 83.	internal reference voltage	163
Table 84.	Internal reference voltage calibration values	163
Table 85.	DAC characteristics	164
Table 86.	Asynchronous non-multiplexed SRAM/PSRAM/NOR - read timings	168
Table 87.	Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings	169
Table 88.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings	170
Table 89.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings	171
Table 90.	Asynchronous multiplexed PSRAM/NOR read timings	172
Table 91.	Asynchronous multiplexed PSRAM/NOR read-NWAIT timings	172
Table 92.	Asynchronous multiplexed PSRAM/NOR write timings	173

Table 93.	Asynchronous multiplexed PSRAM/NOR write-NWAIT timings	174
Table 94.	Synchronous multiplexed NOR/PSRAM read timings	175
Table 95.	Synchronous multiplexed PSRAM write timings	177
Table 96.	Synchronous non-multiplexed NOR/PSRAM read timings	178
Table 97.	Synchronous non-multiplexed PSRAM write timings	179
Table 98.	Switching characteristics for PC Card/CF read and write cycles in attribute/common space	184
Table 99.	Switching characteristics for PC Card/CF read and write cycles in I/O space	185
Table 100.	Switching characteristics for NAND Flash read cycles	187
Table 101.	Switching characteristics for NAND Flash write cycles	188
Table 102.	SDRAM read timings	189
Table 103.	LPSDR SDRAM read timings	189
Table 104.	SDRAM write timings	191
Table 105.	LPSDR SDRAM write timings	191
Table 106.	DCMI characteristics	192
Table 107.	LTDC characteristics	193
Table 108.	Dynamic characteristics: SD / MMC characteristics	196
Table 109.	RTC characteristics	196
Table 110.	LQFP100 100-pin, 14 x 14 mm low-profile quad flat package mechanical data	198
Table 111.	WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package mechanical data	202
Table 112.	WLCSP143 recommended PCB design rules (0.4 mm pitch)	203
Table 113.	LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data	205
Table 114.	LQFP176 - 176-pin, 24 x 24 mm low-profile quad flat package mechanical data	208
Table 115.	LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package mechanical data	213
Table 116.	UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data	216
Table 117.	UFBGA169 recommended PCB design rules (0.5 mm pitch BGA)	217
Table 118.	UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data	219
Table 119.	UFBGA176+25 recommended PCB design rules (0.65 mm pitch BGA)	220
Table 120.	TFBGA216 - 216 ball 13 x 13 mm 0.8 mm pitch thin fine pitch ball grid array package mechanical data	222
Table 121.	Package thermal characteristics	224
Table 122.	Ordering information scheme	225
Table 123.	Limitations depending on the operating power supply range	226
Table 124.	Document revision history	232

List of figures

Figure 1.	Compatible board design STM32F10xx/STM32F2xx/STM32F4xx for LQFP100 package.	17
Figure 2.	Compatible board design between STM32F10xx/STM32F2xx/STM32F4xx for LQFP144 package.	18
Figure 3.	Compatible board design between STM32F2xx and STM32F4xx for LQFP176 and UFBGA176 packages	18
Figure 4.	STM32F427xx and STM32F429xx block diagram	19
Figure 5.	STM32F427xx and STM32F429xx Multi-AHB matrix	22
Figure 6.	Power supply supervisor interconnection with internal reset OFF	26
Figure 7.	PDR_ON control with internal reset OFF	27
Figure 8.	Regulator OFF	29
Figure 9.	Startup in regulator OFF: slow V_{DD} slope - power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization	30
Figure 10.	Startup in regulator OFF mode: fast V_{DD} slope - power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization	30
Figure 11.	STM32F42x LQFP100 pinout	44
Figure 12.	STM32F42x WLCSP143 ballout	45
Figure 13.	STM32F42x LQFP144 pinout	46
Figure 14.	STM32F42x LQFP176 pinout	47
Figure 15.	STM32F42x LQFP208 pinout	48
Figure 16.	STM32F42x UFBGA169 ballout	49
Figure 17.	STM32F42x UFBGA176 ballout	50
Figure 18.	STM32F42x TFBGA216 ballout	51
Figure 19.	Memory map	85
Figure 20.	Pin loading conditions	90
Figure 21.	Pin input voltage	90
Figure 22.	Power supply scheme	91
Figure 23.	Current consumption measurement scheme	92
Figure 24.	External capacitor C_{EXT}	96
Figure 25.	Typical V_{BAT} current consumption (LSE and RTC ON/backup RAM OFF)	106
Figure 26.	Typical V_{BAT} current consumption (LSE and RTC ON/backup RAM ON)	106
Figure 27.	High-speed external clock source AC timing diagram	118
Figure 28.	Low-speed external clock source AC timing diagram	119
Figure 29.	Typical application with an 8 MHz crystal	120
Figure 30.	Typical application with a 32.768 kHz crystal	121
Figure 31.	ACC_HSI accuracy versus temperature	122
Figure 32.	ACC_LSI versus temperature	123
Figure 33.	PLL output clock waveforms in center spread mode	127
Figure 34.	PLL output clock waveforms in down spread mode	127
Figure 35.	FT I/O input characteristics	136
Figure 36.	I/O AC characteristics definition	139
Figure 37.	Recommended NRST pin protection	140
Figure 38.	SPI timing diagram - slave mode and CPHA = 0	143
Figure 39.	SPI timing diagram - slave mode and CPHA = 1	144
Figure 40.	SPI timing diagram - master mode	144
Figure 41.	I ² S slave timing diagram (Philips protocol) ⁽¹⁾	146
Figure 42.	I ² S master timing diagram (Philips protocol) ⁽¹⁾	146
Figure 43.	SAI master timing waveforms	148

Figure 44.	SAI slave timing waveforms	148
Figure 45.	USB OTG full speed timings: definition of data signal rise and fall time	150
Figure 46.	ULPI timing diagram	151
Figure 47.	Ethernet SMI timing diagram	153
Figure 48.	Ethernet RMII timing diagram	154
Figure 49.	Ethernet MII timing diagram	155
Figure 50.	ADC accuracy characteristics	159
Figure 51.	Typical connection diagram using the ADC	160
Figure 52.	Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})	161
Figure 53.	Power supply and reference decoupling (V_{REF+} connected to V_{DDA})	162
Figure 54.	12-bit buffered /non-buffered DAC	166
Figure 55.	Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms	168
Figure 56.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms	170
Figure 57.	Asynchronous multiplexed PSRAM/NOR read waveforms	171
Figure 58.	Asynchronous multiplexed PSRAM/NOR write waveforms	173
Figure 59.	Synchronous multiplexed NOR/PSRAM read timings	175
Figure 60.	Synchronous multiplexed PSRAM write timings	176
Figure 61.	Synchronous non-multiplexed NOR/PSRAM read timings	178
Figure 62.	Synchronous non-multiplexed PSRAM write timings	179
Figure 63.	PC Card/CompactFlash controller waveforms for common memory read access	181
Figure 64.	PC Card/CompactFlash controller waveforms for common memory write access	181
Figure 65.	PC Card/CompactFlash controller waveforms for attribute memory read access	182
Figure 66.	PC Card/CompactFlash controller waveforms for attribute memory write access	183
Figure 67.	PC Card/CompactFlash controller waveforms for I/O space read access	183
Figure 68.	PC Card/CompactFlash controller waveforms for I/O space write access	184
Figure 69.	NAND controller waveforms for read access	186
Figure 70.	NAND controller waveforms for write access	186
Figure 71.	NAND controller waveforms for common memory read access	187
Figure 72.	NAND controller waveforms for common memory write access	187
Figure 73.	SDRAM read access waveforms (CL = 1)	188
Figure 74.	SDRAM write access waveforms	190
Figure 75.	DCMI timing diagram	192
Figure 76.	LCD-TFT horizontal timing diagram	194
Figure 77.	LCD-TFT vertical timing diagram	194
Figure 78.	SDIO high-speed mode	195
Figure 79.	SD default mode	195
Figure 80.	LQFP100 -100-pin, 14 x 14 mm low-profile quad flat package outline	197
Figure 81.	LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint	199
Figure 82.	LQFP100 marking example (package top view)	200
Figure 83.	WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package outline	201
Figure 84.	WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale recommended footprint	202
Figure 85.	WLCSP143 marking example (package top view)	203
Figure 86.	LQFP144-144-pin, 20 x 20 mm low-profile quad flat package outline	204
Figure 87.	LQPF144- 144-pin, 20 x 20 mm low-profile quad flat package recommended footprint	206
Figure 88.	LQFP144 marking example (package top view)	207
Figure 89.	LQFP176 - 176-pin, 24 x 24 mm low-profile quad flat package outline	208

Figure 90.	LQFP176 - 176-pin, 24 x 24 mm low profile quad flat recommended footprint.	210
Figure 91.	LQFP176 marking (package top view)	211
Figure 92.	LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package outline	212
Figure 93.	LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package recommended footprint.	214
Figure 94.	LQFP208 marking example (package top view)	215
Figure 95.	UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package outline.	216
Figure 96.	UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array recommended footprint	217
Figure 97.	UFBGA169 marking example (package top view)	218
Figure 98.	UFBGA176+25 - ball 10 x 10 mm, 0.65 mm pitch ultra thin fine pitch ball grid array package outline	219
Figure 99.	UFBGA176+25-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package recommended footprint	220
Figure 100.	UFBGA176+25 marking example (package top view)	221
Figure 101.	TFBGA216 - 216 ball 13 x 13 mm 0.8 mm pitch thin fine pitch ball grid array package outline	222
Figure 102.	TFBGA176 marking example (package top view)	223
Figure 103.	USB controller configured as peripheral-only and used in Full speed mode	227
Figure 104.	USB controller configured as host-only and used in full speed mode.	227
Figure 105.	USB controller configured in dual mode and used in full speed mode	228
Figure 106.	USB controller configured as peripheral, host, or dual-mode and used in high speed mode.	229
Figure 107.	MII mode using a 25 MHz crystal	230
Figure 108.	RMII with a 50 MHz oscillator	230
Figure 109.	RMII with a 25 MHz crystal and PHY with PLL.	231

1 Introduction

This datasheet provides the description of the STM32F427xx and STM32F429xx line of microcontrollers. For more details on the whole STMicroelectronics STM32 family, please refer to [Section 2.1: Full compatibility throughout the family](#).

The STM32F427xx and STM32F429xx datasheet should be read in conjunction with the STM32F4xx reference manual.

For information on the Cortex[®]-M4 core, please refer to the Cortex[®]-M4 programming manual (PM0214), available from www.st.com.

2 Description

The STM32F427xx and STM32F429xx devices are based on the high-performance ARM[®] Cortex[®]-M4 32-bit RISC core operating at a frequency of up to 180 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all ARM[®] single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F427xx and STM32F429xx devices incorporate high-speed embedded memories (Flash memory up to 2 Mbyte, up to 256 kbytes of SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers. They also feature standard and advanced communication interfaces.

- Up to three I²Cs
- Six SPIs, two I²Ss full duplex. To achieve audio class accuracy, the I²S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus four UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI),
- Two CANs
- One SAI serial audio interface
- An SDIO/MMC interface
- Ethernet and camera interface
- LCD-TFT display controller
- Chrom-ART Accelerator™.

Advanced peripherals include an SDIO, a flexible memory control (FMC) interface, a camera interface for CMOS sensors. Refer to [Table 2: STM32F427xx and STM32F429xx features and peripheral counts](#) for the list of peripherals available on each part number.

The STM32F427xx and STM32F429xx devices operates in the –40 to +105 °C temperature range from a 1.7 to 3.6 V power supply.

The supply voltage can drop to 1.7 V with the use of an external power supply supervisor (refer to [Section 3.17.2: Internal reset OFF](#)). A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F427xx and STM32F429xx devices offer devices in 8 packages ranging from 100 pins to 216 pins. The set of included peripherals changes with the device chosen.



These features make the STM32F427xx and STM32F429xx microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances

Figure 4 shows the general block diagram of the device family.

Table 2. STM32F427xx and STM32F429xx features and peripheral counts

Peripherals	STM32F427 Vx		STM32F429Vx			STM32F427 Zx		STM32F429Zx			STM32F427 Ax		STM32F429 Ax		STM32F427 lx		STM32F429lx			STM32F429Bx			STM32F429Nx			
	1024	2048	512	1024	2048	1024	2048	512	1024	2048	1024	2048	1024	2048	1024	2048	512	1024	2048	512	1024	2048	512	1024	2048	
Flash memory in Kbytes	1024	2048	512	1024	2048	1024	2048	512	1024	2048	1024	2048	1024	2048	1024	2048	512	1024	2048	512	1024	2048	512	1024	2048	
SRAM in Kbytes	System	256(112+16+64+64)																								
	Backup	4																								
FMC memory controller	Yes ⁽¹⁾																									
Ethernet	Yes																									
Timers	General-purpose	10																								
	Advanced-control	2																								
	Basic	2																								
Random number generator	Yes																									



Table 2. STM32F427xx and STM32F429xx features and peripheral counts (continued)

Peripherals		STM32F427 Vx	STM32F429Vx	STM32F427 Zx	STM32F429Zx	STM32F427 Ax	STM32F429 Ax	STM32F427 lx	STM32F429lx	STM32F429Bx	STM32F429Nx
Communication interfaces	SPI / I ² S	4/2 (full duplex) ⁽²⁾			6/2 (full duplex) ⁽²⁾						
	I ² C	3									
	USART/ UART	4/4									
	USB OTG FS	Yes									
	USB OTG HS	Yes									
	CAN	2									
	SAI	1									
	SDIO	Yes									
Camera interface		Yes									
LCD-TFT (STM32F429xx only)		No	Yes	No	Yes	No	Yes	No	Yes		
Chrom-ART Accelerator™		Yes									
GPIOs		82		114		130		140		168	
12-bit ADC Number of channels		3									
		16		24							
12-bit DAC Number of channels		Yes 2									
Maximum CPU frequency		180 MHz									
Operating voltage		1.8 to 3.6 V ⁽³⁾									
Operating temperatures		Ambient temperatures: -40 to +85 °C / -40 to +105 °C									
		Junction temperature: -40 to + 125 °C									
Packages		LQFP100		WLCSP143 LQFP144		UFPGA169		UFPGA176 LQFP176		LQFP208	TFBGA216

1. For the LQFP100 package, only FMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package. For UFPGA169 package, only SDRAM, NAND and multiplexed static memories are supported.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to [Section 3.17.2: Internal reset OFF](#)).

2.1 Full compatibility throughout the family

The STM32F427xx and STM32F429xx devices are part of the STM32F4 family. They are fully pin-to-pin, software and feature compatible with the STM32F2xx devices, allowing the user to try different memory densities, peripherals, and performances (FPU, higher frequency) for a greater degree of freedom during the development cycle.

The STM32F427xx and STM32F429xx devices maintain a close compatibility with the whole STM32F10xx family. All functional pins are pin-to-pin compatible. The STM32F427xx and STM32F429xx, however, are not drop-in replacements for the STM32F10xx devices: the two families do not have the same power scheme, and so their power pins are different. Nonetheless, transition from the STM32F10xx to the STM32F42x family remains simple as only a few pins are impacted.

Figure 1, Figure 2, and Figure 3, give compatible board designs between the STM32F4xx, STM32F2xx, and STM32F10xx families.

Figure 1. Compatible board design STM32F10xx/STM32F2xx/STM32F4xx for LQFP100 package

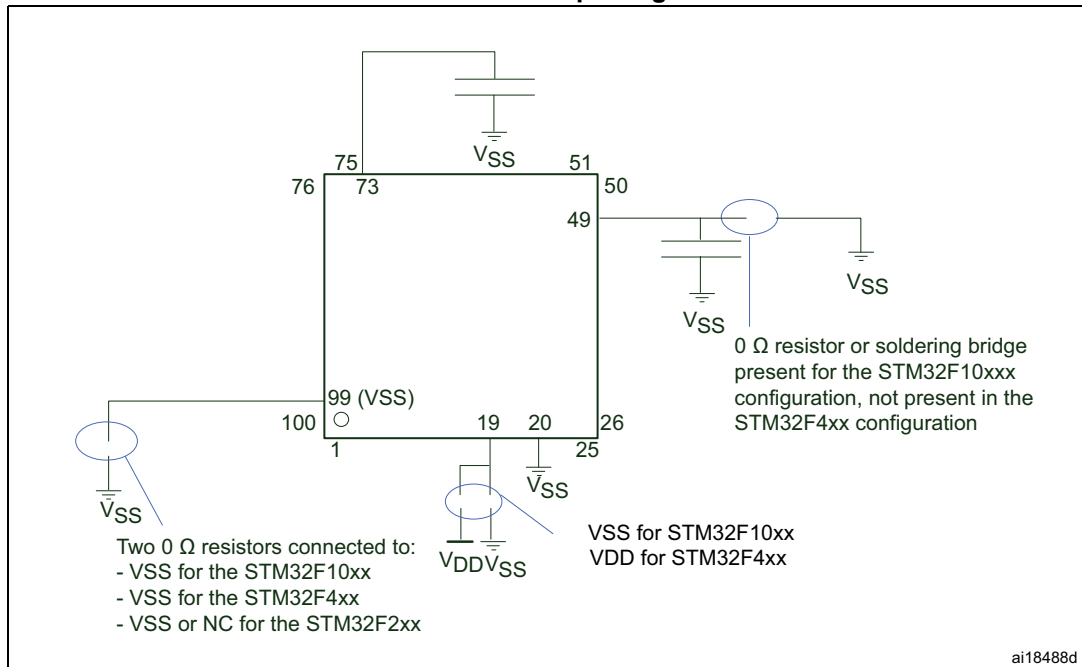


Figure 2. Compatible board design between STM32F10xx/STM32F2xx/STM32F4xx for LQFP144 package

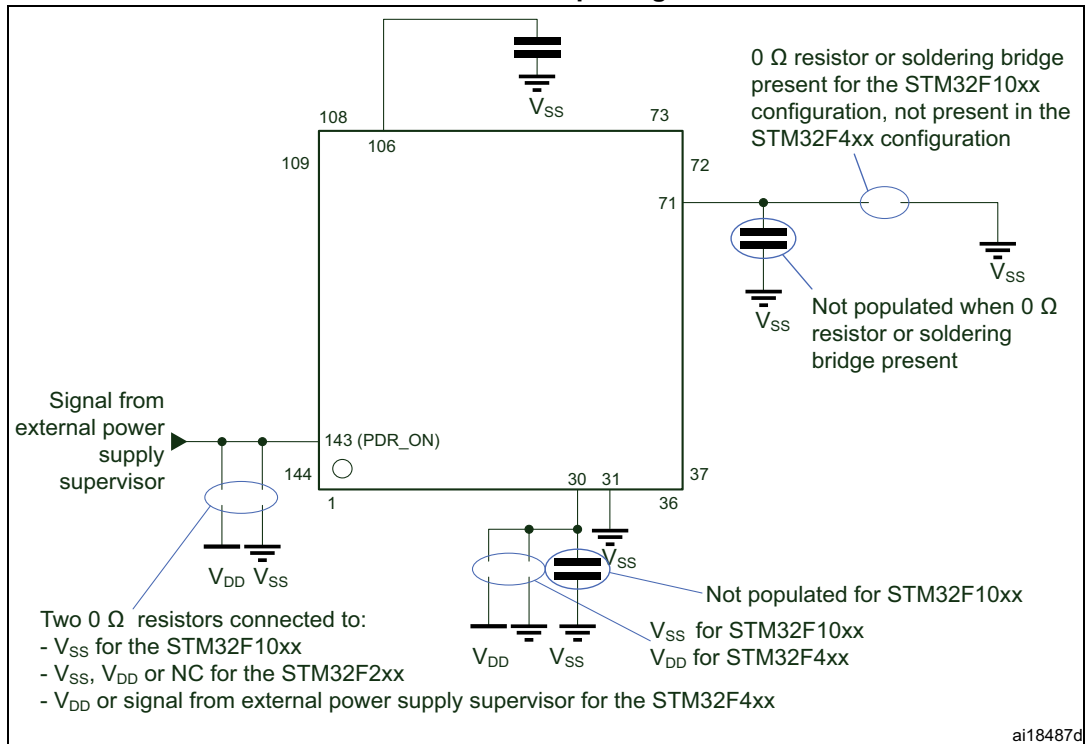


Figure 3. Compatible board design between STM32F2xx and STM32F4xx for LQFP176 and UFBGA176 packages

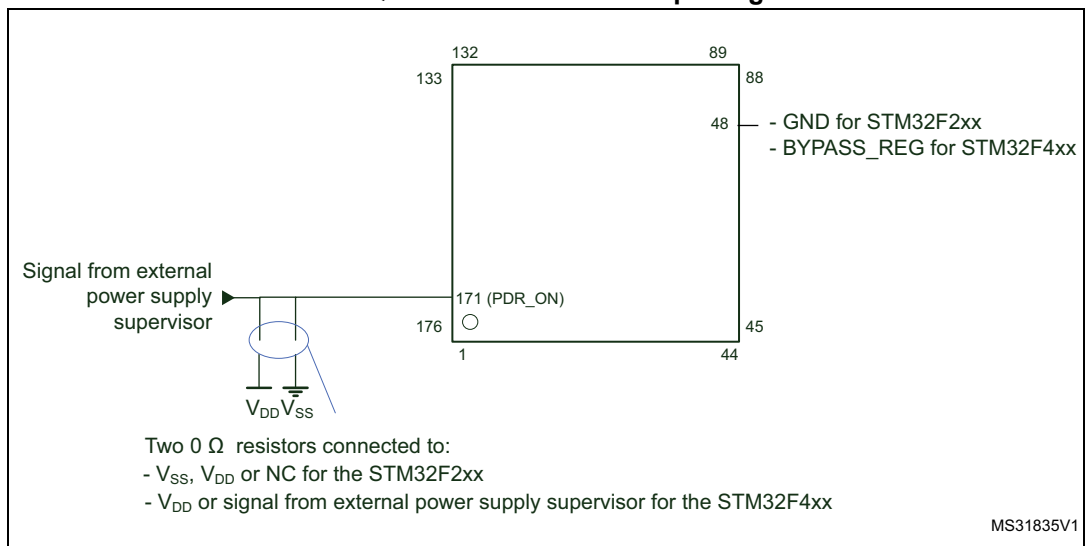
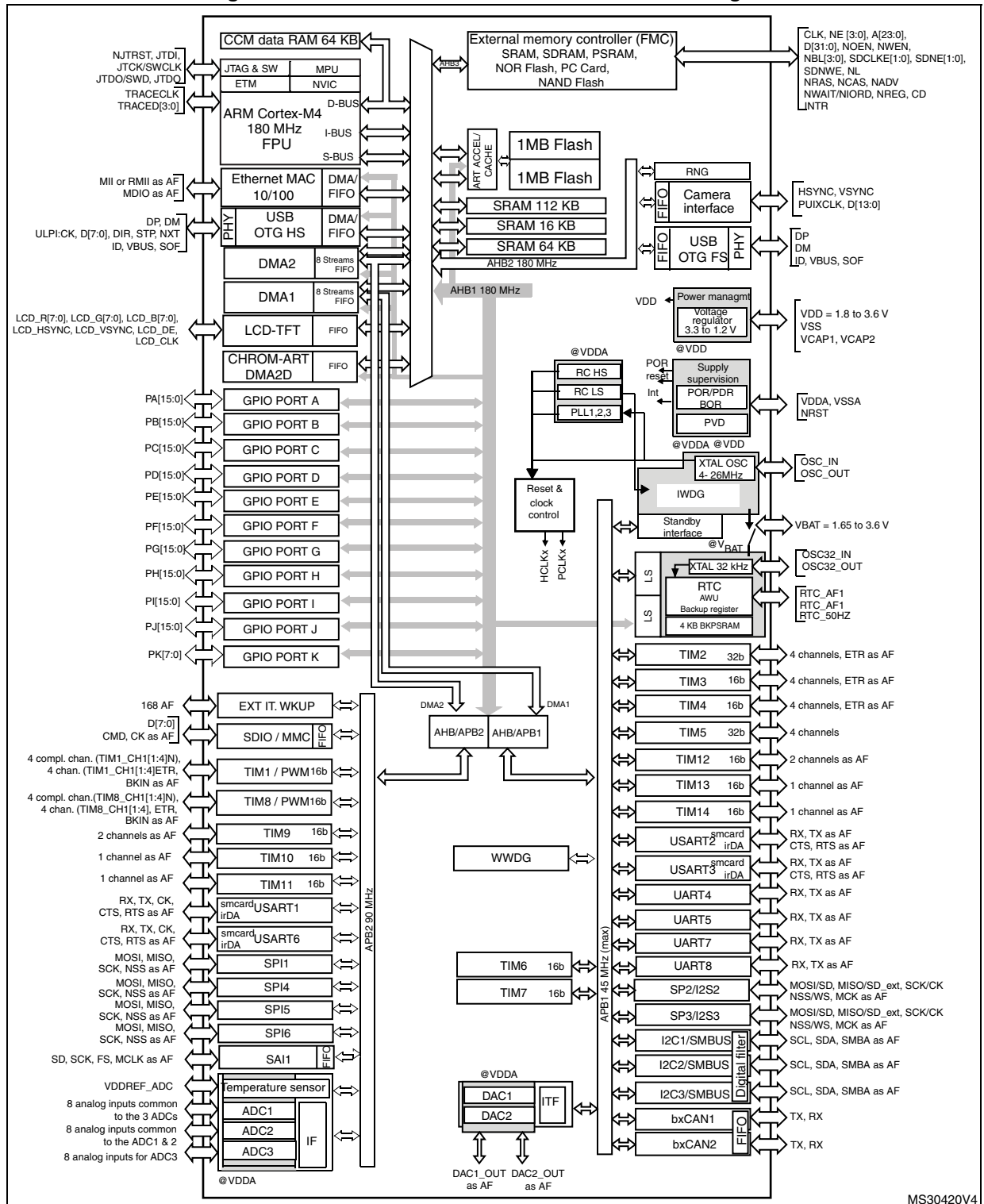


Figure 4. STM32F427xx and STM32F429xx block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 180 MHz, while the timers connected to APB1 are clocked from TIMxCLK either up to 90 MHz or 180 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.
2. The LCD-TFT is available only on STM32F429xx devices.



3 Functional overview

3.1 ARM[®] Cortex[®]-M4 with FPU and embedded Flash and SRAM

The ARM[®] Cortex[®]-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM[®] Cortex[®]-M4 with FPU core is a 32-bit RISC processor that features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F42x family is compatible with all ARM tools and software.

Figure 4 shows the general block diagram of the STM32F42x family.

Note: Cortex-M4 with FPU core is binary compatible with the Cortex-M3 core.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM[®] Cortex[®]-M4 with FPU processors. It balances the inherent performance advantage of the ARM[®] Cortex[®]-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 225 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 180 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded Flash memory

The devices embed a Flash memory of up to 2 Mbytes available for storing programs and data.

3.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.6 Embedded SRAM

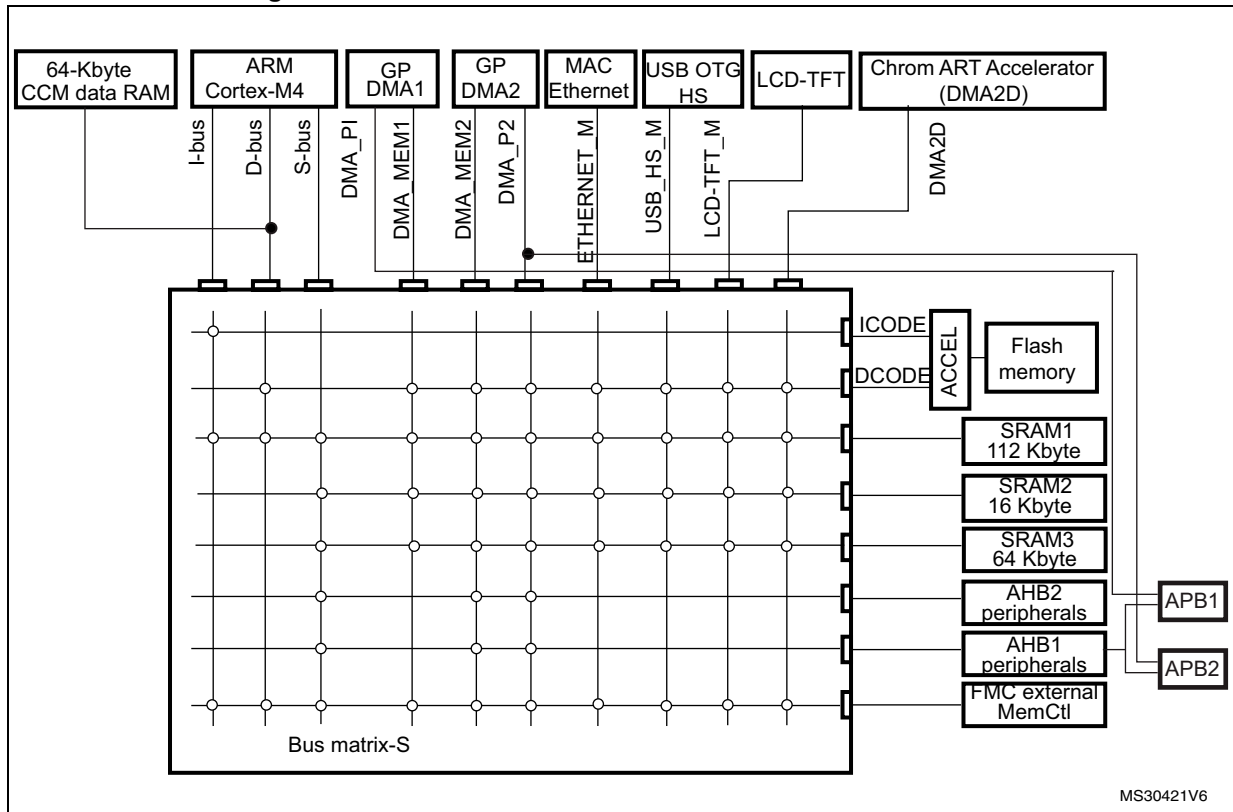
All devices embed:

- Up to 256Kbytes of system SRAM including 64 Kbytes of CCM (core coupled memory) data RAM
RAM memory is accessed (read/write) at CPU clock speed with 0 wait states.
- 4 Kbytes of backup SRAM
This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or VBAT mode.

3.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS, LCD-TFT, and DMA2D) and the slaves (Flash memory, RAM, FMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 5. STM32F427xx and STM32F429xx Multi-AHB matrix



3.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I²S
- I²C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDIO
- Camera interface (DCMI)
- ADC
- SAI1.

3.9 Flexible memory controller (FMC)

All devices embed an FMC. It has four Chip Select outputs supporting the following modes: PCCard/Compact Flash, SDRAM/LPSDR SDRAM, SRAM, PSRAM, NOR Flash and NAND Flash.

Functionality overview:

- 8-, 16-, 32-bit data bus width
- Read FIFO for SDRAM controller
- Write FIFO
- Maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is 90 MHz.

LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

3.10 LCD-TFT controller (available only on STM32F429xx)

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 displays layers with dedicated FIFO (64x32-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 Input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events.

3.11 Chrom-ART Accelerator™ (DMA2D)

The Chrom-Art Accelerator™ (DMA2D) is a graphic accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion.

Various image format coding are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

3.12 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 91 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.13 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 168 GPIOs can be connected to the 16 external interrupt lines.

3.14 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy over the full temperature range. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is

detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 180 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the two AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the two AHB buses is 180 MHz while the maximum frequency of the high-speed APB domains is 90 MHz. The maximum allowed frequency of the low-speed APB domain is 45 MHz.

The devices embed a dedicated PLL (PLL12S) and PLLSAI which allows to achieve audio class performance. In this case, the I²S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

3.15 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory through a serial interface. Refer to application note AN2606 for details.

3.16 Power supply schemes

- $V_{DD} = 1.7$ to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins.
- $V_{SSA}, V_{DDA} = 1.7$ to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.
- $V_{BAT} = 1.65$ to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Note: V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to [Section 3.17.2: Internal reset OFF](#)). Refer to [Table 3: Voltage regulator configuration mode versus device operating mode](#) to identify the packages supporting this option.

3.17 Power supply supervisor

3.17.1 Internal reset ON

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On the other package, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is