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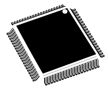
STM32F446xC/E

ARM® Cortex®-M4 32b MCU+FPU, 225DMIPS, up to 512kB Flash/128+4KB RAM, USB OTG HS/FS, 17 TIMs, 3 ADCs, 20 comm. interfaces

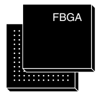
Datasheet - production data

Features

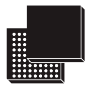
- Core: ARM® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution from Fl ash memory, frequency up to 180 MHz, MPU, 225 DMIPS/1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Memories
  - 512 kB of Flash memory
  - 128 KB of SRAM
  - Flexible external memory controller with up to 16-bit data bus: SRAM,PSRAM,SDRAM/LPSDR SDRAM, Flash NOR/NAND memories
  - Dual mode Quad SPI interface
- LCD parallel interface, 8080/6800 modes
- Clock, reset and supply management
  - 1.7 V to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC (1% accuracy)
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Low power
  - Sleep, Stop and Standby modes
  - V_{BAT} supply for RTC, 20×32 bit backup registers + optional 4 KB backup SRAM
- 3×12-bit, 2.4 MSPS ADC: up to 24 channels and 7.2 MSPS in triple interleaved mode
- 2×12-bit D/A converters
- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Up to 17 timers: 2x watchdog, 1x SysTick timer and up to twelve 16-bit and two 32-bit timers up to 180 MHz, each with up to 4 IC/OC/PWM or pulse counter
- Debug mode
  - SWD & JTAG interfaces
  - Cortex®-M4 Trace Macrocell™



LQFP64 (10 × 10mm)
LQFP100 (14 × 14mm)
LQFP144 (20 x 20 mm)



UFBGA144 (7 x 7 mm)
UFBGA144 (10 x 10 mm)



WLCSP 81

- Up to 114 I/O ports with interrupt capability
  - Up to 111 fast I/Os up to 90 MHz
  - Up to 112 5 V-tolerant I/Os
- Up to 20 communication interfaces
  - SPDIF-Rx
  - Up to 4 × I^2C interfaces (SMBus/PMBus)
  - Up to 4 USARTs/2 UARTs (11.25 Mbit/s, ISO7816 interface, LIN, IrDA, modem control)
  - Up to 4 SPIs (45 Mbits/s), 3 with muxed I^2S for audio class accuracy via internal audio PLL or external clock
  - 2 x SAI (serial audio interface)
  - 2 × CAN (2.0B Active)
  - SDIO interface
  - Consumer electronics control (CEC) I/F
- Advanced connectivity
  - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
  - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
  - Dedicated USB power rail enabling on-chip PHYs operation throughout the entire MCU power supply range
- 8- to 14-bit parallel camera interface up to 54 Mbytes/s
- CRC calculation unit
- RTC: subsecond accuracy, hardware calendar
- 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM32F446xC/E	STM32F446MC, STM32F446ME, STM32F446RC, STM32F446RE, STM32F446VC, STM32F446VE, STM32F446ZC, STM32F446ZE.

Contents

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List of tables

1 Introduction

This document provides the description of the STM32F446xC/E products.

The STM32F446xC/E document should be read in conjunction with the STM32F4xx reference manual.

For information on the Cortex®-M4 core, please refer to the Cortex®-M4 programming manual (PM0214), available from the *www.st.com*.

2 Description

The STM32F446xC/E devices are based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 180 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all ARM® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F446xC/E devices incorporate high-speed embedded memories (Flash memory up to 512 Kbyte, up to 128 Kbyte of SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers.

They also feature standard and advanced communication interfaces.

- Up to four I^2Cs;
- Four SPIs, three I^2Ss full simplex. To achieve audio class accuracy, the I^2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization;
- Four USARTs plus two UARTs;
- An USB OTG full-speed and an USB OTG high-speed with full-speed capability (with the ULPI), both with dedicated power rails allowing to use them throughout the entire power range;
- Two CANs;
- Two SAIs serial audio interfaces. To achieve audio class accuracy, the SAIs can be clocked via a dedicated internal audio PLL;
- An SDIO/MMC interface;
- Camera interface;
- HDMI-CEC;
- SPDIF Receiver (SPDIFRx);
- QuadSPI.

Advanced peripherals include an SDIO, a flexible memory control (FMC) interface, a camera interface for CMOS sensors. Refer to *Table 2: STM32F446xC/E features and peripheral counts* for the list of peripherals available on each part number.

The STM32F446xC/E devices operates in the –40 to +105 °C temperature range from a 1.7 to 3.6 V power supply.

The supply voltage can drop to 1.7 V with the use of an external power supply supervisor (refer to *Section 3.16.2: Internal reset OFF*). A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F446xC/E devices offer devices in 6 packages ranging from 64 pins to 144 pins. The set of included peripherals changes with the device chosen.

These features make the STM32F446xC/E microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances

Table 2. STM32F446xC/E features and peripheral counts

Peripherals		STM32F446MC	STM32F446ME	STM32F446RC	STM32F446RE	STM32F446VC	STM32F446VE	STM32F446ZC	STM32F446ZE
Flash memory in Kbytes		256	512	256	512	256	512	256	512
SRAM in Kbytes	System	128 (112+16)							
	Backup	4							
FMC memory controller		No				Yes(1)			
Timers	General-purpose	10							
	Advanced-control	2							
	Basic	2							
Communication interfaces	SPI / I^2S	4/3 (simplex)(2)							
	I^2C	4/1 FMP +							
	USART/UART	4/2							
	USB OTG FS	Yes (6-Endpoints)							
	USB OTG HS	Yes (8-Endpoints)							
	CAN	2							
	SAI	2							
	SDIO	Yes							
	SPDIF-Rx	1							
	HDMI-CEC	1							
	Quad SPI(3)	1							
Camera interface		Yes							
GPIOs		63		50		81		114	
12-bit ADC Number of channels		3							
		14		16		16		24	
12-bit DAC Number of channels		Yes 2							
Maximum CPU frequency		180 MHz							
Operating voltage		1.8 to 3.6 V(4)							
Operating temperatures		Ambient temperatures: –40 to +85 °C /–40 to +105 °C							
		Junction temperature: –40 to + 125 °C							
Packages		WLCSP81		LQFP64		LQFP100		LQFP144 UFBGA144	

1. For the LQFP100 package, only FMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. The SPI1, SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. For the LQFP64 package, the Quad SPI is available with limited features.
4. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to *Section 3.16.2: Internal reset OFF)*.

2.1 Compatibility with STM32F4 family

The STM32F446xC/xV is software and feature compatible with the STM32F4 family.

The STM32F446xC/xV can be used as drop-in replacement of the other STM32F4 products but some slight changes have to be done on the PCB board.

Figure 1. Compatible board design for LQFP100 package

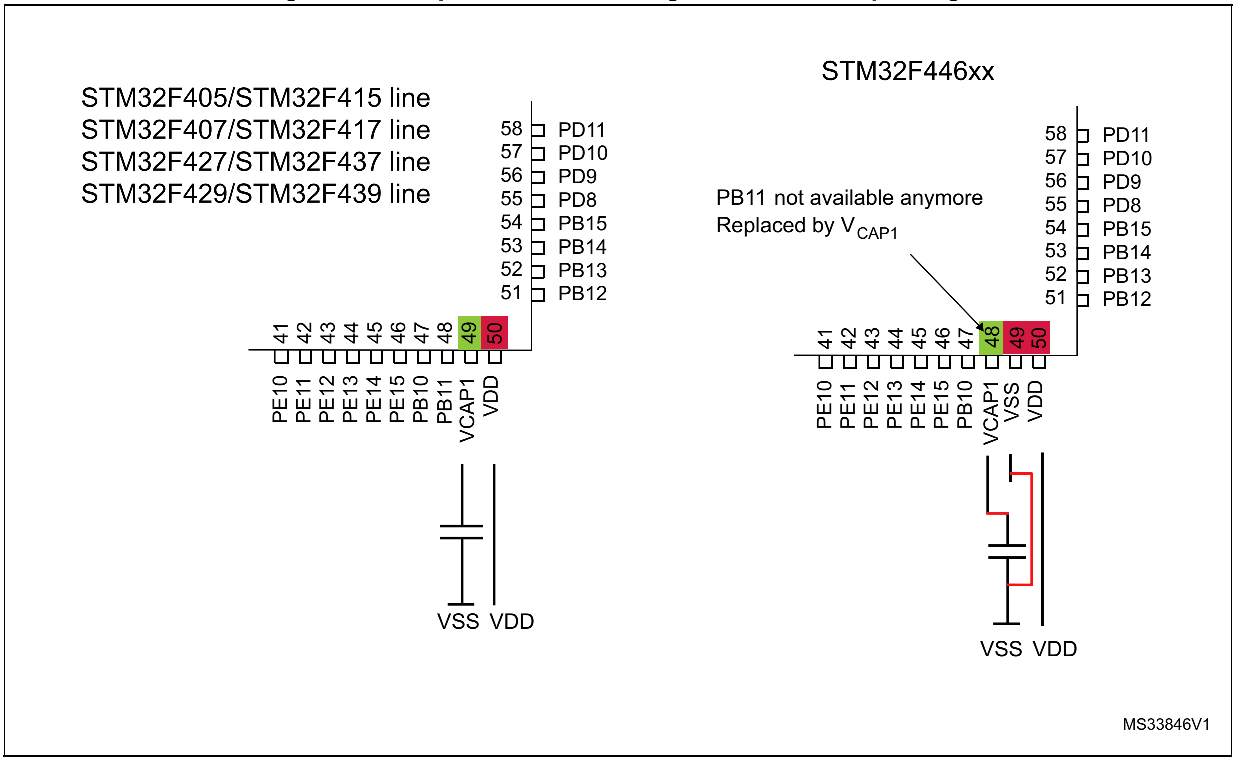


Figure 2. Compatible board for LQFP64 package

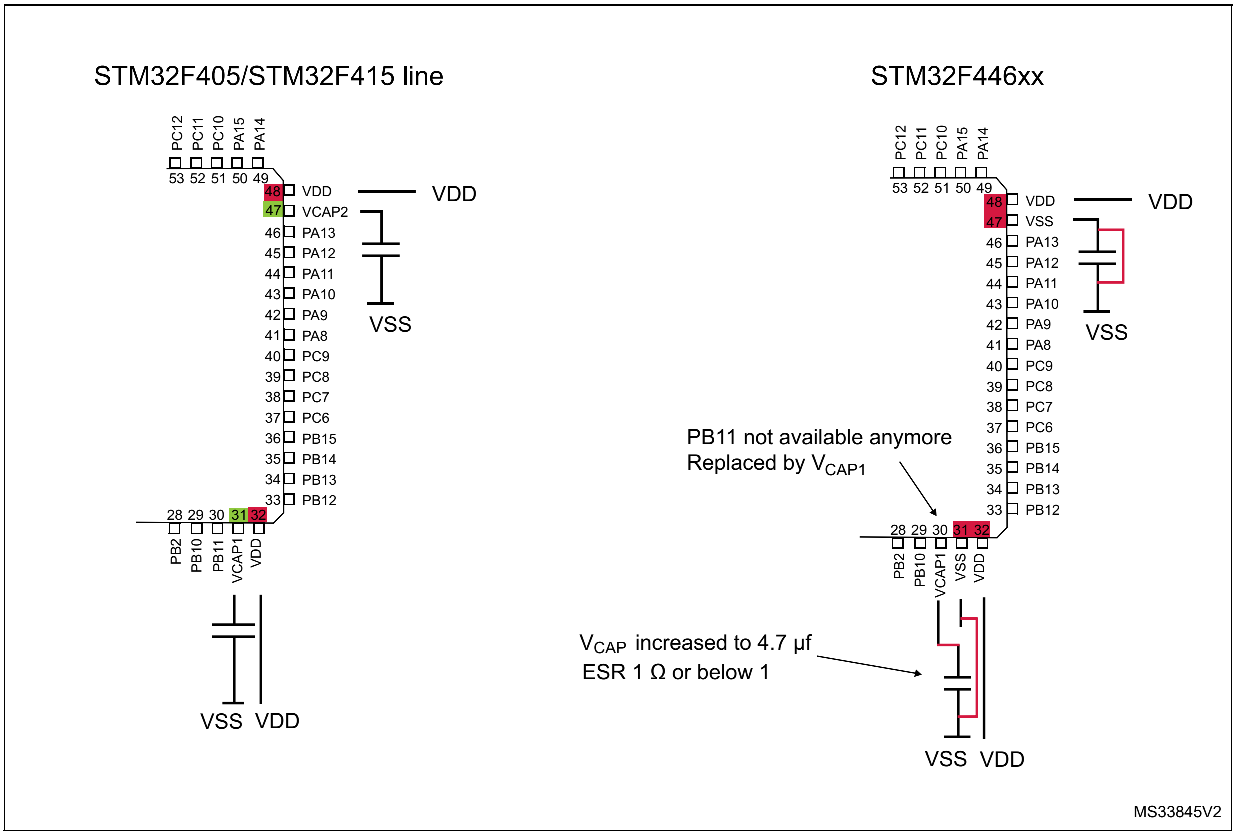
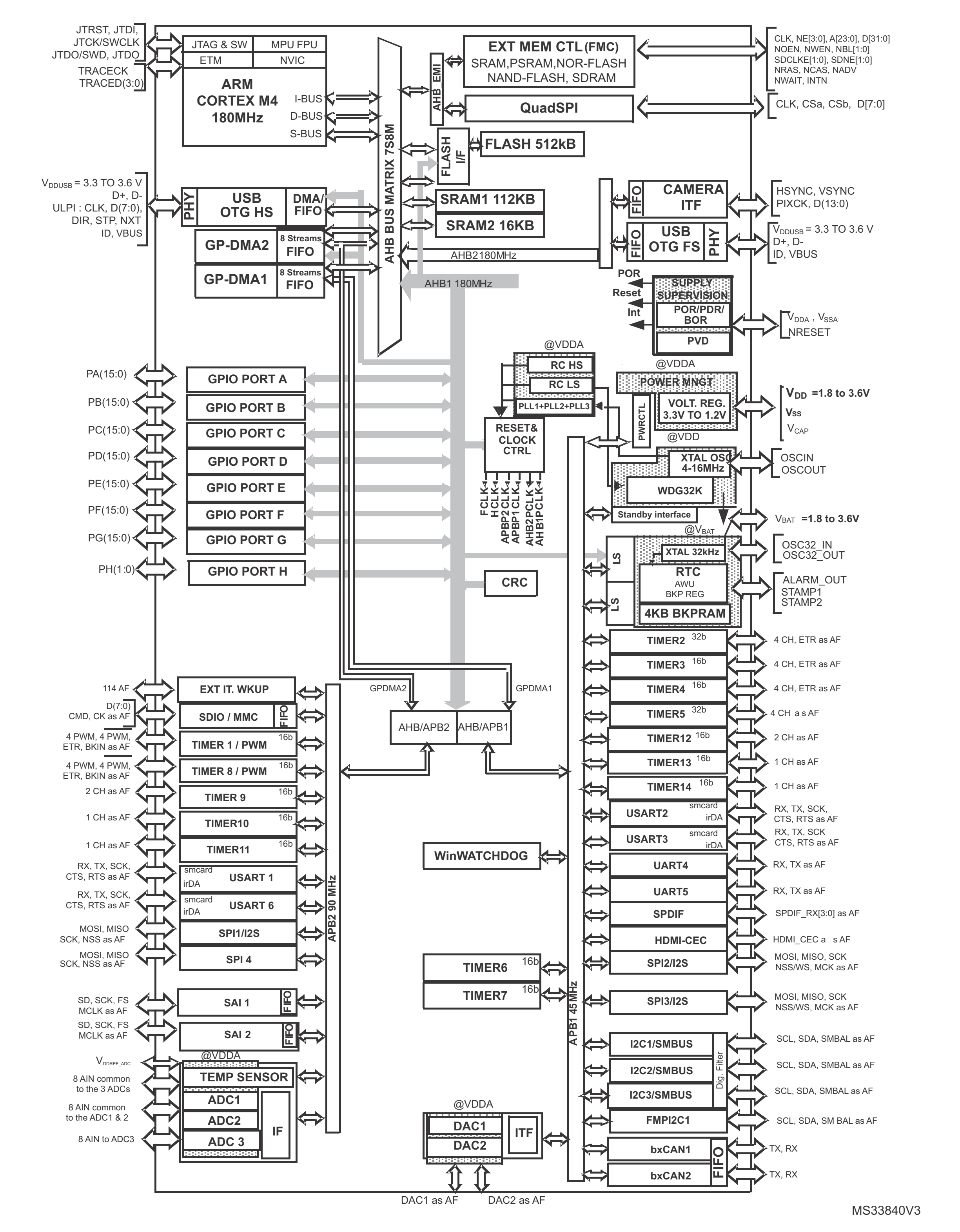


Figure 3 shows the STM32F446xx block diagram.

Figure 3. STM32F446xC/E block diagram



3 Functional overview

3.1 ARM® Cortex®-M4 with FPU and embedded Flash and SRAM

The ARM® Cortex®-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 with FPU core is a 32-bit RISC processor that features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F446xC/E family is compatible with all ARM tools and software.

Figure 3 shows the general block diagram of the STM32F446xC/E family.

Note: Cortex-M4 with FPU core is binary compatible with the Cortex-M3 core.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 with FPU processors. It balances the inherent performance advantage of the ARM® Cortex®-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 225 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 180 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded Flash memory

The devices embed a Flash memory of 512KB available for storing programs and data.

3.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.6 Embedded SRAM

All devices embed:

- Up to 128Kbytes of system SRAM.

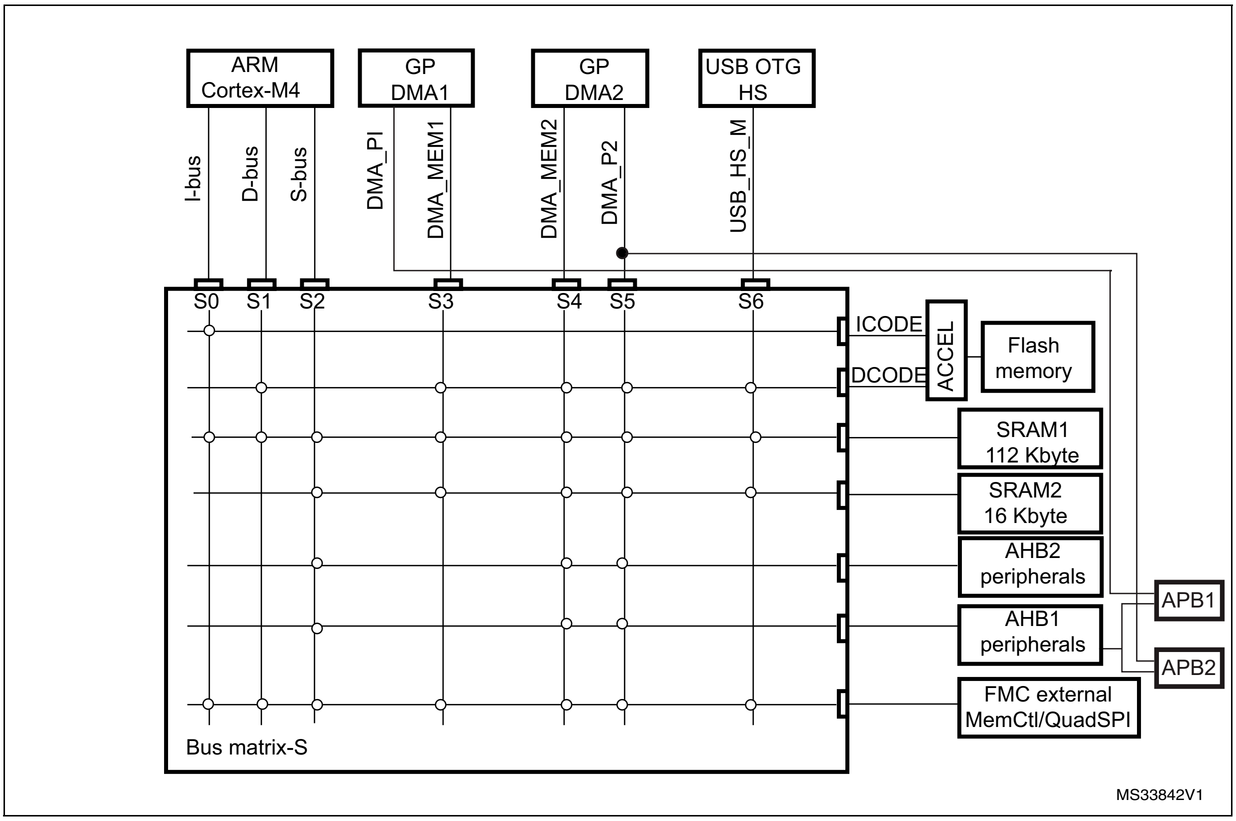
  RAM memory is accessed (read/write) at CPU clock speed with 0 wait states.
- 4 Kbytes of backup SRAM

  This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.

3.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, USB HS) and the slaves Flash memory, RAM, QuadSPI, FMC, AHB and APB peripherals and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 4. STM32F446xC/E and Multi-AHB matrix



3.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I^2S
- I^2C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDIO
- Camera interface (DCMI)
- ADC
- SAI1/SAI2
- SPDIF Receiver (SPDIFRx)
- QuadSPI

3.9 Flexible memory controller (FMC)

All devices embed an FMC. It has seven Chip Select outputs supporting the following modes: SDRAM/LPSDR SDRAM, SRAM, PSRAM, NOR Flash and NAND Flash. With the possibility to remap FMC bank 1 (NOR/PSRAM 1 and 2) and FMC SDRAM bank 1/2 in the Cortex-M4 code area.

Functionality overview:

- 8-,16-bit data bus width
- Read FIFO for SDRAM controller
- Write FIFO
- Maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is 90 MHz.

LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

3.10 Quad SPI memory interface (QUADSPI)

All devices embed a Quad SPI memory interface, which is a specialized communication interface targeting Single, Dual or Quad SPI flash memories. It can work in direct mode through registers, external flash status register polling mode and memory mapped mode. Up to 256 Mbytes external flash are memory mapped, supporting 8, 16 and 32-bit access. Code execution is supported. The opcode and the frame format are fully programmable. Communication can be either in Single Data Rate or Dual Data Rate.

3.11 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 91 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.12 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 114 GPIOs can be connected to the 16 external interrupt lines.

3.13 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy at 25 °C. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 180 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the two AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the two AHB buses is 180 MHz while the maximum frequency of the high-speed APB domains is 90 MHz. The maximum allowed frequency of the low-speed APB domain is 45 MHz.

The devices embed a dedicated PLL (PLLI2S) and PLLSAI which allows to achieve audio class performance. In this case, the I^2S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

3.14 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory through a serial (UART, I^2C, CAN, SPI and USB) communication interface. Refer to application note AN2606 for details.

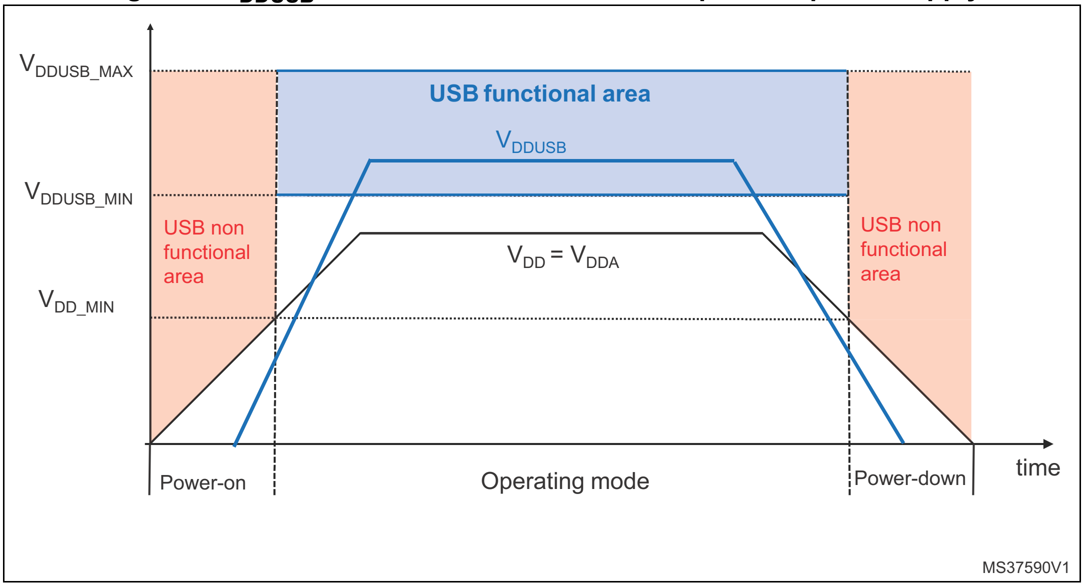
3.15 Power supply schemes

- V_{DD} = 1.7 to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.7 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

Note: V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to Section 3.16.2: Internal reset OFF). Refer to Table 3: Voltage regulator configuration mode versus device operating mode to identify the packages supporting this option.

- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
- V_{DDUSB} can be connected either to VDD or an external independent power supply (3.0 to 3.6V) for USB transceivers.
  For example, when device is powered at 1.8V, an independent power supply 3.3V can be connected to V_{DDUSB}. When the V_{DDUSB} is connected to a separated power supply, it is independent from V_{DD} or V_{DDA} but it must be the last supply to be provided and the first to disappear. The following conditions VDDUSB must be respected:
  - During power-on phase (V_{DD} < VDD_MIN), VDDUSB should be always lower than VDD
  - During power-down phase (VDD < VDD_MIN), VDDUSB should be always lower than VDD
  - VDDUSB rising and falling time rate specifications must be respected.
  - In operating mode phase, V_{DDUSB} could be lower or higher than VDD:
    - If USB (USB OTG_HS/OTG_FS) is used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DDUSB_MIN} and V_{DDUSB_MAX}.The V_{DDUSB} supply both USB transceiver (USB OTG_HS and USB OTG_FS).
    - If only one USB transceiver is used in the application, the GPIOs associated to the other USB transceiver are still supplied by V_{DDUSB}.
    - If USB (USB OTG_HS/OTG_FS) is not used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DD_MIN} and V_{DD_MAX}.

Figure 5. V_{DDUSB} connected to an external independent power supply



3.16 Power supply supervisor

3.16.1 Internal reset ON

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On the other package, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default BOR thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit.

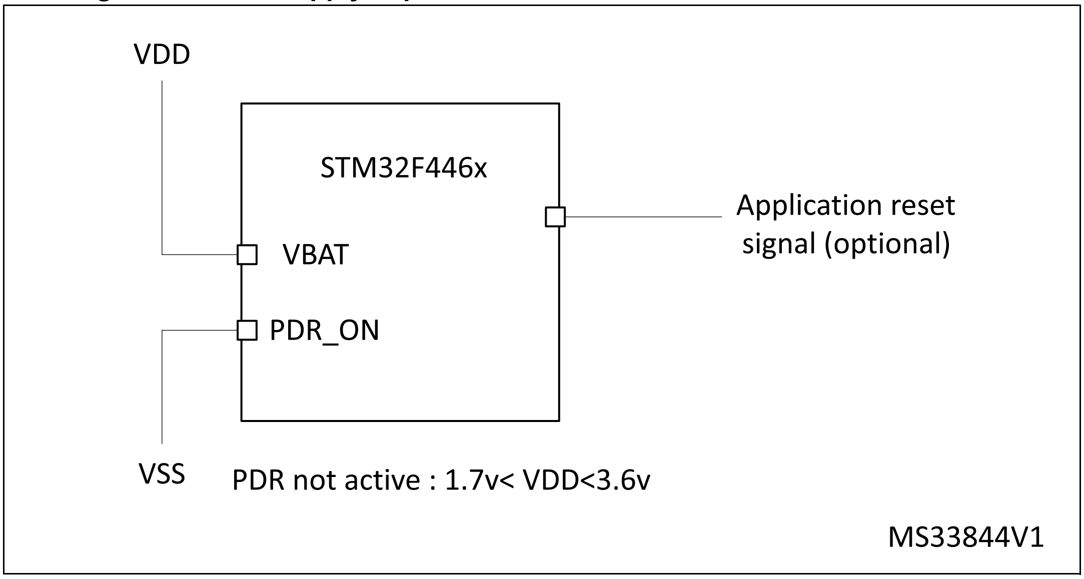
The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.16.2 Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled through the PDR_ON pin.

An external power supply supervisor should monitor V_{DD} and should maintain the device in reset mode as long as V_{DD} is below a specified threshold. PDR_ON should be connected to VSS, to allows device to operate down to 1.7v. Refer to *Figure 6: Power supply supervisor interconnection with internal reset OFF*.

Figure 6. Power supply supervisor interconnection with internal reset OFF



The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.7 V.

A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry must be disabled
- The embedded programmable voltage detector (PVD) is disabled
- V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}.

All packages, except for the LQFP100/LQFP64, allow to disable the internal reset through the PDR_ON signal.

3.17 Voltage regulator

The regulator has four operating modes:

- Regulator ON
  - Main regulator mode (MR)
  - Low power regulator (LPR)
  - Power-down
- Regulator OFF

3.17.1 Regulator ON

On packages embedding the BYPASS_REG pin, the regulator is enabled by holding BYPASS_REG low. On all other packages, the regulator is always enabled.

There are three power modes configured by software when the regulator is ON:

- MR mode used in Run/sleep modes or in Stop modes
  - In Run/Sleep mode

    The MR mode is used either in the normal mode (default mode) or the over-drive mode (enabled by software). Different voltages scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption. The over-drive mode allows operating at a higher frequency than the normal mode for a given voltage scaling.
  - In Stop modes

    The MR can be configured in two ways during stop mode:

    MR operates in normal mode (default mode of MR in stop mode)

    MR operates in under-drive mode (reduced leakage mode).
- LPR is used in the Stop modes:

  The LP regulator mode is configured by software when entering Stop mode.

  Like the MR mode, the LPR can be configured in two ways during stop mode:
  - LPR operates in normal mode (default mode when LPR is ON)
  - LPR operates in under-drive mode (reduced leakage mode).
- Power-down is used in Standby mode.

  The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Refer to *Table 3* for a summary of voltage regulator modes versus device operating modes.

Two external ceramic capacitors should be connected on V_{CAP_1} and V_{CAP_2} pin.

All packages have the regulator ON feature.

Table 3. Voltage regulator configuration mode versus device operating mode(1)

Voltage regulator configuration	Run mode	Sleep mode	Stop mode	Standby mode
Normal mode	MR	MR	MR or LPR	-
Over-drive mode(2)	MR	MR	-	-
Under-drive mode	-	-	MR or LPR	-
Power-down mode	-	-	-	Yes

1. '-' means that the corresponding configuration is not available.
2. The over-drive mode is not available when V_{DD} = 1.7 to 2.1 V.

3.17.2 Regulator OFF

This feature is available only on packages featuring the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a V_{12} voltage source through V_{CAP_1} and V_{CAP_2} pins.