



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

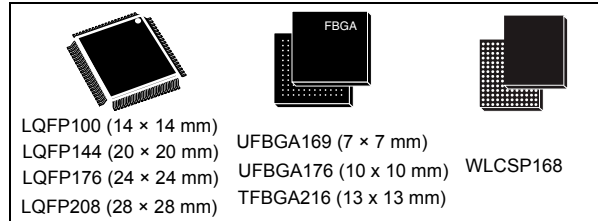


ARM[®]Cortex[®]-M4 32b MCU+FPU, 225DMIPS, up to 2MB Flash/384+4KB RAM, USB OTG HS/FS, Ethernet, FMC, dual Quad-SPI, Graphical accelerator, Camera IF, LCD-TFT & MIPI DSI

Datasheet - production data

Features

- Core: ARM[®] 32-bit Cortex[®]-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator[™]) allowing 0-wait state execution from Flash memory, frequency up to 180 MHz, MPU, 225 DMIPS/1.25 DMIPS/MHz (Dhystone 2.1), and DSP instructions
- Memories
 - Up to 2 MB of Flash memory organized into two banks allowing read-while-write
 - Up to 384+4 KB of SRAM including 64 KB of CCM (core coupled memory) data RAM
 - Flexible external memory controller with up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPDDR, SDRAM, Flash NOR/NAND memories
 - Dual-flash mode Quad-SPI interface
- Graphics:
 - Chrom-ART Accelerator[™] (DMA2D), graphical hardware accelerator enabling enhanced graphical user interface with minimum CPU load
 - LCD parallel interface, 8080/6800 modes
 - LCD TFT controller supporting up to XGA resolution
 - MIPI[®] DSI host controller supporting up to 720p 30Hz resolution
- Clock, reset and supply management
 - 1.7 V to 3.6 V application supply and I/Os
 - POR, PDR, PVD and BOR
 - 4-to-26 MHz crystal oscillator
 - Internal 16 MHz factory-trimmed RC (1% accuracy)
 - 32 kHz oscillator for RTC with calibration
 - Internal 32 kHz RC with calibration
- Low power
 - Sleep, Stop and Standby modes
 - V_{BAT} supply for RTC, 20×32 bit backup registers + optional 4 KB backup SRAM
- 3×12-bit, 2.4 MSPS ADC: up to 24 channels and 7.2 MSPS in triple interleaved mode
- 2×12-bit D/A converters
- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Up to 17 timers: up to twelve 16-bit and two 32-bit timers up to 180 MHz, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input. 2x watchdogs and SysTick timer



- Debug mode
 - SWD & JTAG interfaces
 - Cortex[®]-M4 Trace Macrocell[™]
- Up to 161 I/O ports with interrupt capability
 - Up to 157 fast I/Os up to 90 MHz
 - Up to 159 5 V-tolerant I/Os
- Up to 21 communication interfaces
 - Up to 3 × I²C interfaces (SMBus/PMBus)
 - Up to 4 USARTs and 4 UARTs (11.25 Mbit/s, ISO7816 interface, LIN, IrDA, modem control)
 - Up to 6 SPIs (45 Mbits/s), 2 with muxed full-duplex I²S for audio class accuracy via internal audio PLL or external clock
 - 1 × SAI (serial audio interface)
 - 2 × CAN (2.0B Active)
 - SDIO interface
- Advanced connectivity
 - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
 - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
 - Dedicated USB power rail enabling on-chip PHYs operation throughout the entire MCU power supply range
 - 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII
- 8- to 14-bit parallel camera interface up to 54 Mbytes/s
- True random number generator
- CRC calculation unit
- RTC: subsecond accuracy, hardware calendar
- 96-bit unique ID

Table 1. Device summary

Reference	Part numbers
STM32F469xx	STM32F469AE, STM32F469AG, STM32F469AI STM32F469BE, STM32F469BG, STM32F469BI STM32F469IE, STM32F469IG, STM32F469II STM32F469NE, STM32F469NG, STM32F469NI STM32F469VE, STM32F469VG, STM32F469VI STM32F469ZE, STM32F469ZG, STM32F469ZI

Contents

1	Description	12
1.1	Compatibility throughout the family	15
1.1.1	LQFP176 package	16
1.1.2	LQFP208 package	17
1.1.3	UFPGA176 package	18
1.1.4	TFPGA216 package	19
2	Functional overview	21
2.1	ARM® Cortex®-M4 with FPU and embedded Flash and SRAM	21
2.2	Adaptive real-time memory accelerator (ART Accelerator™)	21
2.3	Memory protection unit	21
2.4	Embedded Flash memory	22
2.5	CRC (cyclic redundancy check) calculation unit	22
2.6	Embedded SRAM	22
2.7	Multi-AHB bus matrix	22
2.8	DMA controller (DMA)	23
2.9	Flexible Memory Controller (FMC)	24
2.10	Quad-SPI memory interface (QUADSPI)	25
2.11	LCD-TFT controller	25
2.12	DSI Host (DSIHOST)	25
2.13	Chrom-ART Accelerator™ (DMA2D)	27
2.14	Nested vectored interrupt controller (NVIC)	27
2.15	External interrupt/event controller (EXTI)	27
2.16	Clocks and startup	28
2.17	Boot modes	28
2.18	Power supply schemes	28
2.19	Power supply supervisor	30
2.19.1	Internal reset ON	30
2.19.2	Internal reset OFF	30
2.20	Voltage regulator	31
2.20.1	Regulator ON	31
2.20.2	Regulator OFF	32

2.20.3	Regulator ON/OFF and internal reset ON/OFF availability	35
2.21	Real-time clock (RTC), backup SRAM and backup registers	35
2.22	Low-power modes	36
2.23	V _{BAT} operation	36
2.24	Timers and watchdogs	37
2.24.1	Advanced-control timers (TIM1, TIM8)	38
2.24.2	General-purpose timers (TIMx)	38
2.24.3	Basic timers TIM6 and TIM7	38
2.24.4	Independent watchdog	39
2.24.5	Window watchdog	39
2.24.6	SysTick timer	39
2.25	Inter-integrated circuit interface (I ² C)	39
2.26	Universal synchronous/asynchronous receiver transmitters (USART)	39
2.27	Serial peripheral interface (SPI)	40
2.28	Inter-integrated sound (I ² S)	41
2.29	Serial Audio interface (SAI1)	41
2.30	Audio PLL (PLLI2S)	41
2.31	Audio and LCD PLL(PLLSAI)	41
2.32	Secure digital input/output interface (SDIO)	42
2.33	Ethernet MAC interface with dedicated DMA and IEEE 1588 support	42
2.34	Controller area network (bxCAN)	42
2.35	Universal serial bus on-the-go full-speed (OTG_FS)	43
2.36	Universal serial bus on-the-go high-speed (OTG_HS)	43
2.37	Digital camera interface (DCMI)	44
2.38	Random number generator (RNG)	44
2.39	General-purpose input/outputs (GPIOs)	44
2.40	Analog-to-digital converters (ADCs)	45
2.41	Temperature sensor	45
2.42	Digital-to-analog converter (DAC)	45
2.43	Serial wire JTAG debug port (SWJ-DP)	46
2.44	Embedded Trace Macrocell™	46
3	Pinouts and pin description	47

4 Memory mapping 83

5 Electrical characteristics 88

5.1 Parameter conditions 88

5.1.1 Minimum and maximum values 88

5.1.2 Typical values 88

5.1.3 Typical curves 88

5.1.4 Loading capacitor 88

5.1.5 Pin input voltage 88

5.1.6 Power supply scheme 89

5.1.7 Current consumption measurement 90

5.2 Absolute maximum ratings 90

5.3 Operating conditions 92

5.3.1 General operating conditions 92

5.3.2 VCAP1/VCAP2 external capacitor 94

5.3.3 Operating conditions at power-up / power-down (regulator ON) 95

5.3.4 Operating conditions at power-up / power-down (regulator OFF) 95

5.3.5 Reset and power control block characteristics 95

5.3.6 Over-drive switching characteristics 97

5.3.7 Supply current characteristics 97

5.3.8 Wakeup time from low-power modes 113

5.3.9 External clock source characteristics 114

5.3.10 Internal clock source characteristics 118

5.3.11 PLL characteristics 119

5.3.12 PLL spread spectrum clock generation (SSCG) characteristics 122

5.3.13 MIPI D-PHY characteristics 123

5.3.14 MIPI D-PHY PLL characteristics 126

5.3.15 MIPI D-PHY regulator characteristics 127

5.3.16 Memory characteristics 128

5.3.17 EMC characteristics 130

5.3.18 Absolute maximum ratings (electrical sensitivity) 131

5.3.19 I/O current injection characteristics 132

5.3.20 I/O port characteristics 133

5.3.21 NRST pin characteristics 139

5.3.22 TIM timer characteristics 140

5.3.23 Communications interfaces 140

5.3.24 12-bit ADC characteristics 155



5.3.25	Temperature sensor characteristics	161
5.3.26	V _{BAT} monitoring characteristics	161
5.3.27	Reference voltage	161
5.3.28	DAC electrical characteristics	162
5.3.29	FMC characteristics	164
5.3.30	Quad-SPI interface characteristics	184
5.3.31	Camera interface (DCMI) timing specifications	185
5.3.32	LCD-TFT controller (LTDC) characteristics	186
5.3.33	SD/SDIO MMC card host interface (SDIO) characteristics	188
5.3.34	RTC characteristics	190
6	Package information	191
6.1	LQFP100 package information	191
6.2	LQFP144 package information	194
6.3	WLCSP168 package information	197
6.4	UFBGA169 package information	199
6.5	LQFP176 package information	201
6.6	UFBGA176+25 package information	205
6.7	LQFP208 package information	207
6.8	TFBGA216 package information	211
6.9	Thermal characteristics	213
7	Part numbering	214
	Appendix A Recommendations when using internal reset OFF	215
A.1	Operating conditions	215
	Revision history	216

List of tables

Table 1.	Device summary	1
Table 2.	STM32F469xx features and peripheral counts	13
Table 3.	Voltage regulator configuration mode versus device operating mode	32
Table 4.	Regulator ON/OFF and internal reset ON/OFF availability	35
Table 5.	Voltage regulator modes in stop mode	36
Table 6.	Timer feature comparison	37
Table 7.	Comparison of I2C analog and digital filters	39
Table 8.	USART feature comparison	40
Table 9.	Legend/abbreviations used in the pinout table	55
Table 10.	STM32F469xx pin and ball definitions	56
Table 11.	FMC pin definition	70
Table 12.	Alternate function	73
Table 13.	STM32F469xx register boundary addresses	84
Table 14.	Voltage characteristics	90
Table 15.	Current characteristics	91
Table 16.	Thermal characteristics	91
Table 17.	General operating conditions	92
Table 18.	Limitations depending on the operating power supply range	94
Table 19.	VCAP1/VCAP2 operating conditions	95
Table 20.	Operating conditions at power-up / power-down (regulator ON)	95
Table 21.	Operating conditions at power-up / power-down (regulator OFF)	95
Table 22.	Reset and power control block characteristics	96
Table 23.	Over-drive switching characteristics	97
Table 24.	Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM, regulator ON	99
Table 25.	Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled), regulator ON	100
Table 26.	Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch), regulator OFF	101
Table 27.	Typical and maximum current consumption in Sleep mode, regulator ON	102
Table 28.	Typical and maximum current consumption in Sleep mode, regulator OFF	103
Table 29.	Typical and maximum current consumption in Stop mode	104
Table 30.	Typical and maximum current consumption in Standby mode	105
Table 31.	Typical and maximum current consumption in V _{BAT} mode	106
Table 32.	Switching output I/O current consumption	108
Table 33.	Peripheral current consumption	110
Table 34.	Low-power mode wakeup timings	113
Table 35.	High-speed external user clock characteristics	114
Table 36.	Low-speed external user clock characteristics	114
Table 37.	HSE 4-26 MHz oscillator characteristics	116
Table 38.	LSE oscillator characteristics (f _{LSE} = 32.768 kHz)	117
Table 39.	HSI oscillator characteristics	118
Table 40.	LSI oscillator characteristics	119
Table 41.	Main PLL characteristics	119
Table 42.	PLL12S (audio PLL) characteristics	120
Table 43.	PLLSAI (audio and LCD-TFT PLL) characteristics	121

Table 44.	SSCG parameters constraint	122
Table 45.	MIPI D-PHY characteristics	123
Table 46.	MIPI D-PHY AC characteristics LP mode and HS/LP transitions	125
Table 47.	DSI-PLL characteristics	126
Table 48.	DSI regulator characteristics	127
Table 49.	Flash memory characteristics	128
Table 50.	Flash memory programming	128
Table 51.	Flash memory programming with V_{PP}	129
Table 52.	Flash memory endurance and data retention	130
Table 53.	EMS characteristics	130
Table 54.	EMI characteristics	131
Table 55.	ESD absolute maximum ratings	132
Table 56.	Electrical sensitivities	132
Table 57.	I/O current injection susceptibility	133
Table 58.	I/O static characteristics	133
Table 59.	Output voltage characteristics	136
Table 60.	I/O AC characteristics	137
Table 61.	NRST pin characteristics	139
Table 62.	TIMx characteristics	140
Table 63.	I2C analog filter characteristics	140
Table 64.	SPI dynamic characteristics	141
Table 65.	I ² S dynamic characteristics	145
Table 66.	SAI characteristics	147
Table 67.	USB OTG full speed startup time	149
Table 68.	USB OTG full speed DC electrical characteristics	149
Table 69.	USB OTG full speed electrical characteristics	150
Table 70.	USB HS DC electrical characteristics	150
Table 71.	USB HS clock timing parameters	151
Table 72.	Dynamic characteristics: USB ULPI	152
Table 73.	Dynamics characteristics: Ethernet MAC signals for SMI	153
Table 74.	Dynamics characteristics: Ethernet MAC signals for RMII	154
Table 75.	Dynamics characteristics: Ethernet MAC signals for MII	154
Table 76.	ADC characteristics	155
Table 77.	ADC static accuracy at $f_{ADC} = 18$ MHz	157
Table 78.	ADC static accuracy at $f_{ADC} = 30$ MHz	157
Table 79.	ADC static accuracy at $f_{ADC} = 36$ MHz	157
Table 80.	ADC dynamic accuracy at $f_{ADC} = 18$ MHz - limited test conditions	158
Table 81.	ADC dynamic accuracy at $f_{ADC} = 36$ MHz - limited test conditions	158
Table 82.	Temperature sensor characteristics	161
Table 83.	Temperature sensor calibration values	161
Table 84.	V_{BAT} monitoring characteristics	161
Table 85.	internal reference voltage	161
Table 86.	Internal reference voltage calibration values	162
Table 87.	DAC characteristics	162
Table 88.	Asynchronous non-multiplexed SRAM/PSRAM/NOR - read timings	166
Table 89.	Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings	166
Table 90.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings	167
Table 91.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings	168
Table 92.	Asynchronous multiplexed PSRAM/NOR read timings	169
Table 93.	Asynchronous multiplexed PSRAM/NOR read-NWAIT timings	169
Table 94.	Asynchronous multiplexed PSRAM/NOR write timings	170
Table 95.	Asynchronous multiplexed PSRAM/NOR write-NWAIT timings	171

Table 96.	Synchronous multiplexed NOR/PSRAM read timings	173
Table 97.	Synchronous multiplexed PSRAM write timings	175
Table 98.	Synchronous non-multiplexed NOR/PSRAM read timings	176
Table 99.	Synchronous non-multiplexed PSRAM write timings	177
Table 100.	Switching characteristics for NAND Flash read cycles	180
Table 101.	Switching characteristics for NAND Flash write cycles	180
Table 102.	SDRAM read timings	181
Table 103.	LPSDR SDRAM read timings	182
Table 104.	SDRAM write timings	183
Table 105.	LPSDR SDRAM write timings	183
Table 106.	Quad-SPI characteristics in SDR mode	184
Table 107.	Quad-SPI characteristics in DDR mode	185
Table 108.	DCMI characteristics	186
Table 109.	LTDC characteristics	187
Table 110.	Dynamic characteristics: SD / MMC characteristics, VDD = 2.7 to 3.6 V	189
Table 111.	Dynamic characteristics: SD / MMC characteristics, VDD = 1.71 to 1.9 V	190
Table 112.	RTC characteristics	190
Table 113.	LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data	192
Table 114.	LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data	195
Table 115.	WLCSP168 - 168-pin, 4.891 x 5.692 mm, 0.4 mm pitch wafer level chip scale package mechanical data	198
Table 116.	UFBGA169 - 169-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data	199
Table 117.	LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package mechanical data	201
Table 118.	UFBGA176+25, - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data	205
Table 119.	UFBGA176+25 recommended PCB design rules (0.65 mm pitch BGA)	206
Table 120.	LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package mechanical data	207
Table 121.	TFBGA216 - thin fine pitch ball grid array 13 x 13 x 0.8mm package mechanical data	211
Table 122.	Package thermal characteristics	213
Table 123.	Ordering information scheme	214
Table 124.	Limitations depending on the operating power supply range	215
Table 125.	Document revision history	216

List of figures

Figure 1.	Incompatible board design for LQFP176 package	16
Figure 2.	Incompatible board design for LQFP208 package	17
Figure 3.	UFBGA176 port-to-terminal assignment differences	18
Figure 4.	TFBGA216 port-to-terminal assignment differences.	19
Figure 5.	STM32F469xx block diagram	20
Figure 6.	STM32F469xx Multi-AHB matrix	23
Figure 7.	VDDUSB connected to an external independent power supply	29
Figure 8.	Power supply supervisor interconnection with internal reset OFF	30
Figure 9.	PDR_ON control with internal reset OFF	31
Figure 10.	Regulator OFF	33
Figure 11.	Startup in regulator OFF: slow V_{DD} slope - power-down reset risen after V_{CAP_1} , V_{CAP_2} stabilization	34
Figure 12.	Startup in regulator OFF mode: fast V_{DD} slope - power-down reset risen before V_{CAP_1} , V_{CAP_2} stabilization	34
Figure 13.	STM32F46x LQFP100 pinout	47
Figure 14.	STM32F46x LQFP144 pinout	48
Figure 15.	STM32F46x WLCSP168 pinout	49
Figure 16.	STM32F46x UFBGA169 ballout	50
Figure 17.	STM32F46x UFBGA176 ballout	51
Figure 18.	STM32F46x LQFP176 pinout	52
Figure 19.	STM32F46x LQFP208 pinout	53
Figure 20.	STM32F46x TFBGA216 ballout	54
Figure 21.	Memory map	83
Figure 22.	Pin loading conditions	88
Figure 23.	Pin input voltage	88
Figure 24.	Power supply scheme	89
Figure 25.	Current consumption measurement scheme	90
Figure 26.	External capacitor C_{EXT}	94
Figure 27.	Typical V_{BAT} current consumption (RTC ON / backup SRAM ON and LSE in Low drive mode)	106
Figure 28.	Typical V_{BAT} current consumption (RTC ON / backup SRAM ON and LSE in High drive mode)	107
Figure 29.	High-speed external clock source AC timing diagram	115
Figure 30.	Low-speed external clock source AC timing diagram	115
Figure 31.	Typical application with an 8 MHz crystal	116
Figure 32.	Typical application with a 32.768 kHz crystal	117
Figure 33.	ACC _{HSI} vs. temperature	118
Figure 34.	ACC _{LSI} versus temperature	119
Figure 35.	PLL output clock waveforms in center spread mode	123
Figure 36.	PLL output clock waveforms in down spread mode	123
Figure 37.	MIPI D-PHY HS/LP clock lane transition timing diagram	126
Figure 38.	MIPI D-PHY HS/LP data lane transition timing diagram	126
Figure 39.	FT I/O input characteristics	135
Figure 40.	I/O AC characteristics definition	138
Figure 41.	Recommended NRST pin protection	139
Figure 42.	SPI timing diagram - slave mode and CPHA = 0	143
Figure 43.	SPI timing diagram - slave mode and CPHA = 1 ⁽¹⁾	143
Figure 44.	SPI timing diagram - master mode ⁽¹⁾	144

Figure 45.	I ² S slave timing diagram (Philips protocol) ⁽¹⁾	146
Figure 46.	I ² S master timing diagram (Philips protocol) ⁽¹⁾	146
Figure 47.	SAI master timing waveforms	148
Figure 48.	SAI slave timing waveforms	148
Figure 49.	USB OTG full speed timings: definition of data signal rise and fall time	150
Figure 50.	ULPI timing diagram	151
Figure 51.	Ethernet SMI timing diagram	152
Figure 52.	Ethernet RMII timing diagram	153
Figure 53.	Ethernet MII timing diagram	154
Figure 54.	ADC accuracy characteristics	159
Figure 55.	Typical connection diagram using the ADC	159
Figure 56.	Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})	160
Figure 57.	Power supply and reference decoupling (V_{REF+} connected to V_{DDA})	160
Figure 58.	12-bit buffered/non-buffered DAC	164
Figure 59.	Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms	165
Figure 60.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms	167
Figure 61.	Asynchronous multiplexed PSRAM/NOR read waveforms	168
Figure 62.	Asynchronous multiplexed PSRAM/NOR write waveforms	170
Figure 63.	Synchronous multiplexed NOR/PSRAM read timings	172
Figure 64.	Synchronous multiplexed PSRAM write timings	174
Figure 65.	Synchronous non-multiplexed NOR/PSRAM read timings	176
Figure 66.	Synchronous non-multiplexed PSRAM write timings	177
Figure 67.	NAND controller waveforms for read access	178
Figure 68.	NAND controller waveforms for write access	179
Figure 69.	NAND controller waveforms for common memory read access	179
Figure 70.	NAND controller waveforms for common memory write access	180
Figure 71.	SDRAM read access waveforms (CL = 1)	181
Figure 72.	SDRAM write access waveforms	182
Figure 73.	Quad-SPI SDR timing diagram	184
Figure 74.	Quad-SPI DDR timing diagram	185
Figure 75.	DCMI timing diagram	186
Figure 76.	LCD-TFT horizontal timing diagram	187
Figure 77.	LCD-TFT vertical timing diagram	188
Figure 78.	SDIO high-speed mode	188
Figure 79.	SD default mode	189
Figure 80.	LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline	191
Figure 81.	LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint	193
Figure 82.	LQFP100 marking example (package top view)	193
Figure 83.	LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline	194
Figure 84.	LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package recommended footprint	196
Figure 85.	LQFP144 marking example (package top view)	196
Figure 86.	WLCSP168 - 168-pin, 4.891 x 5.692 mm, 0.4 mm pitch wafer level chip scale package outline	197
Figure 87.	UFPGA169 - 169-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline	199
Figure 88.	UFPGA169 marking example (package top view)	200
Figure 89.	LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package outline	201
Figure 90.	LQFP176 recommended footprint	203
Figure 91.	LQFP176 marking example (package top view)	204
Figure 92.	UFPGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch,	

	ultra fine pitch ball grid array package outline	205
Figure 93.	UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package recommended footprint	206
Figure 94.	LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package outline	207
Figure 95.	LQFP208 recommended footprint	209
Figure 96.	LQFP208 marking example (package top view)	210
Figure 97.	TFBGA216 - thin fine pitch ball grid array 13 x 13 x 0.8mm, package outline	211
Figure 98.	TFBGA216 marking example (package top view)	212

1 Description

The STM32F469xx devices are based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 180 MHz. The Cortex®-M4 core features a Floating point unit (FPU) single precision which supports all ARM® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F469xx devices incorporate high-speed embedded memories (Flash memory up to 2 Mbytes, up to 384 Kbytes of SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers, and a true random number generator (RNG). They also feature standard and advanced communication interfaces:

- Up to three I²Cs
- Six SPIs, two I²Ss full duplex. To achieve audio class accuracy, the I²S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus four UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI),
- Two CANs
- One SAI serial audio interface
- An SDMMC host interface
- Ethernet and camera interface
- LCD-TFT display controller
- Chrom-ART Accelerator™
- DSI Host.

Advanced peripherals include an SDMMC interface, a flexible memory control (FMC) interface, a Quad-SPI Flash memory, and camera interface for CMOS sensors. Refer to [Table 2](#) for the list of peripherals available on each part number.

The STM32F469xx devices operate in the –40 to +105 °C temperature range from a 1.7 to 3.6 V power supply. A dedicated supply input for USB (OTG_FS and OTG_HS) only in full speed mode, is available on all packages.

The supply voltage can drop to 1.7 V (refer to [Section 2.19.2](#)). A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F469xx devices are offered in eight packages, ranging from 100 to 216 pins. The set of included peripherals changes with the device chosen, according to [Table 2](#).

These features make the STM32F469xx microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances

Figure 5 shows the general block diagram of the device family.

Table 2. STM32F469xx features and peripheral counts

Peripherals		STM32F469Vx	STM32F469Zx	STM32F469Ax	STM32F469Jx	STM32F469Bx	STM32F469Nxx	
Flash memory in Kbytes		512 1024 2048	512 1024 2048	512 1024 2048	512 1024 2048	512 1024 2048	512 1024 2048	
SRAM in Kbytes	System	384 (160+32+128+64)						
	Backup	4						
FMC memory controller		Yes						
Quad-SPI		Yes						
Ethernet		No			Yes			
Timers	General-purpose	10						
	Advanced-control	2						
	Basic	2						
Random number generator		Yes						
Communication interfaces	SPI / I ² S	4/2(full duplex) ⁽¹⁾		6/2(full duplex) ⁽¹⁾				
	I ² C	3						
	USART/UART	4/3		4/4				
	USB OTG FS	Yes						
	USB OTG HS	Yes						
	CAN	2						
	SAI	1						
SDIO	Yes							
Camera interface		Yes						

Table 2. STM32F469xx features and peripheral counts (continued)

Peripherals	STM32F469Vx	STM32F469Zx	STM32F469Ax	STM32F469Ix	STM32F469Bx	STM32F469Nx
MIPI-DSI Host	Yes					
LCD-TFT	Yes					
Chrom-ART Accelerator™ (DMA2D)	Yes					
GPIOs	71	106	114	131	161	161
12-bit ADC Number of channels	3					
	14	20	24	16	24	24
12-bit DAC Number of channels	Yes 2					
Maximum CPU frequency	180 MHz					
Operating voltage	1.7 to 3.6V ⁽²⁾					
Operating temperatures	Ambient operating temperature: -40 to 85 °C / -40 to 105 °C Junction temperature: -40 to 105 °C / -40 to 125 °C					
Package	LQFP100	LQPF144	UFBGA169 WLCSP168	LQFP176 UFBGA176	LQFP208	TFBGA216

1. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
2. VDD/VDDA minimum value of 1.7 V is obtained when the internal reset is OFF (refer to [Section 2.19.2](#)).

1.1 Compatibility throughout the family

STM32F469xx devices are not compatible with other STM32F4xx devices.

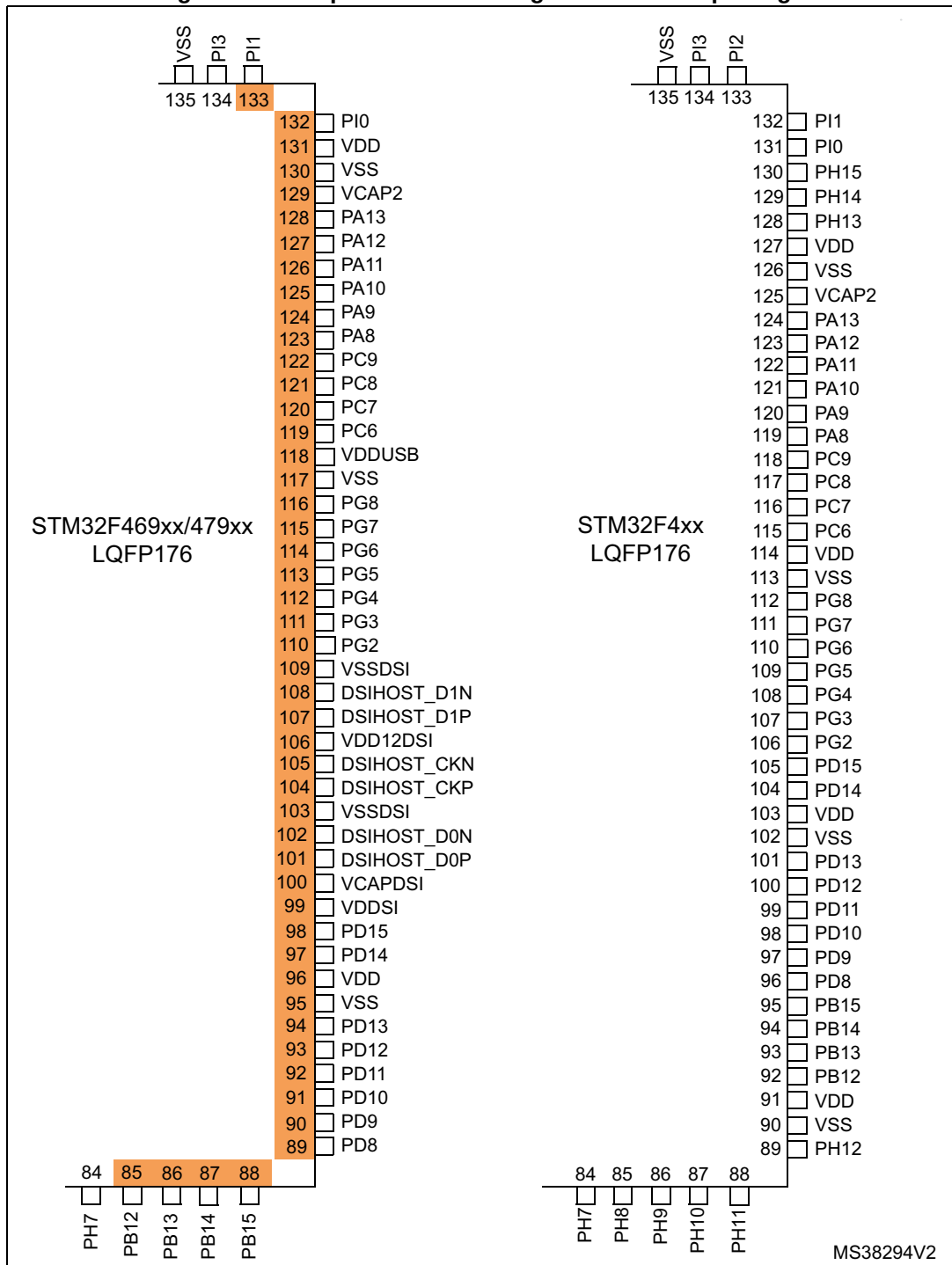
Figure 1 and *Figure 2* show incompatible board designs, respectively, for LQFP176 and LQFP208 packages (highlighted pins).

The UFBGA176 and TFBGA216 ballouts are compatible with other STM32F4xx devices, only few IO port pins are substituted, as shown in *Figure 3* and *Figure 4*.

The LQFP100, LQFP144 and UFBGA169 packages are incompatible with other STM32F4xx devices.

1.1.1 LQFP176 package

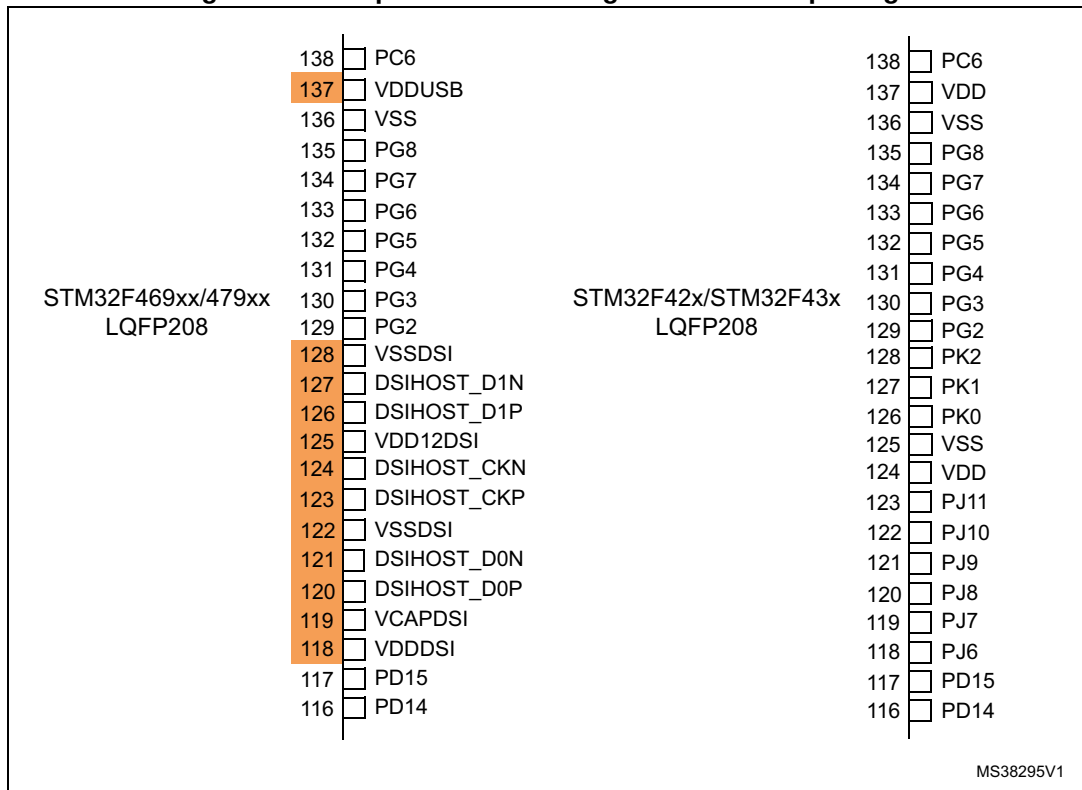
Figure 1. Incompatible board design for LQFP176 package



1. Pins from 85 to 133 are not compatible.

1.1.2 LQFP208 package

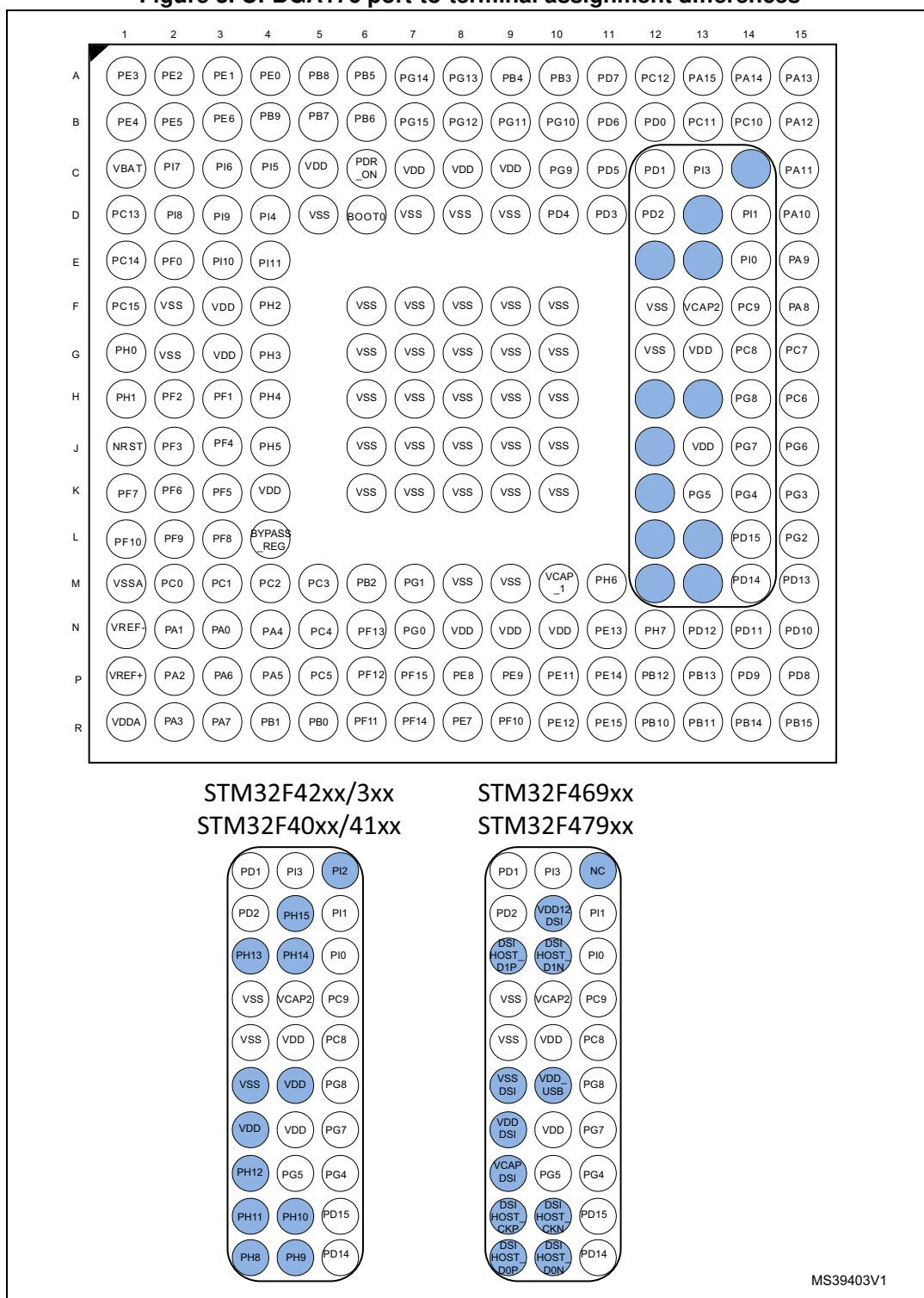
Figure 2. Incompatible board design for LQFP208 package



1. Pins from 118 to 128 and pin 137 are not compatible

1.1.3 UFBGA176 package

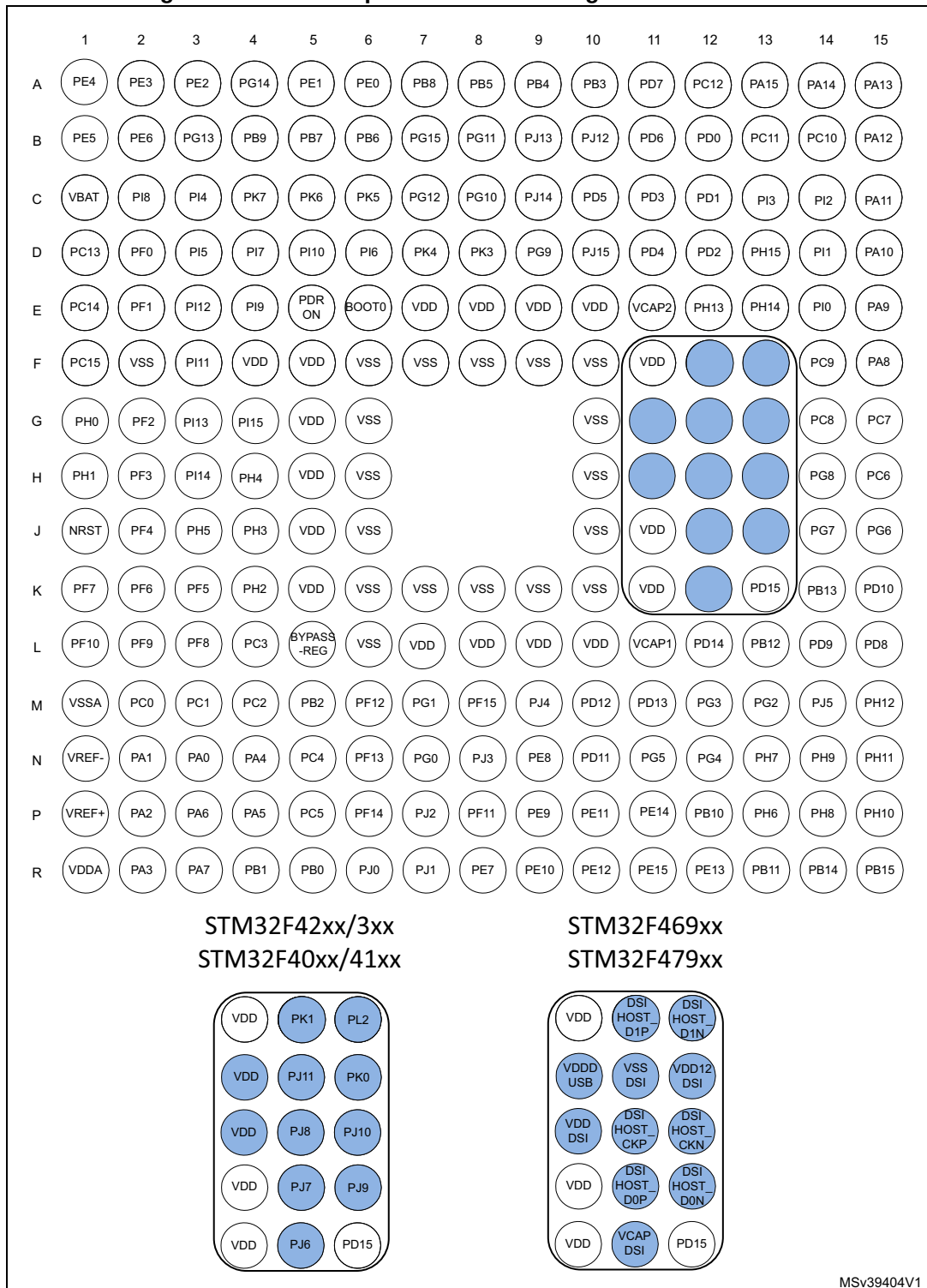
Figure 3. UFBGA176 port-to-terminal assignment differences



- The highlighted pins are substituted with dedicated DSI IO pins on STM32F469xx/479xx devices.

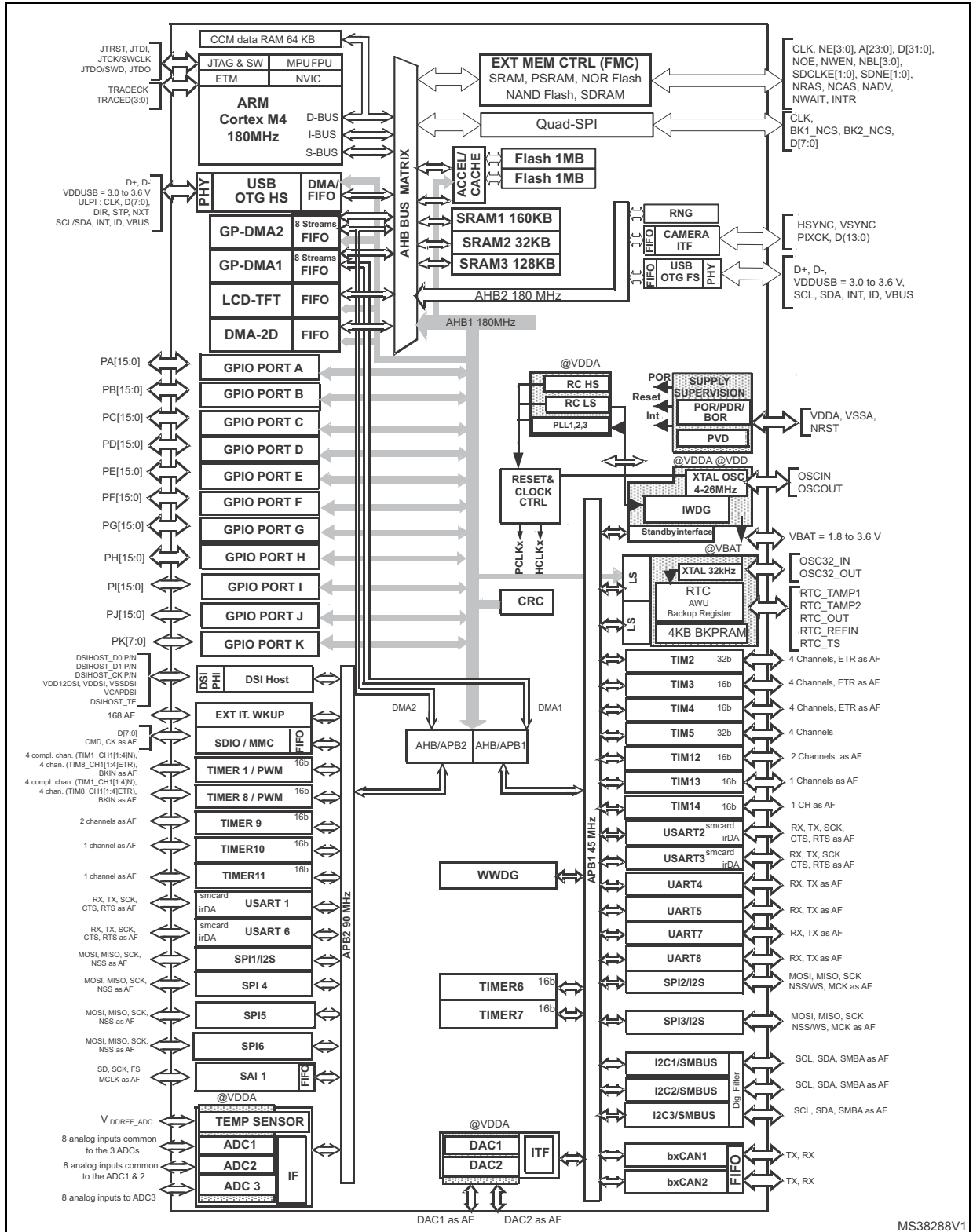
1.1.4 TFBGA216 package

Figure 4. TFBGA216 port-to-terminal assignment differences



1. The highlighted pins are substituted with dedicated DSI IO pins on STM32F469xx/479xx devices.

Figure 5. STM32F469xx block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 180 MHz, while the timers connected to APB1 are clocked from TIMxCLK either up to 90 MHz or 180 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

2 Functional overview

2.1 ARM[®] Cortex[®]-M4 with FPU and embedded Flash and SRAM

The ARM[®] Cortex[®]-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM[®] Cortex[®]-M4 with FPU core is a 32-bit RISC processor that features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F46x line is compatible with all ARM tools and software.

Figure 5 shows the general block diagram of the STM32F46x line.

Note: Cortex[®]-M4 with FPU core is binary compatible with the Cortex[®]-M3 core.

2.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator optimized for STM32 industry-standard ARM[®] Cortex[®]-M4 with FPU processors. It balances the inherent performance advantage of the ARM[®] Cortex[®]-M4 with FPU over Flash memory technologies, which normally require the processor to wait for the Flash memory at higher frequencies.

To release the processor full 225 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark[®] benchmark, the performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 180 MHz.

2.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.4 Embedded Flash memory

The devices embed a Flash memory of up to 2 Mbytes available for storing programs and data.

2.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.6 Embedded SRAM

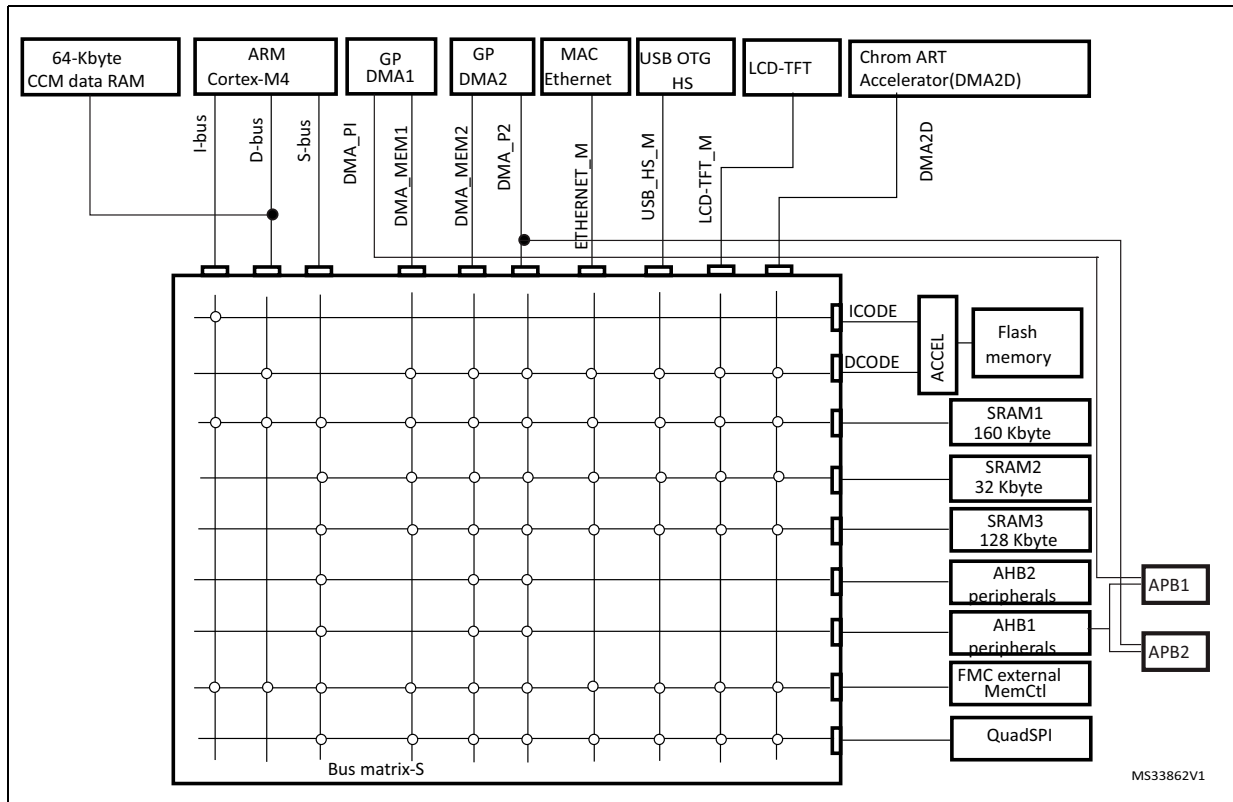
All devices embed:

- Up to 384Kbytes of system SRAM including 64 Kbytes of CCM (core coupled memory) data RAM
RAM memory is accessed (read/write) at CPU clock speed with 0 wait states.
- 4 Kbytes of backup SRAM
This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or VBAT mode.

2.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS, LCD-TFT, and DMA2D) and the slaves (Flash memory, RAM, FMC, QUADSPI, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 6. STM32F469xx Multi-AHB matrix



2.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I²S
- I²C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDIO
- Camera interface (DCMI)
- ADC
- SAI1
- QUADSPI.

2.9 Flexible Memory Controller (FMC)

The Flexible memory controller (FMC) includes three memory controllers:

- The NOR/PSRAM memory controller
- The NAND/memory controller
- The Synchronous DRAM (SDRAM/Mobile LPDDR SDRAM) controller

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
 - Static random access memory (SRAM)
 - NOR Flash memory/OneNAND Flash memory
 - PSRAM
 - NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPDDR SDRAM) memories
- 8-,16-,32-bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The Maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is HCLK/2.

LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

2.10 Quad-SPI memory interface (QUADSPI)

All STM32F469xx devices embeds a Quad-SPI memory interface, which is a specialized communication interface targeting Single, Dual, Quad or Dual-flash SPI memories. It can work in direct mode through registers, external flash status register polling mode and memory mapped mode. Up to 256 Mbytes external Flash memory are mapped, supporting 8, 16 and 32-bit access. Code execution is supported.

The opcode and the frame format are fully programmable. Communication can be either in Single Data Rate or Dual Data Rate.

2.11 LCD-TFT controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 displays layers with dedicated FIFO (64x32-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 Input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events.

2.12 DSI Host (DSIHOST)

The DSI Host is a dedicated peripheral for interfacing with MIPI[®] DSI compliant displays. It includes a dedicated video interface internally connected to the LTDC and a generic APB interface that can be used to transmit information to the display.

These interfaces are as follows:

- LTDC interface:
 - Used to transmit information in Video Mode, in which the transfers from the host processor to the peripheral take the form of a real-time pixel stream (DPI).
 - Through a customized for mode, this interface can be used to transmit information in full bandwidth in the Adapted Command Mode (DBI).
- APB slave interface:
 - Allows the transmission of generic information in Command mode, and follows a proprietary register interface.
 - Can operate concurrently with either LTDC interface in either Video Mode or Adapted Command Mode.
- Video mode pattern generator:
 - Allows the transmission of horizontal/vertical color bar and D-PHY BER testing pattern without any kind of stimuli.