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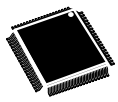
# STM32F722xx
# STM32F723xx

## ARM® Cortex®-M7 32b MCU+FPU, 462DMIPS, up to 512KB Flash /256+16+4KB RAM, USB OTG HS/FS, 18 TIMs, 3 ADCs, 21 com IF

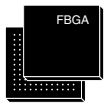
**Datasheet - production data**

## Features

- Core: ARM® 32-bit Cortex®-M7 CPU with FPU, adaptive real-time accelerator (ART Accelerator™) and L1-cache: 8 Kbytes of data cache and 8 Kbytes of instruction cache, allowing 0-wait state execution from embedded Flash memory and external memories, frequency up to 216 MHz, MPU, 462 DMIPS/2.14 DMIPS/MHz (Dhrystone 2.1) and DSP instructions.
- Memories
  - Up to 512 Kbytes of Flash memory with protection mechanisms (read and write protections, proprietary code readout protection (PCROP))
  - 528 bytes of OTP memory
  - SRAM: 256 Kbytes (including 64 Kbytes of data TCM RAM for critical real-time data) + 16 Kbytes of instruction TCM RAM (for critical real-time routines) + 4 Kbytes of backup SRAM (available in the lowest power modes)
  - Flexible external memory controller with up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPSDR SDRAM, NOR/NAND memories
- Dual mode Quad-SPI
- Clock, reset and supply management
  - 1.7 V to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - Dedicated USB power
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC (1% accuracy)
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Low-power
  - Sleep, Stop and Standby modes



LQFP64 (10 × 10 mm)
LQFP100 (14 × 14 mm)
LQFP144 (20 × 20 mm)
LQFP176 (24 x 24 mm)




UFBGA144 (7 x 7 mm)
UFBGA176 (10 x 10 mm)

WLCSP100
(0.4 mm pitch)

  - $V_{BAT}$ supply for RTC, 32×32 bit backup registers + 4 Kbytes of backup SRAM
- 3×12-bit, 2.4 MSPS ADC: up to 24 channels and 7.2 MSPS in triple interleaved mode
- 2×12-bit D/A converters
- Up to 18 timers: up to thirteen 16-bit (1x low-power 16-bit timer available in Stop mode) and two 32-bit timers, each with up to 4 IC/OC/PWMs or pulse counter and quadrature (incremental) encoder inputs. All 15 timers running up to 216 MHz. 2x watchdogs, SysTick timer
- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Debug mode
  - SWD & JTAG interfaces
  - Cortex®-M7 Trace Macrocell™
- Up to 140 I/O ports with interrupt capability
  - Up to 136 fast I/Os up to 108 MHz
  - Up to 138 5 V-tolerant I/Os
- Up to 21 communication interfaces
  - Up to 3× $I^2C$ interfaces (SMBus/PMBus)
  - Up to 4 USARTs/4 UARTs (27 Mbit/s, ISO7816 interface, LIN, IrDA, modem control)
  - Up to 5 SPIs (up to 54 Mbit/s), 3 with muxed simplex $I^2S$s for audio class accuracy via internal audio PLL or external clock
  - 2 x SAIs (serial audio interface)

  - 1 x CAN (2.0B active)
  - 2 x SDMMCs
- Advanced connectivity
  - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
  - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and on-chip Hi-speed PHY or ULPI depending on the part number
- True random number generator
- CRC calculation unit
- RTC: subsecond accuracy, hardware calendar
- 96-bit unique ID

**Table 1. Device summary**

| Reference | Part number |
|---|---|
| STM32F722xx | STM32F722IE, STM32F722ZE, STM32F722VE, STM32F722RE, STM32F722IC, STM32F722ZC, STM32F722VC, STM32F722RC |
| STM32F723xx | STM32F723IE, STM32F723ZE, STM32F723VE, STM32F723IC, STM32F723ZC |

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# 1 Description

The STM32F722xx and STM32F723xx devices are based on the high-performance ARM® Cortex®-M7 32-bit RISC core operating at up to 216 MHz frequency. The Cortex®-M7 core features a single floating point unit (SFPU) precision which supports ARM® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances the application security.

The STM32F722xx and STM32F723xx devices incorporate high-speed embedded memories with a Flash memory up to 512 Kbytes, 256 Kbytes of SRAM (including 64 Kbytes of data TCM RAM for critical real-time data), 16 Kbytes of instruction TCM RAM (for critical real-time routines), 4 Kbytes of backup SRAM available in the lowest power modes, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses, a 32-bit multi-AHB bus matrix and a multi layer AXI interconnect supporting internal and external memories access.

All the devices offer three 12-bit ADCs, two DACs, a low-power RTC, thirteen general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers, a true random number generator (RNG). They also feature standard and advanced communication interfaces.

- Up to three $I^2C$s
- Five SPIs, three $I^2S$s in half duplex mode. To achieve the audio class accuracy, the $I^2S$ peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus four UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI in the STM32F722xx devices and with the integrated HS PHY in the STM32F723xx devices)
- One CAN
- Two SAI serial audio interfaces
- Two SDMMC host interfaces

Advanced peripherals include two SDMMC interfaces, a flexible memory control (FMC) interface, a Quad-SPI Flash memory interface. Refer to *Table 2: STM32F722xx and STM32F723xx features and peripheral counts* for the list of peripherals available on each part number.

The STM32F722xx and STM32F723xx devices operate in the –40 to +105 °C temperature range from a 1.7 to 3.6 V power supply. Dedicated supply inputs for the USB (OTG_FS and OTG_HS) and the SDMMC2 (clock, command and 4-bit data) are available on all the packages except LQFP100 and LQFP64 for a greater power supply choice.

The supply voltage can drop to 1.7 V with the use of an external power supply supervisor (refer to *Section 2.15.2: Internal reset OFF*). A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F722xx and STM32F723xx devices offer devices in 7 packages ranging from 64 pins to 176 pins. The set of included peripherals changes with the device chosen.

These features make the STM32F722xx and STM32F723xx microcontrollers suitable for a wide range of applications:

- Motor drive and application control,
- Medical equipment,
- Industrial applications: PLC, inverters, circuit breakers,
- Printers, and scanners,
- Alarm systems, video intercom, and HVAC,
- Home audio appliances,
- Mobile applications, Internet of Things,
- Wearable devices: smartwatches.

*Figure 5* shows the general block diagram of the device family

**Table 2. STM32F722xx and STM32F723xx features and peripheral counts**

| Peripherals | | STM32F72xRx | | STM32F72xVx | | STM32F72xZx | | STM32F72xIx | |
|---|---|---|---|---|---|---|---|---|---|
| Flash memory in Kbytes | | 256 | 512 | 256 | 512 | 256 | 512 | 256 | 512 |
| SRAM in Kbytes | System | 256(176+16+64) | | | | | | | |
| | Instruction | 16 | | | | | | | |
| | Backup | 4 | | | | | | | |
| FMC memory controller | | No | | Yes(1) | | | | | |
| Quad-SPI | | Yes | | | | | | | |
| Timers | General-purpose | 10(2) | | | | | | | |
| | Advanced-control | 2 | | | | | | | |
| | Basic | 2 | | | | | | | |
| | Low-power | No | | 1 | | | | | |
| Random number generator | | Yes | | | | | | | |
| Communication interfaces | SPI / $I^2S$ | 3/3 (simplex)(3) | | 4/3 (simplex)(3) | | 5/3 (simplex)(3) | | | |
| | $I^2C$ | 3 | | | | | | | |
| | USART/UART | 4/2 | | 4/4 | | | | | |
| | USB OTG FS | Yes | | | | | | | |
| | USB OTG HS(4) | Yes | | | | | | | |
| | USB OTG PHY HS controller (USBPHYC) | No | | Yes(10) | | | | | |
| | CAN | 1 | | | | | | | |
| | SAI | 2 | | | | | | | |
| | SDMMC1 | Yes | | | | | | | |
| | SDMMC2 | No | | Yes(5)(6) | | | | | |
| GPIOs | | 50 | | 82 in STM32F722xx<br>79 in STM32F723xx | | 114 in STM32F722xx<br>112 in STM32F723xx | | 140 in STM32F722xx<br>138 in STM32F723xx | |
| 12-bit ADC | | 3 | | | | | | | |
| Number of channels | | 16 | | | | 24 | | | |
| 12-bit DAC<br>Number of channels | | Yes<br>2 | | | | | | | |
| Maximum CPU frequency | | 216 MHz(7) | | | | | | | |

**Table 2. STM32F722xx and STM32F723xx features and peripheral counts (continued)**

| Peripherals | STM32F72xRx | STM32F72xVx | STM32F72xZx | STM32F72xIx |
|---|---|---|---|---|
| Operating voltage | 1.7 to 3.6 V(8) | | | |
| Operating temperatures | Ambient temperatures: –40 to +85 °C /–40 to +105 °C | | | |
| | Junction temperature: –40 to + 125 °C | | | |
| Package | LQFP64(9) | LQFP100(9)<br>WLCSP100(10) | LQFP144<br>UFBGA144(10) | UFBGA176<br>LQFP176 |

1. For the LQFP100 package, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select.
2. On the STM32F723xx device packages, except the 176-pin ones, the TIM12 is not available, so there are 9 general-purpose timers.
3. The SPI1, SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the $I^2S$ audio mode.
4. USB OTG HS with the ULPI on the STM32F722xx devices and with integrated HS PHY on the STM32F723xx devices.
5. The SDMMC2 supports a dedicated power rail for clock, command and data 0..4 lines, feature available starting from 144 pin package.
6. The SDMMC2 is not available on the STM32F723Vx devices.
7. 216 MHz maximum frequency for - 40°C to + 85°C ambient temperature range (200 MHz maximum frequency for - 40°C to + 105°C ambient temperature range).
8. $V_{DD}/V_{DDA}$ minimum value of 1.7 V is obtained when the internal reset is OFF (refer to *Section 2.15.2: Internal reset OFF*).
9. Available only on the STM32F722xx devices.
10. Available only on the STM32F723xx devices.

## 1.1 Full compatibility throughout the family

The STM32F722xx devices are fully pin-to-pin, compatible with the STM32F7x5xx, STM32F7x6xx, STM32F7x7xx devices.

The STM32F722xx devices are fully pin-to-pin, compatible with the STM32F4xxxx devices, allowing the user to try different peripherals, and reaching higher performances (higher frequency) for a greater degree of freedom during the development cycle.

*Figure 1* and *Figure 2* give compatible board designs between the STM32F722xx and STM32F4xx families.

**Figure 1. Compatible board design for LQFP100 package**

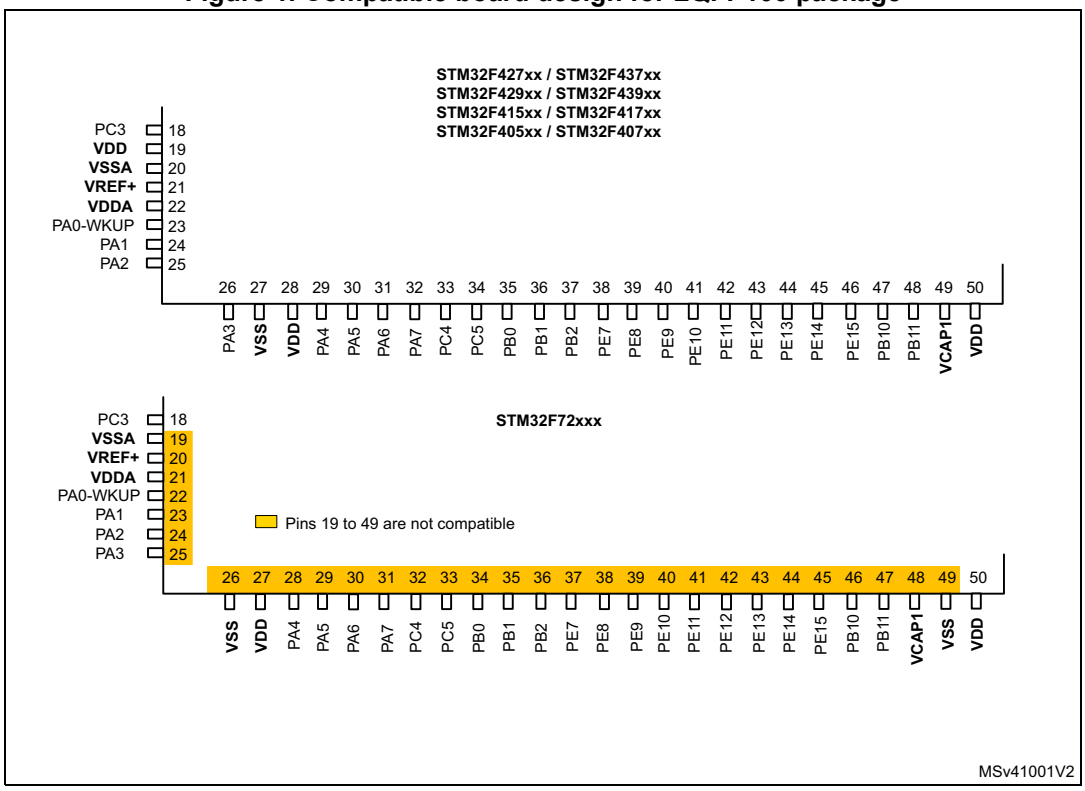
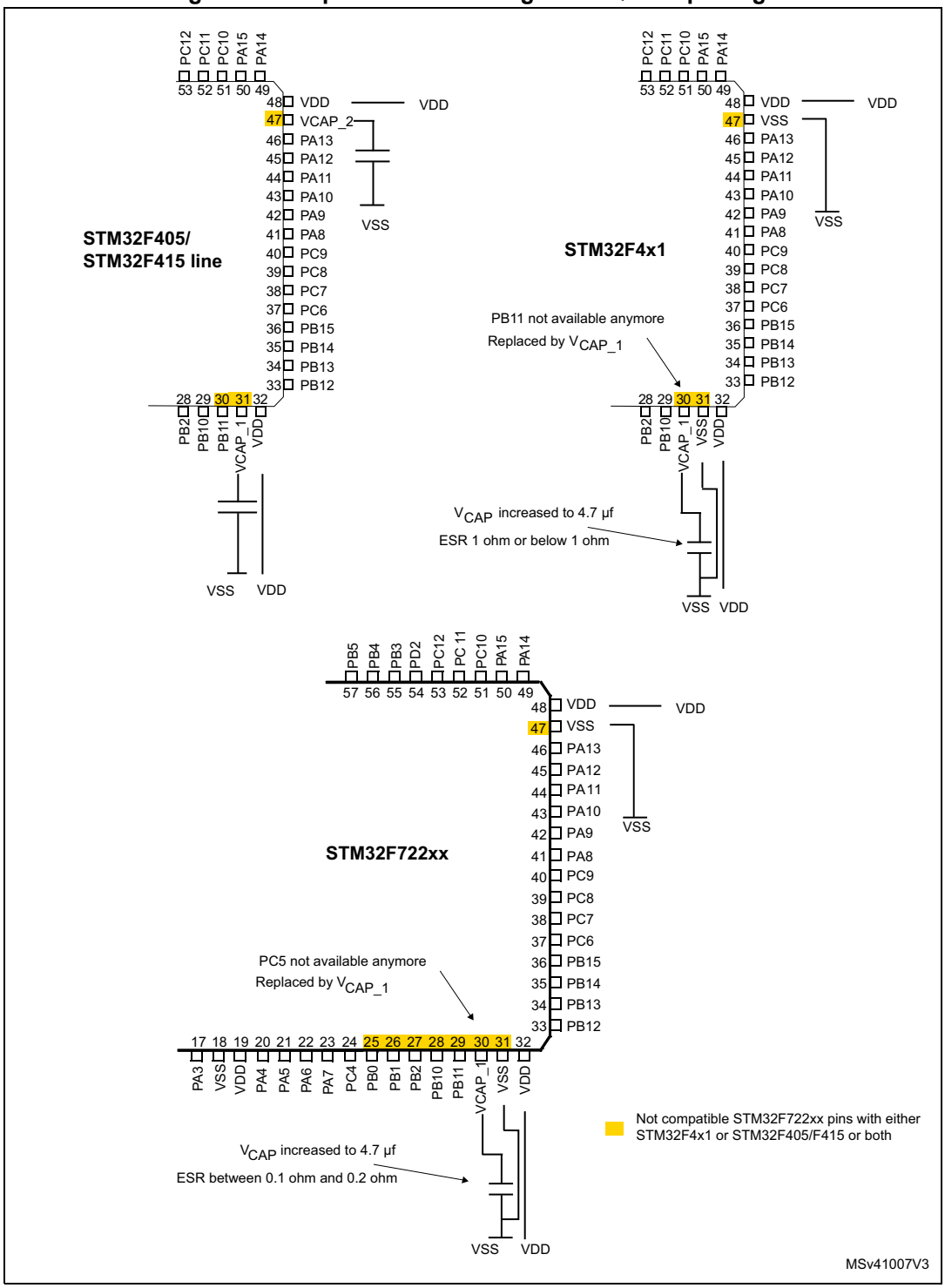


**Figure 2. Compatible board design for LQFP64 package**




The STM32F722xx LQFP144, UFBGA176 and LQFP176 packages are fully pin to pin compatible with the STM32F4xx devices.

## 1.2 STM32F723xx versus STM32F722xx LQFP144/LQFP176 packages:

**Figure 3. Compatible board design for LQFP144 package**

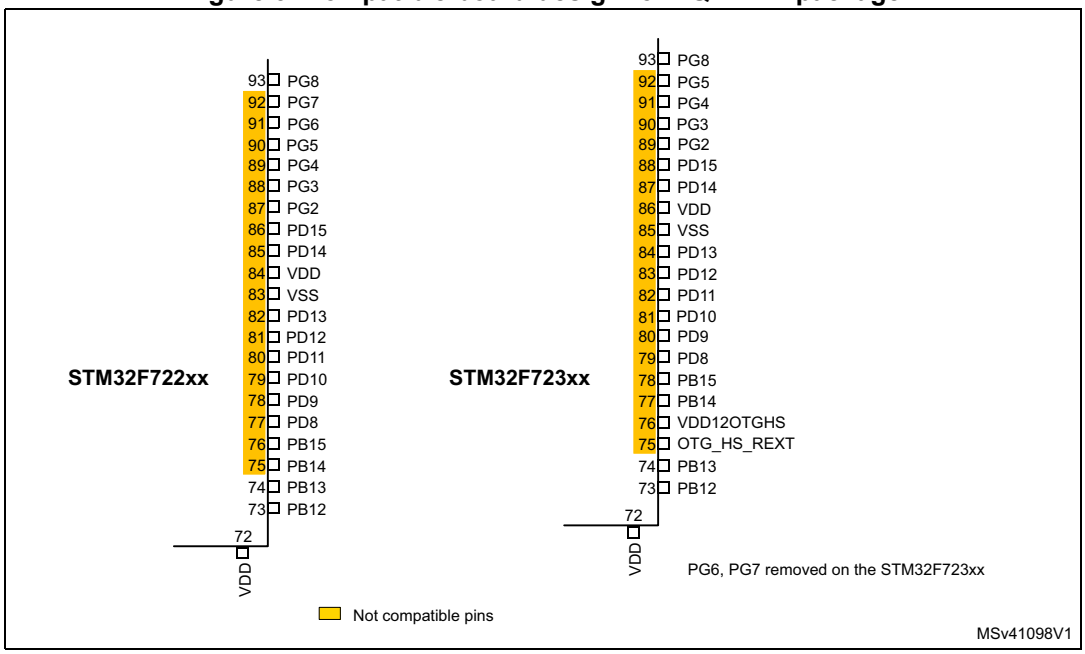



**Figure 4. Compatible board design for LQFP176 package**

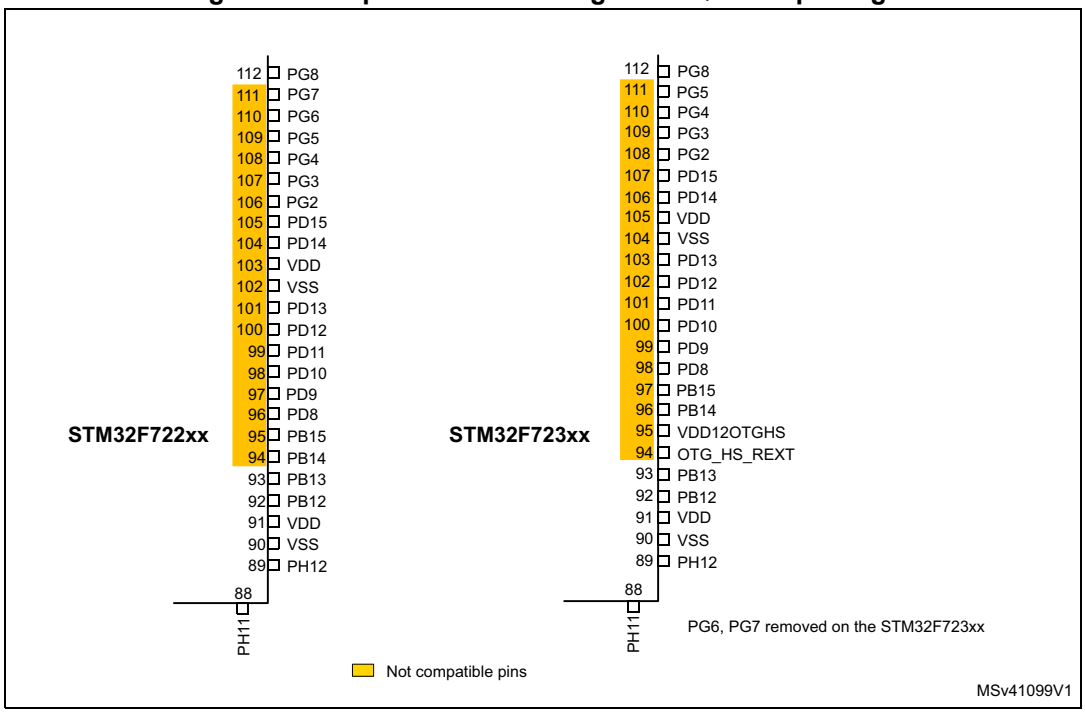
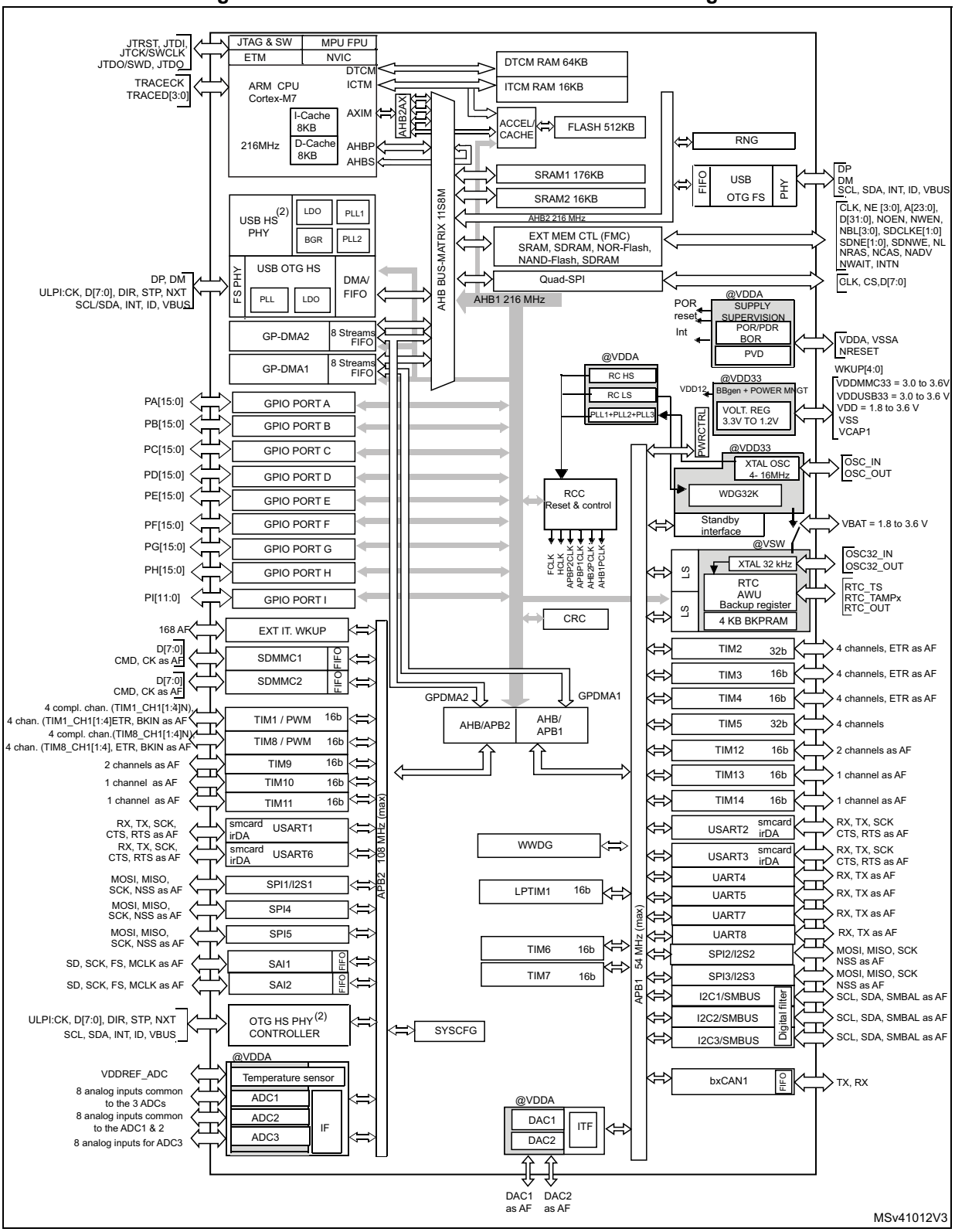


**Figure 5. STM32F722xx and STM32F723xx block diagram**




1. The timers connected to APB2 are clocked from TIMxCLK up to 216 MHz, while the timers connected to APB1 are clocked from TIMxCLK either up to 108 MHz or 216 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

2. Available only on the STM32F723xx devices.

# 2 Functional overview

## 2.1 ARM® Cortex®-M7 with FPU

The ARM® Cortex®-M7 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and low interrupt latency.

The Cortex®-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard caches (8 Kbytes of I-cache and 8 Kbytes of D-cache)
- 64-bit AXI4 interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The processor supports the following memory interfaces:

- Tightly Coupled Memory (TCM) interface.
- Harvard instruction and data caches and AXI master (AXIM) interface.
- Dedicated low-latency AHB-Lite peripheral (AHBP) interface.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

It supports single precision FPU (floating point unit), speeds up software development by using metalanguage development tools, while avoiding saturation.

*Figure 5* shows the general block diagram of the STM32F722xx and STM32F723xx family.

*Note: Cortex®-M7 with FPU core is binary compatible with the Cortex®-M4 core.*

## 2.2 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

## 2.3 Embedded Flash memory

The STM32F722xx and STM32F723xx devices embed a Flash memory of up to 512 Kbytes available for storing programs and data.

The flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
  - Level 0: no readout protection
  - Level 1: No access (read, erase, program) to the Flash memory or backup SRAM can be performed while the debug feature is connected or while booting from RAM or system memory bootloader
  - Level 2: debug/chip read protection disabled.
- Write protection (WRP): the protected area is protected against erasing and programming.
- Proprietary code readout protection (PCROP): Flash memory user sectors (0 to 7) can be protected against D-bus read accesses by using the proprietary readout protection (PCROP). The protected area is execute-only.

## 2.4 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

## 2.5 Embedded SRAM

All the devices feature:

- System SRAM up to 256 Kbytes:
  - SRAM1 on AHB bus Matrix: 176 Kbytes
  - SRAM2 on AHB bus Matrix: 16 Kbytes
  - DTCM-RAM on TCM interface (Tighly Coupled Memory interface): 64 Kbytes for critical real-time data.
- Instruction RAM (ITCM-RAM) 16 Kbytes:
  - It is mapped on TCM interface and reserved only for CPU Execution/Instruction useful for critical real-time routines.

The Data TCM RAM is accessible by the GP-DMAs and peripheral DMAs through the specific AHB slave of the CPU.The instruction TCM RAM is reserved only for CPU. It is accessed at CPU clock speed with 0 wait states.

- 4 Kbytes of backup SRAM

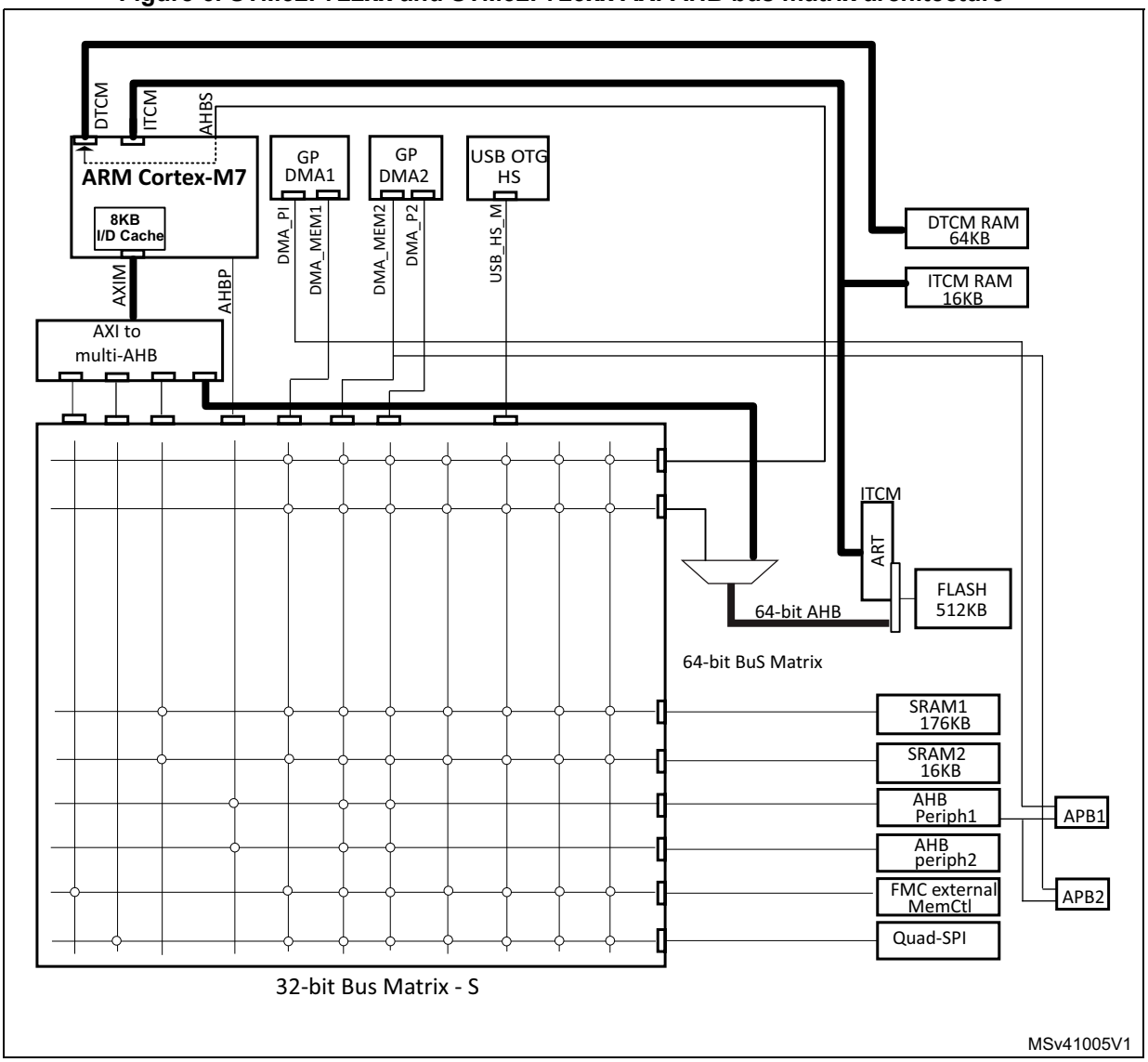
  This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or $V_{BAT}$ mode.

## 2.6 AXI-AHB bus matrix

The STM32F722xx and STM32F723xx system architecture is based on 2 sub-systems:

- An AXI to multi AHB bridge converting AXI4 protocol to AHB-Lite protocol:
  - 3x AXI to 32-bit AHB bridges connected to AHB bus matrix
  - 1x AXI to 64-bit AHB bridge connected to the embedded Flash memory
- A multi-AHB Bus-Matrix
  - The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, USB HS) and the slaves (Flash memory, RAM, FMC, Quad-SPI, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

**Figure 6. STM32F722xx and STM32F723xx AXI-AHB bus matrix architecture(1)**




1. The above figure has large wires for 64-bits bus and thin wires for 32-bits bus.

## 2.7 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support a circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. The configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and $I^2S$
- $I^2C$
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDMMC
- ADC
- SAI
- Quad-SPI

## 2.8 Flexible memory controller (FMC)

The Flexible memory controller (FMC) includes three memory controllers:

- The NOR/PSRAM memory controller
- The NAND/memory controller
- The Synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) controller

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR Flash memory/OneNAND Flash memory
  - PSRAM (4 memory banks)
  - NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) memories
- 8-, 16-, 32-bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is HCLK/2

### LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

## 2.9 Quad-SPI memory interface (QUADSPI)

All the devices embed a Quad-SPI memory interface, which is a specialized communication interface targetting Single, Dual or Quad-SPI Flash memories. It can work in:

- Direct mode through registers
- External Flash status register polling mode
- Memory mapped mode.

Up to 256 Mbytes of external Flash are memory mapped, supporting 8, 16 and 32-bit access. The code execution is supported.

The opcode and the frame format are fully programmable. The communication can be either in Single Data Rate or Dual Data Rate.

## 2.10 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 110 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M7 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with a minimum interrupt latency.

## 2.11 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 24 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 140 GPIOs in the STM32F722xx devices (138 GPIOs in the STM32F723xx devices) can be connected to the 16 external interrupt lines.

## 2.12 Clocks and startup

On reset the 16 MHz internal HSI RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 216 MHz. Similarly, a full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the two AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the two AHB buses is 216 MHz while the maximum frequency of the high-speed APB domains is 108 MHz. The maximum allowed frequency of the low-speed APB domain is 54 MHz.

The devices embed two dedicated PLLs (PLLI2S and PLLSAI) which allow to achieve audio class performance. In this case, the $I^2S$ and SAI master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

The STM32F723xx devices embed two PLLs inside the PHY HS controller: PLL1 and PLL2. The PLL1 allows to output 60 MHz used as an input for PLL2 which itself allows to generate the 480 Mbps in the USB OTG High Speed mode.

The PLL1 has as input HSE clock.