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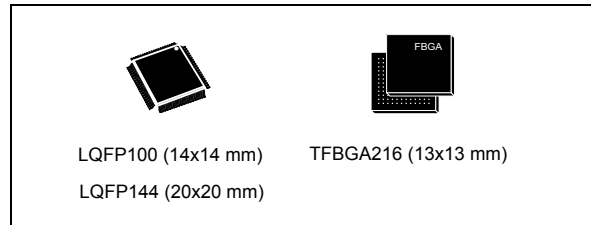


Arm[®]-based Cortex[®]-M7 32b MCU+FPU, 462DMIPS, 64KB Flash/ 320+16+ 4KB RAM, USB OTG HS/FS, 25 com IF, cam, LCD

Datasheet - production data

Features

- Core: Arm[®] 32-bit Cortex[®]-M7 CPU with FPU, adaptive real-time accelerator (ART Accelerator™) and L1-cache: 4-Kbyte data cache and 4-Kbyte instruction cache, allowing 0-wait state execution from embedded Flash memory and external memories, frequency up to 216 MHz, MPU, 462 DMIPS/2.14 DMIPS/MHz (Dhrystone 2.1), and DSP instructions.
- Memories
 - 64 Kbytes of Flash memory
 - 1024 bytes of OTP memory
 - SRAM: 320 Kbytes (including 64 Kbytes of data TCM RAM for critical real-time data) + 16 Kbytes of instruction TCM RAM (for critical real-time routines) + 4 Kbytes of backup SRAM (available in the lowest power modes)
 - Flexible external memory controller with up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPSDR SDRAM, NOR/NAND memories
- Dual mode Quad-SPI
- LCD parallel interface, 8080/6800 modes
- LCD-TFT controller up to XGA resolution with dedicated Chrom-ART Accelerator™ for enhanced graphic content creation (DMA2D)
- Clock, reset and supply management
 - 1.7 V to 3.6 V application supply and I/Os
 - POR, PDR, PVD and BOR
 - Dedicated USB power
 - 4-to-26 MHz crystal oscillator
 - Internal 16 MHz factory-trimmed RC (1% accuracy)
 - 32 kHz oscillator for RTC with calibration
 - Internal 32 kHz RC with calibration
- Low-power
 - Sleep, Stop and Standby modes



- V_{BAT} supply for RTC, 32×32-bit backup registers + 4 Kbytes of backup SRAM
- 3×12-bit, 2.4 MSPS ADC: up to 24 channels and 7.2 MSPS in triple interleaved mode
- 2×12-bit D/A converters
- Up to 18 timers: up to thirteen 16-bit (1x low-power 16-bit timer available in Stop mode) and two 32-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input. All 15 timers running up to 216 MHz. 2x watchdogs, SysTick timer
- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Debug mode
 - SWD & JTAG interfaces
 - Cortex[®]-M7 Trace Macrocell™
- Up to 168 I/O ports with interrupt capability
 - Up to 164 fast I/Os up to 108 MHz
 - Up to 166 5 V-tolerant I/Os
- Up to 25 communication interfaces
 - Up to 4× I²C interfaces (SMBus/PMBus)
 - Up to 4 USARTs/4 UARTs (27 Mbit/s, ISO7816 interface, LIN, IrDA, modem control)
 - Up to 6 SPIs (up to 50 Mbit/s), 3 with muxed simplex I²S for audio class accuracy via internal audio PLL or external clock
 - 2 x SAls (serial audio interface)
 - 2 × CANs (2.0B active) and SDMMC interface

- SPDIFRX interface
- HDMI-CEC
- Advanced connectivity
 - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
 - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
 - 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII
- 8- to 14-bit parallel camera interface up to 54 Mbyte/s
- Cryptographic acceleration: hardware acceleration for AES 128, 192, 256, triple DES, HASH (MD5, SHA-1, SHA-2), and HMAC
- True random number generator
- CRC calculation unit
- RTC: subsecond accuracy, hardware calendar
- 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM32F750x8	STM32F750V8, STM32F750Z8, STM32F750N8

Contents

1	Introduction	12
2	Description	13
	2.1 Full compatibility throughout the family	16
3	Functional overview	18
	3.1 Arm [®] Cortex [®] -M7 with FPU	18
	3.2 Memory protection unit	18
	3.3 Embedded Flash memory	19
	3.4 CRC (cyclic redundancy check) calculation unit	19
	3.5 Embedded SRAM	19
	3.6 AXI-AHB bus matrix	19
	3.7 DMA controller (DMA)	20
	3.8 Flexible memory controller (FMC)	21
	3.9 Quad-SPI memory interface (QUADSPI)	22
	3.10 LCD-TFT controller	22
	3.11 Chrom-ART Accelerator™ (DMA2D)	22
	3.12 Nested vectored interrupt controller (NVIC)	23
	3.13 External interrupt/event controller (EXTI)	23
	3.14 Clocks and startup	23
	3.15 Boot modes	24
	3.16 Power supply schemes	24
	3.17 Power supply supervisor	25
	3.17.1 Internal reset ON	25
	3.17.2 Internal reset OFF	26
	3.18 Voltage regulator	27
	3.18.1 Regulator ON	27
	3.18.2 Regulator OFF	28
	3.18.3 Regulator ON/OFF and internal reset ON/OFF availability	31
	3.19 Real-time clock (RTC), backup SRAM and backup registers	31
	3.20 Low-power modes	32
	3.21 V _{BAT} operation	33

3.22	Timers and watchdogs	33
3.22.1	Advanced-control timers (TIM1, TIM8)	35
3.22.2	General-purpose timers (TIMx)	35
3.22.3	Basic timers TIM6 and TIM7	36
3.22.4	Low-power timer (LPTIM1)	36
3.22.5	Independent watchdog	36
3.22.6	Window watchdog	36
3.22.7	SysTick timer	36
3.23	Inter-integrated circuit interface (I ² C)	37
3.24	Universal synchronous/asynchronous receiver transmitters (USART)	38
3.25	Serial peripheral interface (SPI)/inter-integrated sound interfaces (I2S)	39
3.26	Serial audio interface (SAI)	39
3.27	SPDIFRX Receiver Interface (SPDIFRX)	40
3.28	Audio PLL (PLLI2S)	40
3.29	Audio and LCD PLL(PLLSAI)	41
3.30	SD/SDIO/MMC card host interface (SDMMC)	41
3.31	Ethernet MAC interface with dedicated DMA and IEEE 1588 support	41
3.32	Controller area network (bxCAN)	42
3.33	Universal serial bus on-the-go full-speed (OTG_FS)	42
3.34	Universal serial bus on-the-go high-speed (OTG_HS)	42
3.35	High-definition multimedia interface (HDMI) - consumer electronics control (CEC)	43
3.36	Digital camera interface (DCMI)	43
3.37	Cryptographic acceleration	43
3.38	Random number generator (RNG)	44
3.39	General-purpose input/outputs (GPIOs)	44
3.40	Analog-to-digital converters (ADCs)	44
3.41	Temperature sensor	45
3.42	Digital-to-analog converter (DAC)	45
3.43	Serial wire JTAG debug port (SWJ-DP)	45
3.44	Embedded Trace Macrocell™	45
4	Pinouts and pin description	47
5	Memory mapping	82

6	Electrical characteristics	83
6.1	Parameter conditions	83
6.1.1	Minimum and maximum values	83
6.1.2	Typical values	83
6.1.3	Typical curves	83
6.1.4	Loading capacitor	83
6.1.5	Pin input voltage	83
6.1.6	Power supply scheme	84
6.1.7	Current consumption measurement	85
6.2	Absolute maximum ratings	85
6.3	Operating conditions	87
6.3.1	General operating conditions	87
6.3.2	VCAP1/VCAP2 external capacitor	89
6.3.3	Operating conditions at power-up / power-down (regulator ON)	90
6.3.4	Operating conditions at power-up / power-down (regulator OFF)	90
6.3.5	Reset and power control block characteristics	90
6.3.6	Over-drive switching characteristics	92
6.3.7	Supply current characteristics	92
6.3.8	Wakeup time from low-power modes	110
6.3.9	External clock source characteristics	111
6.3.10	Internal clock source characteristics	116
6.3.11	PLL characteristics	117
6.3.12	PLL spread spectrum clock generation (SSCG) characteristics	120
6.3.13	Memory characteristics	122
6.3.14	EMC characteristics	124
6.3.15	Absolute maximum ratings (electrical sensitivity)	126
6.3.16	I/O current injection characteristics	126
6.3.17	I/O port characteristics	127
6.3.18	NRST pin characteristics	133
6.3.19	TIM timer characteristics	134
6.3.20	RTC characteristics	134
6.3.21	12-bit ADC characteristics	134
6.3.22	Temperature sensor characteristics	140
6.3.23	V _{BAT} monitoring characteristics	140
6.3.24	Reference voltage	140
6.3.25	DAC electrical characteristics	141
6.3.26	Communications interfaces	143

6.3.27	FMC characteristics	158
6.3.28	Quad-SPI interface characteristics	178
6.3.29	Camera interface (DCMI) timing specifications	180
6.3.30	LCD-TFT controller (LTDC) characteristics	181
6.3.31	SD/SDIO MMC card host interface (SDMMC) characteristics	183
7	Package information	185
7.1	LQFP100, 14 x 14 mm low-profile quad flat package information	185
7.2	LQFP144, 20 x 20 mm low-profile quad flat package information	189
7.3	TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package information	192
7.4	Thermal characteristics	195
8	Ordering information	196
Appendix A	Recommendations when using internal reset OFF	197
A.1	Operating conditions	197
	Revision history	198

List of tables

Table 1.	Device summary	2
Table 2.	STM32F750x8 features and peripheral counts	14
Table 3.	Voltage regulator configuration mode versus device operating mode	28
Table 4.	Regulator ON/OFF and internal reset ON/OFF availability	31
Table 5.	Voltage regulator modes in Stop mode	32
Table 6.	Timer feature comparison	34
Table 7.	I2C implementation	37
Table 8.	USART implementation	38
Table 9.	Legend/abbreviations used in the pinout table	50
Table 10.	STM32F750x8 pin and ball definition	50
Table 11.	FMC pin definition	66
Table 12.	STM32F750x8 alternate function mapping	69
Table 13.	Voltage characteristics	85
Table 14.	Current characteristics	86
Table 15.	Thermal characteristics	86
Table 16.	General operating conditions	87
Table 17.	Limitations depending on the operating power supply range	89
Table 18.	VCAP1/VCAP2 operating conditions	89
Table 19.	Operating conditions at power-up / power-down (regulator ON)	90
Table 20.	Operating conditions at power-up / power-down (regulator OFF)	90
Table 21.	reset and power control block characteristics	91
Table 22.	Over-drive switching characteristics	92
Table 23.	Typical and maximum current consumption in Run mode, code with data processing running from ITCM RAM, regulator ON	93
Table 24.	Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART ON except prefetch / L1-cache ON) or SRAM on AXI (L1-cache ON), regulator ON	94
Table 25.	Typical and maximum current consumption in Run mode, code with data processing running from Flash memory or SRAM on AXI (L1-cache disabled), regulator ON	95
Table 26.	Typical and maximum current consumption in Run mode, code with data processing running from Flash memory on ITCM interface (ART disabled), regulator ON	96
Table 27.	Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART ON except prefetch / L1-cache ON) or SRAM on AXI (L1-cache ON), regulator OFF	97
Table 28.	Typical and maximum current consumption in Sleep mode, regulator ON	98
Table 29.	Typical and maximum current consumption in Sleep mode, regulator OFF	98
Table 30.	Typical and maximum current consumptions in Stop mode	99
Table 31.	Typical and maximum current consumptions in Standby mode	100
Table 32.	Typical and maximum current consumptions in V _{BAT} mode	101
Table 33.	Switching output I/O current consumption	105
Table 34.	Peripheral current consumption	107
Table 35.	Low-power mode wakeup timings	110
Table 36.	High-speed external user clock characteristics	111
Table 37.	Low-speed external user clock characteristics	112
Table 38.	HSE 4-26 MHz oscillator characteristics	113
Table 39.	LSE oscillator characteristics (f _{LSE} = 32.768 kHz)	114
Table 40.	HSI oscillator characteristics	116
Table 41.	LSI oscillator characteristics	117

Table 42.	Main PLL characteristics	117
Table 43.	PLLI2S characteristics	118
Table 44.	PLLI2M characteristics	119
Table 45.	SSCG parameters constraint	120
Table 46.	Flash memory characteristics	122
Table 47.	Flash memory programming	122
Table 48.	Flash memory programming with VPP	123
Table 49.	Flash memory endurance and data retention	124
Table 50.	EMS characteristics	124
Table 51.	EMI characteristics	125
Table 52.	ESD absolute maximum ratings	126
Table 53.	Electrical sensitivities	126
Table 54.	I/O current injection susceptibility	127
Table 55.	I/O static characteristics	127
Table 56.	Output voltage characteristics	130
Table 57.	I/O AC characteristics	131
Table 58.	NRST pin characteristics	133
Table 59.	TIMx characteristics	134
Table 60.	RTC characteristics	134
Table 61.	ADC characteristics	134
Table 62.	ADC static accuracy at $f_{ADC} = 18$ MHz	136
Table 63.	ADC static accuracy at $f_{ADC} = 30$ MHz	136
Table 64.	ADC static accuracy at $f_{ADC} = 36$ MHz	137
Table 65.	ADC dynamic accuracy at $f_{ADC} = 18$ MHz - limited test conditions	137
Table 66.	ADC dynamic accuracy at $f_{ADC} = 36$ MHz - limited test conditions	137
Table 67.	Temperature sensor characteristics	140
Table 68.	Temperature sensor calibration values	140
Table 69.	V_{BAT} monitoring characteristics	140
Table 70.	internal reference voltage	140
Table 71.	Internal reference voltage calibration values	141
Table 72.	DAC characteristics	141
Table 73.	Minimum I2CCLK frequency in all I2C modes	143
Table 74.	I2C analog filter characteristics	144
Table 75.	SPI dynamic characteristics	145
Table 76.	I ² S dynamic characteristics	148
Table 77.	SAI characteristics	150
Table 78.	USB OTG full speed startup time	152
Table 79.	USB OTG full speed DC electrical characteristics	152
Table 80.	USB OTG full speed electrical characteristics	153
Table 81.	USB HS DC electrical characteristics	153
Table 82.	USB HS clock timing parameters	154
Table 83.	Dynamic characteristics: USB ULPI	155
Table 84.	Dynamics characteristics: Ethernet MAC signals for SMI	156
Table 85.	Dynamics characteristics: Ethernet MAC signals for RMII	156
Table 86.	Dynamics characteristics: Ethernet MAC signals for MII	157
Table 87.	Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings	160
Table 88.	Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings	160
Table 89.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings	161
Table 90.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings	162
Table 91.	Asynchronous multiplexed PSRAM/NOR read timings	163
Table 92.	Asynchronous multiplexed PSRAM/NOR read-NWAIT timings	163
Table 93.	Asynchronous multiplexed PSRAM/NOR write timings	164

Table 94.	Asynchronous multiplexed PSRAM/NOR write-NWAIT timings	165
Table 95.	Synchronous multiplexed NOR/PSRAM read timings	167
Table 96.	Synchronous multiplexed PSRAM write timings	169
Table 97.	Synchronous non-multiplexed NOR/PSRAM read timings	170
Table 98.	Synchronous non-multiplexed PSRAM write timings	172
Table 99.	Switching characteristics for NAND Flash read cycles	174
Table 100.	Switching characteristics for NAND Flash write cycles	174
Table 101.	SDRAM read timings	176
Table 102.	LPSDR SDRAM read timings	176
Table 103.	SDRAM write timings	177
Table 104.	LPSDR SDRAM write timings	178
Table 105.	Quad-SPI characteristics in SDR mode	178
Table 106.	Quad-SPI characteristics in DDR mode	179
Table 107.	DCMI characteristics	180
Table 108.	LTDC characteristics	181
Table 109.	Dynamic characteristics: SD / MMC characteristics, VDD=2.7V to 3.6V	184
Table 110.	Dynamic characteristics: eMMC characteristics, VDD=1.71V to 1.9V	184
Table 111.	LQPF100, 14 x 14 mm 100-pin low-profile quad flat package mechanical data	186
Table 112.	LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data	189
Table 113.	TFBGA216, 13 x 13 x 0.8 mm thin fine-pitch ball grid array package mechanical data	192
Table 114.	TFBGA216 recommended PCB design rules (0.8 mm pitch BGA).	193
Table 115.	Package thermal characteristics	195
Table 116.	Ordering information scheme	196
Table 117.	Limitations depending on the operating power supply range	197
Table 118.	Document revision history	198

List of figures

Figure 1.	Compatible board design for LQFP100 package	16
Figure 2.	STM32F750x8 block diagram	17
Figure 3.	STM32F750x8 AXI-AHB bus matrix architecture	20
Figure 4.	VDDUSB connected to VDD power supply	25
Figure 5.	VDDUSB connected to external power supply	25
Figure 6.	Power supply supervisor interconnection with internal reset OFF	26
Figure 7.	PDR_ON control with internal reset OFF	27
Figure 8.	Regulator OFF	29
Figure 9.	Startup in regulator OFF: slow V_{DD} slope - power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization	30
Figure 10.	Startup in regulator OFF mode: fast V_{DD} slope - power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization	30
Figure 11.	STM32F750V8 LQFP100 pinout	47
Figure 12.	STM32F750Z8 LQFP144 pinout	48
Figure 13.	STM32F750N8 TFBGA216 ballout	49
Figure 14.	Pin loading conditions	83
Figure 15.	Pin input voltage	83
Figure 16.	Power supply scheme	84
Figure 17.	Current consumption measurement scheme	85
Figure 18.	External capacitor C_{EXT}	89
Figure 19.	Typical V_{BAT} current consumption (RTC ON/BKP SRAM OFF and LSE in low drive mode)	102
Figure 20.	Typical V_{BAT} current consumption (RTC ON/BKP SRAM OFF and LSE in medium low drive mode)	102
Figure 21.	Typical V_{BAT} current consumption (RTC ON/BKP SRAM OFF and LSE in medium high drive mode)	103
Figure 22.	Typical V_{BAT} current consumption (RTC ON/BKP SRAM OFF and LSE in high drive mode)	103
Figure 23.	Typical V_{BAT} current consumption (RTC ON/BKP SRAM OFF and LSE in high medium drive mode)	104
Figure 24.	High-speed external clock source AC timing diagram	112
Figure 25.	Low-speed external clock source AC timing diagram	113
Figure 26.	Typical application with an 8 MHz crystal	114
Figure 27.	Typical application with a 32.768 kHz crystal	115
Figure 28.	HSI deviation versus temperature	116
Figure 29.	LSI deviation versus temperature	117
Figure 30.	PLL output clock waveforms in center spread mode	121
Figure 31.	PLL output clock waveforms in down spread mode	122
Figure 32.	FT I/O input characteristics	129
Figure 33.	I/O AC characteristics definition	132
Figure 34.	Recommended NRST pin protection	133
Figure 35.	ADC accuracy characteristics	138
Figure 36.	Typical connection diagram using the ADC	138
Figure 37.	Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})	139
Figure 38.	Power supply and reference decoupling (V_{REF+} connected to V_{DDA})	139
Figure 39.	12-bit buffered /non-buffered DAC	143
Figure 40.	SPI timing diagram - slave mode and CPHA = 0	146
Figure 41.	SPI timing diagram - slave mode and CPHA = 1	147

Figure 42.	SPI timing diagram - master mode	147
Figure 43.	I ² S slave timing diagram (Philips protocol) ⁽¹⁾	149
Figure 44.	I ² S master timing diagram (Philips protocol) ⁽¹⁾	149
Figure 45.	SAI master timing waveforms	151
Figure 46.	SAI slave timing waveforms	151
Figure 47.	USB OTG full speed timings: definition of data signal rise and fall time	153
Figure 48.	ULPI timing diagram	154
Figure 49.	Ethernet SMI timing diagram	155
Figure 50.	Ethernet RMII timing diagram	156
Figure 51.	Ethernet MII timing diagram	157
Figure 52.	Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms	159
Figure 53.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms	161
Figure 54.	Asynchronous multiplexed PSRAM/NOR read waveforms	162
Figure 55.	Asynchronous multiplexed PSRAM/NOR write waveforms	164
Figure 56.	Synchronous multiplexed NOR/PSRAM read timings	166
Figure 57.	Synchronous multiplexed PSRAM write timings	168
Figure 58.	Synchronous non-multiplexed NOR/PSRAM read timings	170
Figure 59.	Synchronous non-multiplexed PSRAM write timings	171
Figure 60.	NAND controller waveforms for read access	173
Figure 61.	NAND controller waveforms for write access	173
Figure 62.	NAND controller waveforms for common memory read access	173
Figure 63.	NAND controller waveforms for common memory write access	174
Figure 64.	SDRAM read access waveforms (CL = 1)	175
Figure 65.	SDRAM write access waveforms	177
Figure 66.	Quad-SPI timing diagram - SDR mode	180
Figure 67.	Quad-SPI timing diagram - DDR mode	180
Figure 68.	DCMI timing diagram	181
Figure 69.	LCD-TFT horizontal timing diagram	182
Figure 70.	LCD-TFT vertical timing diagram	182
Figure 71.	SDIO high-speed mode	183
Figure 72.	SD default mode	183
Figure 73.	LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline	185
Figure 74.	LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package recommended footprint	187
Figure 75.	LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package top view example	188
Figure 76.	LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline	189
Figure 77.	LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package recommended footprint	190
Figure 78.	LQFP144, 20 x 20mm, 144-pin low-profile quad flat package top view example	191
Figure 79.	TFBGA216, 13 x 13 x 0.8 mm thin fine-pitch ball grid array package outline	192
Figure 80.	TFBGA216, 13 x 13 x 0.8 mm thin fine-pitch ball grid array package recommended footprint	193
Figure 81.	TFBGA216, 13 x 13 x 0.8 mm thin fine-pitch ball grid array package top view example	194

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F750x8 microcontrollers.

This document should be read in conjunction with the *STM32F75xxx and STM32F74xxx advanced Arm[®]-based 32-bit MCUs* reference manual (RM0385). The reference manual is available from the STMicroelectronics website www.st.com.

For information on the Arm^{®(a)} Cortex[®]-M7 core, refer to the Cortex[®]-M7 technical reference manual available from the <http://www.arm.com> website.



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2 Description

The STM32F750x8 devices are based on the high-performance Arm® Cortex®-M7 32-bit RISC core operating at up to 216 MHz frequency. The Cortex®-M7 core features a single floating point unit (SFPU) precision which supports all Arm® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances the application security.

The STM32F750x8 devices incorporate high-speed embedded memories with a Flash memory of 64 Kbytes, 320 Kbytes of SRAM (including 64 Kbytes of Data TCM RAM for critical real-time data), 16 Kbytes of instruction TCM RAM (for critical real-time routines), 4 Kbytes of backup SRAM available in the lowest power modes, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses, a 32-bit multi-AHB bus matrix and a multi layer AXI interconnect supporting internal and external memories access.

All the devices offer three 12-bit ADCs, two DACs, a low-power RTC, thirteen general-purpose 16-bit timers including two PWM timers for motor control and one low-power timer available in Stop mode, two general-purpose 32-bit timers, a true random number generator (RNG), and a cryptographic acceleration cell. They also feature standard and advanced communication interfaces.

- Up to four I²Cs
- Six SPIs, three I²Ss in duplex mode. To achieve the audio class accuracy, the I²S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus four UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI),
- Two CANs
- Two SAI serial audio interfaces
- An SDMMC host interface
- Ethernet and camera interfaces
- LCD-TFT display controller
- Chrom-ART Accelerator™
- SPDIFRX interface
- HDMI-CEC

Advanced peripherals include an SDMMC interface, a flexible memory control (FMC) interface, a Quad-SPI Flash memory interface, a camera interface for CMOS sensors and a cryptographic acceleration cell.

The STM32F750x8 devices operate in the –40 to +105 °C temperature range from a 1.7 to 3.6 V power supply. A dedicated supply input for USB (OTG_FS and OTG_HS) is available on all the packages except LQFP100 for a greater power supply choice.

The supply voltage can drop to 1.7 V with the use of an external power supply supervisor. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F750x8 devices offer devices in 3 packages ranging from 100 pins to 216 pins. The set of included peripherals changes with the device chosen.

These features make the STM32F750x8 microcontrollers suitable for a wide range of applications.

- Motor drive and application control,
- Medical equipment,
- Industrial applications: PLC, inverters, circuit breakers,
- Printers, and scanners,
- Alarm systems, video intercom, and HVAC,
- Home audio appliances,
- Mobile applications, Internet of Things,
- Wearable devices: smartwatches.

Table 2. STM32F750x8 features and peripheral counts

Peripherals		STM32F750V8	STM32F750Z8	STM32F750N8
Flash memory in Kbytes		64		
SRAM in Kbytes	System	320(240+16+64)		
	Instruction	16		
	Backup	4		
FMC memory controller		Yes ⁽¹⁾		
Ethernet		Yes		
Timers	General-purpose	10		
	Advanced-control	2		
	Basic	2		
	Low-power	1		
Random number generator		Yes		
Communication interfaces	SPI / I ² S	4/3 (simplex) ⁽²⁾	6/3 (simplex) ⁽²⁾	
	I ² C	4		
	USART/UART	4/4		
	USB OTG FS	Yes		
	USB OTG HS	Yes		
	CAN	2		
	SAI	2		
	SPDIFRX	4 inputs		
	SDMMC	Yes		
Camera interface		Yes		
LCD-TFT		Yes		
Chrom-ART Accelerator™ (DMA2D)		Yes		
Cryptography		Yes		
GPIOs		82	114	168

Table 2. STM32F750x8 features and peripheral counts (continued)

Peripherals	STM32F750V8	STM32F750Z8	STM32F750N8
12-bit ADC	3		
Number of channels	16	24	
12-bit DAC	Yes		
Number of channels	2		
Maximum CPU frequency	216 MHz ⁽³⁾		
Operating voltage	1.7 to 3.6 V ⁽⁴⁾		
Operating temperatures	Ambient temperatures: -40 to +85 °C / -40 to +105 °C		
	Junction temperature: -40 to + 125 °C		
Package	LQFP100	LQFP144	TFBGA216

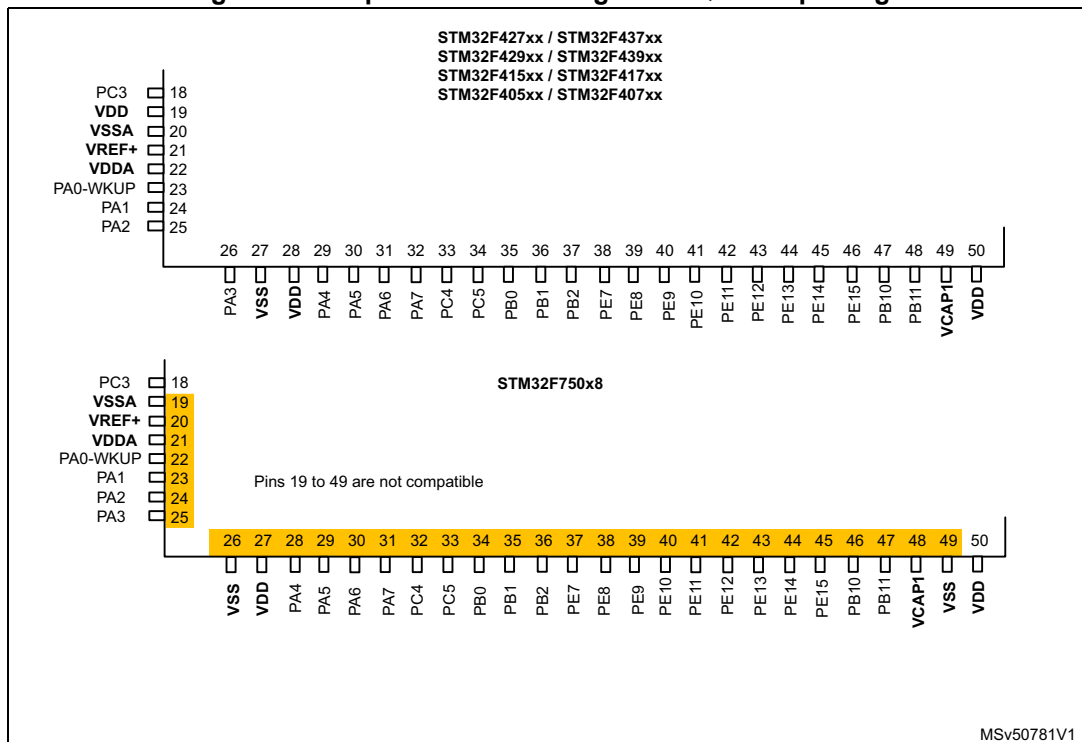
1. For the LQFP100 package, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select.
2. The SPI1, SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. 216 MHz maximum frequency for -40°C to + 85°C ambient temperature range (200 MHz maximum frequency for -40°C to + 105°C ambient temperature range).
4. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the internal reset is OFF (refer to [Section 3.17.2: Internal reset OFF](#)).

2.1 Full compatibility throughout the family

The STM32F750x8 devices are fully pin-to-pin, compatible with the STM32F4xxxx devices, allowing the user to try different peripherals, and reaching higher performances (higher frequency) for a greater degree of freedom during the development cycle.

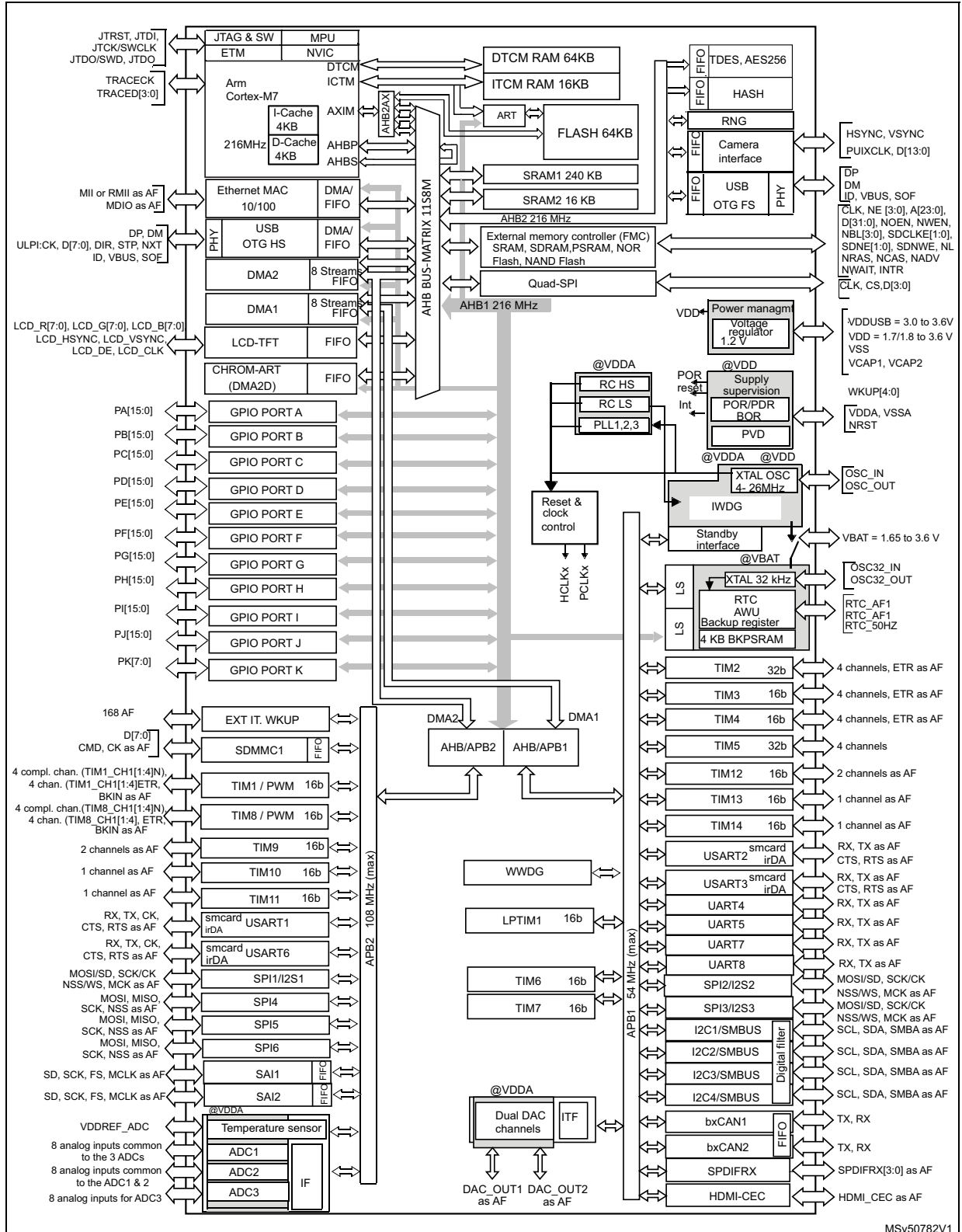
Figure 1 give compatible board designs between the STM32F4xx families.

Figure 1. Compatible board design for LQFP100 package



The STM32F750x8 LQFP144 and TFBGA216 packages are fully pin to pin compatible with STM32F4xxxx devices.

Figure 2. STM32F750x8 block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 216 MHz, while the timers connected to APB1 are clocked from TIMxCLK either up to 108 MHz or 216 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

3 Functional overview

3.1 Arm[®] Cortex[®]-M7 with FPU

The Arm[®] Cortex[®]-M7 with FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and a low-power consumption, while delivering an outstanding computational performance and low interrupt latency.

The Cortex[®]-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard caches (4 Kbytes of I-cache and 4 Kbytes of D-cache)
- 64-bit AXI4 interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The processor supports the following memory interfaces:

- Tightly Coupled Memory (TCM) interface.
- Harvard instruction and data caches and AXI master (AXIM) interface.
- Dedicated low-latency AHB-Lite peripheral (AHBP) interface.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up the software development by using metalanguage development tools, while avoiding saturation.

Figure 2 shows the general block diagram of the STM32F750x8 devices.

Note: Cortex[®]-M7 with FPU core is binary compatible with the Cortex[®]-M4 core.

3.2 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.3 Embedded Flash memory

The STM32F750x8 devices embed a Flash memory of 64 Kbytes available for storing programs and data.

3.4 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify the data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean of verifying the Flash memory integrity. The CRC calculation unit helps to compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.5 Embedded SRAM

All the devices features:

- System SRAM up to 320 Kbytes:
 - SRAM1 on AHB bus Matrix: 240 Kbytes
 - SRAM2 on AHB bus Matrix: 16 Kbytes
 - DTCM-RAM on TCM interface (Tightly Coupled Memory interface): 64 Kbytes for critical real-time data.
- Instruction RAM (ITCM-RAM) 16 Kbytes:
 - It is mapped on TCM interface and reserved only for CPU Execution/Instruction useful for critical real-time routines.

The Data TCM RAM is accessible by the GP-DMA's and peripherals DMA's through specific AHB slave of the CPU. The TCM RAM instruction is reserved only for CPU. It is accessed at CPU clock speed with 0-wait states.

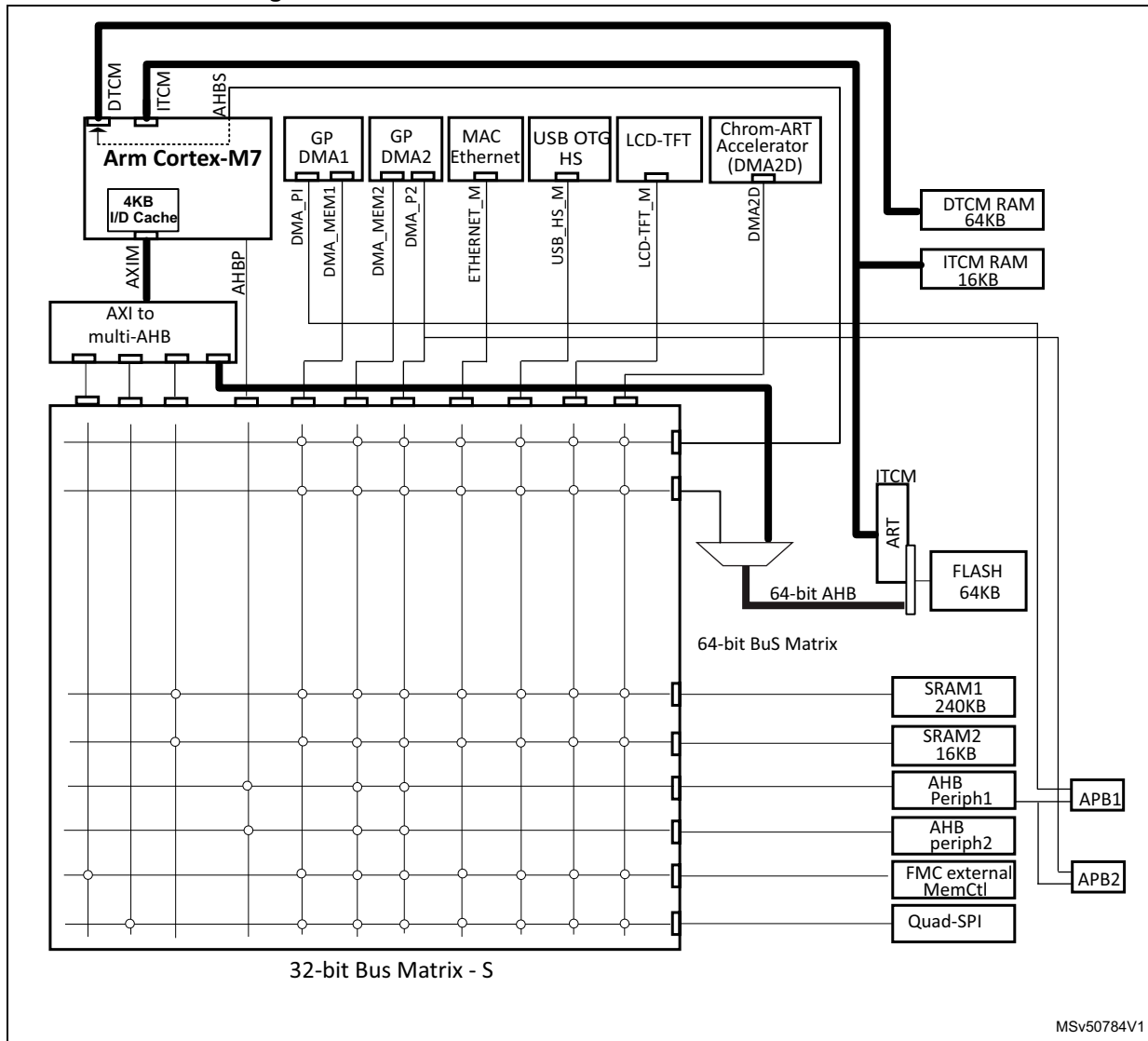
- 4 Kbytes of backup SRAM
 - This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or VBAT mode.

3.6 AXI-AHB bus matrix

The STM32F750x8 system architecture is based on 2 sub-systems:

- An AXI to multi AHB bridge converting AXI4 protocol to AHB-Lite protocol:
 - 3x AXI to 32-bit AHB bridges connected to AHB bus matrix
 - 1x AXI to 64-bit AHB bridge connected to the embedded flash
- A multi-AHB Bus-Matrix:
 - The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMA's, Ethernet, USB HS, LCD-TFT, and DMA2D) and the slaves (Flash memory, RAM, FMC, Quad-SPI, AHB and APB peripherals) and ensures a seamless and an efficient operation even when several high-speed peripherals work simultaneously.

Figure 3. STM32F750x8 AXI-AHB bus matrix architecture



1. The above figure has large wires for 64-bits bus and thin wires for 32-bits bus.

3.7 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I²S
- I²C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDMMC
- Cryptographic acceleration
- Camera interface (DCMI)
- ADC
- SAI
- SPDIFRX
- Quad-SPI
- HDMI-CEC

3.8 Flexible memory controller (FMC)

The Flexible memory controller (FMC) includes three memory controllers:

- The NOR/PSRAM memory controller
- The NAND/memory controller
- The Synchronous DRAM (SDRAM/Mobile LPDDR SDRAM) controller

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
 - Static random access memory (SRAM)
 - NOR Flash memory/OneNAND Flash memory
 - PSRAM (4 memory banks)
 - NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPDDR SDRAM) memories
- 8-, 16-, 32-bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The Maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is HCLK/2.

LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to

specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

3.9 Quad-SPI memory interface (QUADSPI)

All devices embed a Quad-SPI memory interface, which is a specialized communication interface targeting Single, Dual or Quad-SPI Flash memories. It can work in:

- Direct mode through registers.
- External flash status register polling mode.
- Memory mapped mode.

Up to 256 Mbytes external flash are memory mapped, supporting 8, 16 and 32-bit access. Code execution is supported.

The opcode and the frame format are fully programmable. Communication can be either in Single Data Rate or Dual Data Rate.

3.10 LCD-TFT controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 displays layers with dedicated FIFO (64x32-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 Input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events.

3.11 Chrom-ART Accelerator™ (DMA2D)

The Chrom-Art Accelerator™ (DMA2D) is a graphic accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion.

Various image format coding are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

3.12 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 97 maskable interrupt channels plus the 16 interrupt lines of the Cortex[®]-M7 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.13 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 24 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 168 GPIOs can be connected to the 16 external interrupt lines.

3.14 Clocks and startup

On reset the 16 MHz internal HSI RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 216 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the two AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the two AHB buses is 216 MHz while the maximum frequency of the high-speed APB domains is 108 MHz. The maximum allowed frequency of the low-speed APB domain is 54 MHz.

The devices embed two dedicated PLL (PLL12S and PLLSAI) which allow to achieve audio class performance. In this case, the I²S and SAI master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

3.15 Boot modes

At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDx option bytes, allowing to program any boot memory address from 0x0000 0000 to 0x3FFF FFFF which includes:

- All Flash address space mapped on ITCM or AXIM interface
- All RAM address space: ITCM, DTCM RAMs and SRAMs mapped on AXIM interface
- The System memory bootloader

The boot loader is located in system memory. It is used to reprogram the Flash memory through a serial interface.

3.16 Power supply schemes

- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
- V_{DD} = 1.7 to 3.6 V external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins.
- V_{SSA} , V_{DDA} = 1.7 to 3.6 V: external analog power supplies for ADC, DAC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.

Note: V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the internal reset is OFF (refer to [Section 3.17.2: Internal reset OFF](#)). Refer to [Table 3: Voltage regulator configuration mode versus device operating mode](#) to identify the packages supporting this option.

- V_{DDUSB} can be connected either to V_{DD} or an external independent power supply (3.0 to 3.6V) for USB transceivers (refer to [Figure 4](#) and [Figure 5](#)). For example, when device is powered at 1.8V, an independent power supply 3.3V can be connected to V_{DDUSB} . When the V_{DDUSB} is connected to a separated power supply, it is independent from V_{DD} or V_{DDA} but it must be the last supply to be provided and the first to disappear. The following conditions V_{DDUSB} must be respected:
 - During power-on phase ($V_{DD} < V_{DD_MIN}$), V_{DDUSB} should be always lower than V_{DD}
 - During power-down phase ($V_{DD} < V_{DD_MIN}$), V_{DDUSB} should be always lower than V_{DD}
 - V_{DDSUB} rising and falling time rate specifications must be respected (see [Table 19](#) and [Table 20](#))
 - In operating mode phase, V_{DDUSB} could be lower or higher than V_{DD} :
 - If USB (USB OTG_HS/OTG_FS) is used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DDUSB_MIN} and V_{DDUSB_MAX} .
 - The V_{DDUSB} supply both USB transceiver (USB OTG_HS and USB OTG_FS). If only one USB transceiver is used in the application, the GPIOs associated to the other USB transceiver are still supplied by V_{DDUSB} .
 - If USB (USB OTG_HS/OTG_FS) is not used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DD_MIN} and V_{DD_MAX} .

Figure 4. V_{DDUSB} connected to V_{DD} power supply

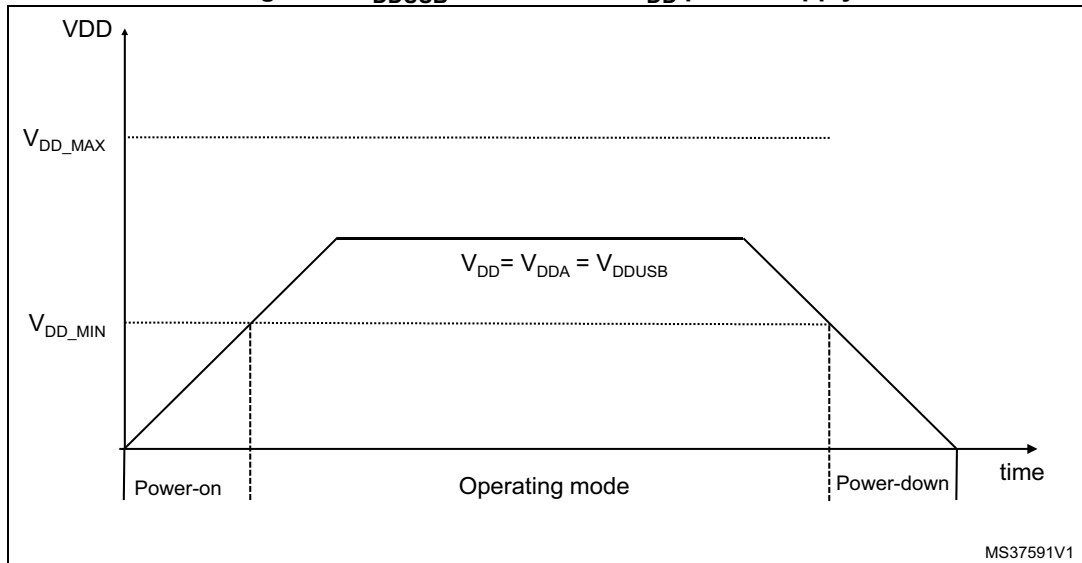
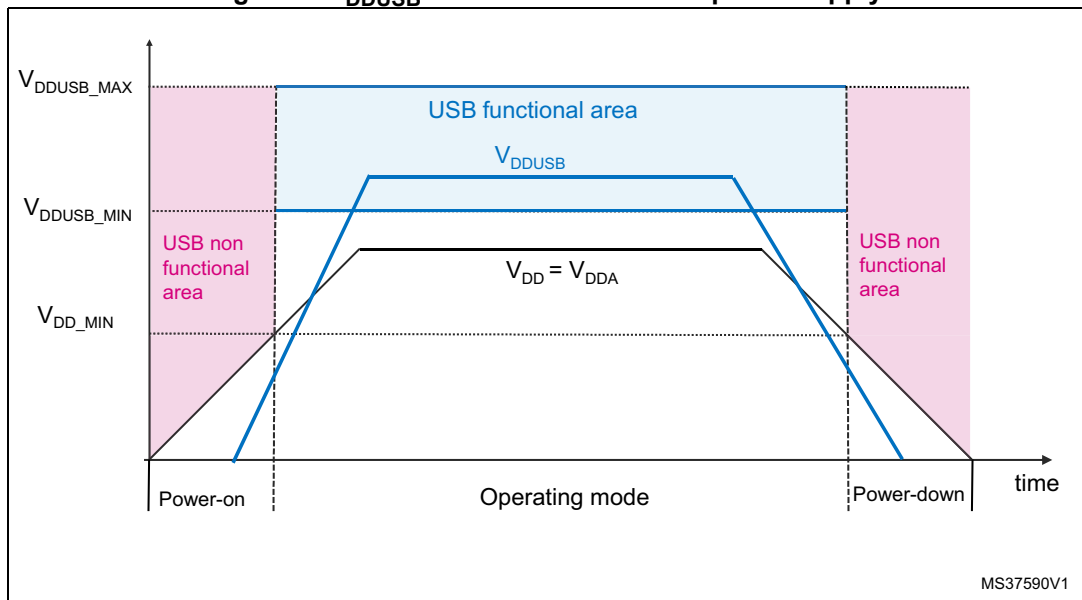


Figure 5. V_{DDUSB} connected to external power supply



3.17 Power supply supervisor

3.17.1 Internal reset ON

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On the other packages, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is