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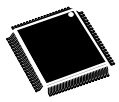
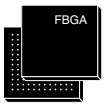
STM32F777xx STM32F778Ax STM32F779xx

ARM®-based Cortex®-M7 32b MCU+FPU, 462DMIPS, up to 2MB Flash/512+16+4KB RAM, crypto, USB OTG HS/FS, ethernet, 18 TIMs, 3 ADCs, 28 com itf, cam, LCD, DSI

Datasheet - production data

Features

- Core: ARM® 32-bit Cortex®-M7 CPU with DPFPU, ART Accelerator™ and L1-cache: 16 Kbytes I/D cache, allowing 0-wait state execution from embedded Flash and external memories, up to 216 MHz, MPU, 462 DMIPS/2.14 DMIPS/MHz (Dhrystone 2.1), and DSP instructions.
- Memories
  - Up to 2 Mbytes of Flash memory organized into two banks allowing read-while-write
  - SRAM: 512 Kbytes (including 128 Kbytes of data TCM RAM for critical real-time data) + 16 Kbytes of instruction TCM RAM (for critical real-time routines) + 4 Kbytes of backup SRAM
  - Flexible external memory controller with up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPSDR SDRAM, NOR/NAND memories
- Dual mode Quad-SPI
- Graphics
  - Chrom-ART Accelerator™ (DMA2D), graphical hardware accelerator enabling enhanced graphical user interface
  - Hardware JPEG codec
  - LCD-TFT controller supporting up to XGA resolution
  - MIPI® DSI host controller supporting up to 720p 30 Hz resolution
- Clock, reset and supply management
  - 1.7 V to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - Dedicated USB power
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC (1% accuracy)
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration

LQFP100 (14 × 14 mm)
LQFP144 (20 × 20 mm)
LQFP176 (24 × 24 mm)
LQFP208 (28 x 28 mm)

UFBGA176 (10 x 10 mm)
TFBGA216 (13 x 13 mm)

WLCSP180 (0.4 mm pitch)

- Low-power
  - Sleep, Stop and Standby modes
  - V_{BAT} supply for RTC, 32×32 bit backup registers + 4 Kbytes backup SRAM
- 3×12-bit, 2.4 MSPS ADC: up to 24 channels
- Digital filters for sigma delta modulator (DFSDM), 8 channels / 4 filters
- 2×12-bit D/A converters
- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Up to 18 timers: up to thirteen 16-bit (1x low-power 16-bit timer available in Stop mode) and two 32-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input. All 15 timers running up to 216 MHz. 2x watchdogs, SysTick timer
- Debug mode
  - SWD & JTAG interfaces
  - Cortex®-M7 Trace Macrocell™
- Up to 168 I/O ports with interrupt capability
  - Up to 164 fast I/Os up to 108 MHz
  - Up to 166 5 V-tolerant I/Os

- Up to 28 communication interfaces
  - Up to 4 I^2C interfaces (SMBus/PMBus)
  - Up to 4 USARTs/4 UARTs (12.5 Mbit/s, ISO7816 interface, LIN, IrDA, modem control)
  - Up to 6 SPIs (up to 54 Mbit/s), 3 with muxed simplex I^2S for audio
  - 2 x SAIs (serial audio interface)
  - 3 × CANs (2.0B Active) and 2x SDMMCs
  - SPDIFRX interface
  - HDMI-CEC
  - MDIO slave interface
- Advanced connectivity
  - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
  - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
  - 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII
- 8- to 14-bit camera interface up to 54 Mbyte/s
- Cryptographic acceleration: hardware acceleration for AES 128, 192, 256, triple DES, HASH (MD5, SHA-1, SHA-2), and HMAC
- True random number generator
- CRC calculation unit
- RTC: subsecond accuracy, hardware calendar
- 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM32F777xx	STM32F777BI, STM32F777II, STM32F777NI, STM32F777VI, STM32F777ZI
STM32F778Ax	STM32F778AI
STM32F779xx	STM32F779AI, STM32F779BI, STM32F779II, STM32F779NI

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1 Description

The STM32F777xx, STM32F778Ax and STM32F779xx devices are based on the high-performance ARM® Cortex®-M7 32-bit RISC core operating at up to 216 MHz frequency. The Cortex®-M7 core features a floating point unit (FPU) which supports ARM® double-precision and single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances the application security.

The STM32F777xx, STM32F778Ax and STM32F779xx devices incorporate high-speed embedded memories with a Flash memory up to 2 Mbytes, 512 Kbytes of SRAM (including 128 Kbytes of Data TCM RAM for critical real-time data), 16 Kbytes of instruction TCM RAM (for critical real-time routines), 4 Kbytes of backup SRAM available in the lowest power modes, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses, a 32-bit multi-AHB bus matrix and a multi layer AXI interconnect supporting internal and external memories access.

All the devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers, a true random number generator (RNG), and a cryptographic acceleration cell. They also feature standard and advanced communication interfaces.

- Up to four I^2Cs
- Six SPIs, three I^2Ss in half-duplex mode. To achieve audio class accuracy, the I^2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus four UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI)
- Three CANs
- Two SAI serial audio interfaces
- Two SDMMC host interfaces
- Ethernet and camera interfaces
- LCD-TFT display controller
- Chrom-ART Accelerator™
- SPDIFRX interface
- HDMI-CEC

Advanced peripherals include two SDMMC interfaces, a flexible memory control (FMC) interface, a Quad-SPI Flash memory interface, a camera interface for CMOS sensors and a cryptographic acceleration cell. Refer to *Table 2: STM32F777xx, STM32F778Ax and STM32F779xx features and peripheral counts* for the list of peripherals available on each part number.

The STM32F777xx, STM32F778Ax and STM32F779xx devices operate in the –40 to +105 °C temperature range from a 1.7 to 3.6 V power supply. Dedicated supply inputs for USB (OTG_FS and OTG_HS) and SDMMC2 (clock, command and 4-bit data) are available on all the packages except LQFP100 for a greater power supply choice.

The supply voltage can drop to 1.7 V with the use of an external power supply supervisor (refer to *Section 2.18.2: Internal reset OFF*). A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F777xx, STM32F778Ax and STM32F779xx devices offer devices in 10 packages ranging from 100 pins to 216 pins. The set of included peripherals changes with the device chosen.

These features make the STM32F777xx, STM32F778Ax and STM32F779xx microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile applications, Internet of Things
- Wearable devices: smartwatches.

Figure 2 shows the general block diagram of the device family

Table 2. STM32F777xx, STM32F778Ax and STM32F779xx features and peripheral counts

Peripherals		STM32F77xVx		STM32F77xZx		STM32F779Ax		STM32F778Ax	STM32F77xIx		STM32F77xBx		STM32F77xNx	
Flash memory in Kbytes		1024	2048	1024	2048	1024	2048	2048	1024	2048	1024	2048	1024	2048
SRAM in Kbytes	System	512(368+16+128)												
	Instruction	16												
	Backup	4												
FMC memory controller		Yes(1)												
Quad-SPI		Yes												
Ethernet		Yes				No			Yes					
Timers	General-purpose	10												
	Advanced-control	2												
	Basic	2												
	Low-power	1												
Random number generator		Yes												
Communication interfaces	SPI / I^2S	4/3 (simplex)(2)		6/3 (simplex)(2)										
	I^2C	4												
	USART/UART	4/4												
	USB OTG FS	Yes												
	USB OTG HS	Yes												
	CAN	3												
	SAI	2												
	SPDIFRX	4 inputs												
	SDMMC1	Yes												
	SDMMC2	Yes(3)												
Camera interface		Yes												
MIPI-DSI Host(4)		No				Yes								
LCD-TFT		Yes												
Chrom-ART Accelerator™ (DMA2D)		Yes												
JPEG codec		Yes												
Cryptography		Yes												

Table 2. STM32F777xx, STM32F778Ax and STM32F779xx features and peripheral counts (continued)

Peripherals	STM32F77xVx	STM32F77xZx	STM32F779Ax	STM32F778Ax	STM32F77xIx	STM32F77xBx	STM32F77xNx
GPIOs	82	114	129		132	159	
DFSDM1	Yes (4 filters)						
12-bit ADC	3						
Number of channels	16	24					
12-bit DAC Number of channels	Yes 2						
Maximum CPU frequency	216 MHz(5)						
Operating voltage	1.7 to 3.6 V(6)						
Operating temperatures	Ambient temperatures: –40 to +85 °C /–40 to +105 °C						
	Junction temperature: –40 to + 125 °C						
Package	LQFP100	LQFP144	WLCSP180		UFBGA176(7) LQFP176	LQFP208	TFBGA216

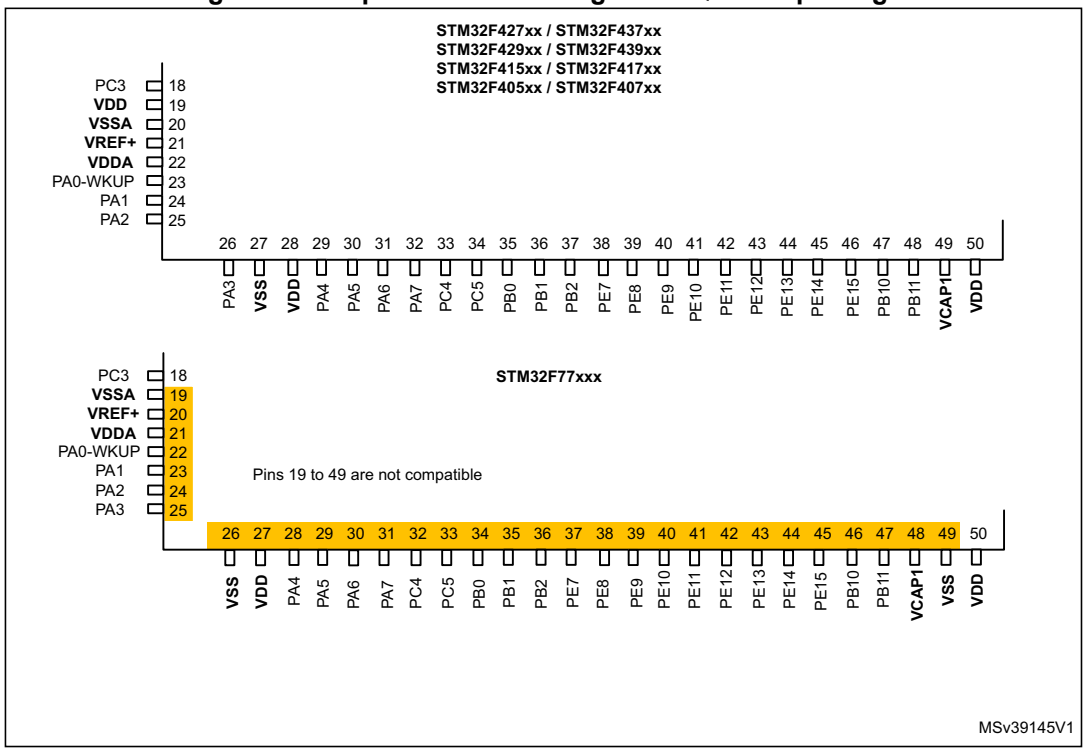
1. For the LQFP100 package, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select.
2. The SPI1, SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. SDMMC2 supports a dedicated power rail for clock, command and data 0..4 lines, feature available starting from 144 pin package.
4. DSI host interface is only available on STM32F779x sales types.
5. 216 MHz maximum frequency for - 40°C to + 85°C ambient temperature range (200 MHz maximum frequency for - 40°C to + 105°C ambient temperature range).
6. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the internal reset is OFF (refer to *Section 2.18.2: Internal reset OFF*).
7. UFBGA176 is not available for STM32F779x sales types.

1.1 Full compatibility throughout the family

The STM32F777xx, STM32F778Ax and STM32F779xx devices are fully pin-to-pin, compatible with the STM32F4xxxx devices, allowing the user to try different peripherals, and reaching higher performances (higher frequency) for a greater degree of freedom during the development cycle.

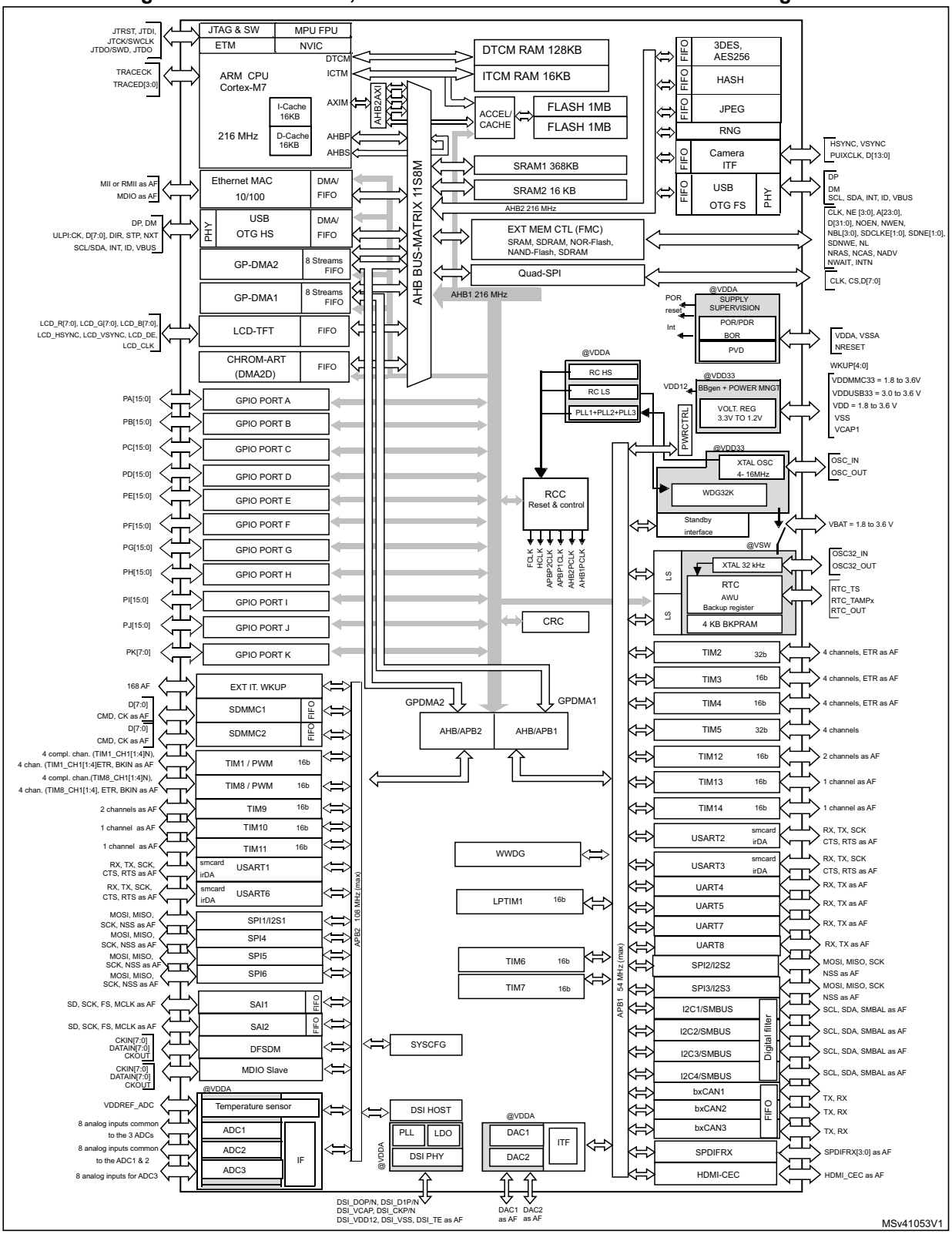
Figure 1 gives compatible board designs between the STM32F7xx and STM32F4xx families.

Figure 1. Compatible board design for LQFP100 package



The STM32F77x LQFP144, LQFP176, LQFP208, TFBGA216, UFBGA176 packages are fully pin to pin compatible with STM32F4xx devices.

Figure 2. STM32F777xx, STM32F778Ax and STM32F779xx block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 216 MHz, while the timers connected to APB1 are clocked from TIMxCLK either up to 108 MHz or 216 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

2 Functional overview

2.1 ARM® Cortex®-M7 with FPU

The ARM® Cortex®-M7 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering an outstanding computational performance and low interrupt latency.

The Cortex®-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard caches (16 Kbytes of I-cache and 16 Kbytes of D-cache)
- 64-bit AXI4 interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The processor supports the following memory interfaces:

- Tightly Coupled Memory (TCM) interface.
- Harvard instruction and data caches and AXI master (AXIM) interface.
- Dedicated low-latency AHB-Lite peripheral (AHBP) interface.

The processor supports a set of DSP instructions which allow an efficient signal processing and a complex algorithm execution.

It supports single and double precision FPU (floating point unit), speeds up software development by using metalanguage development tools, while avoiding saturation.

Figure 2 shows the general block diagram of the STM32F77xxx family.

Note: The Cortex®-M7 with FPU core is binary compatible with the Cortex®-M4 core.

2.2 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.3 Embedded Flash memory

The STM32F777xx, STM32F778Ax and STM32F779xx devices embed a Flash memory of up to 2 Mbytes available for storing programs and data. The Flash interface features:

- Single /or Dual bank operating modes,
- Read-While-Write (RWW) in Dual bank mode.

2.4 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.5 Embedded SRAM

All the devices feature:

- System SRAM up to 512 Kbytes:
  - SRAM1 on AHB bus Matrix: 368 Kbytes
  - SRAM2 on AHB bus Matrix: 16 Kbytes
  - DTCM-RAM on TCM interface (Tighly Coupled Memory interface): 128 Kbytes for critical real-time data.
- Instruction RAM (ITCM-RAM) 16 Kbytes:
  - It is mapped on TCM interface and reserved only for CPU Execution/Instruction useful for critical real-time routines.

The Data TCM RAM is accessible by the GP-DMAs and peripherals DMAs through specific AHB slave of the CPU.The instruction TCM RAM is reserved only for CPU. It is accessed at CPU clock speed with 0 wait states.

- 4 Kbytes of backup SRAM

  This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.

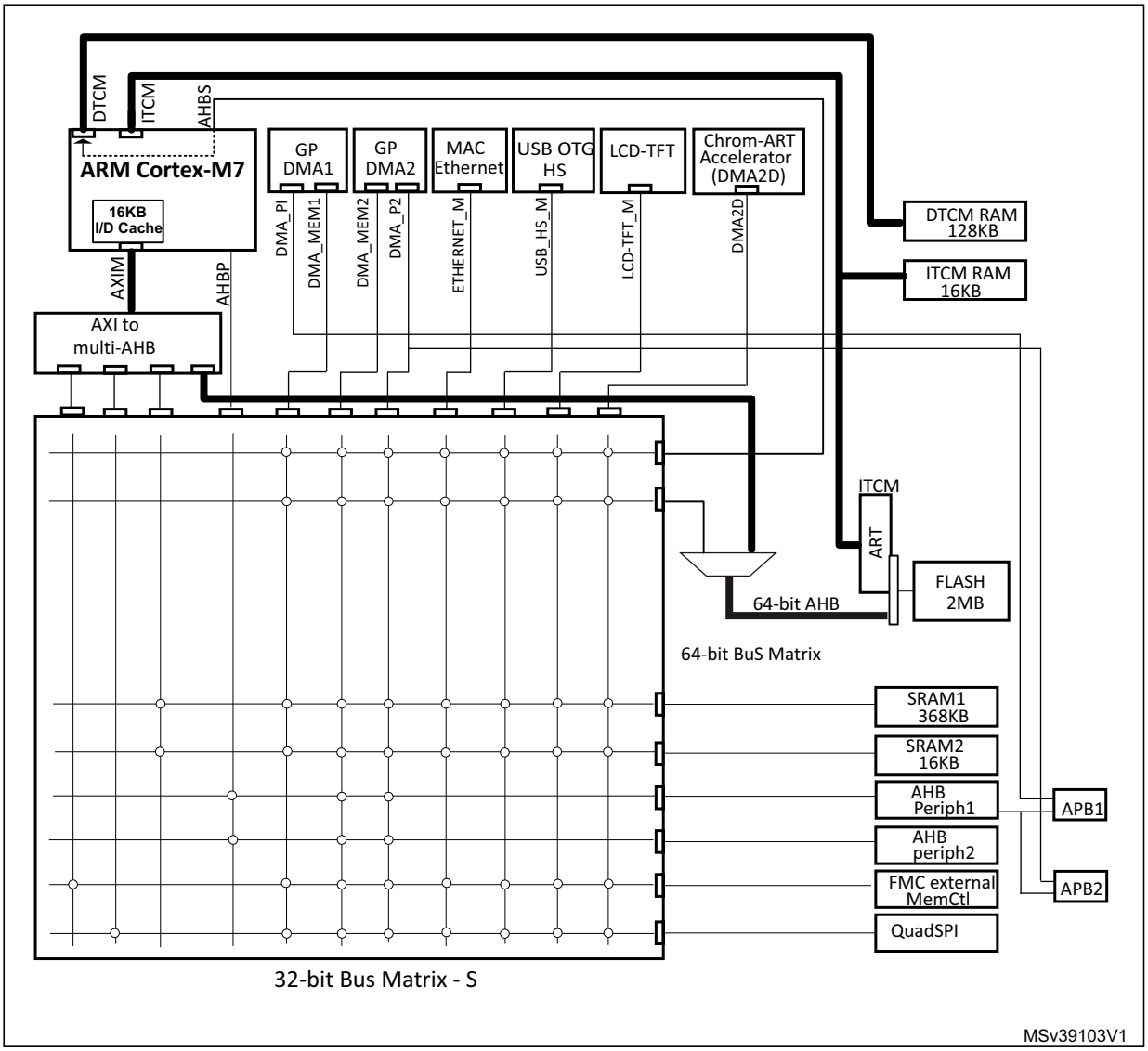
2.6 AXI-AHB bus matrix

The STM32F777xx, STM32F778Ax and STM32F779xx system architecture is based on 2 sub-systems:

- An AXI to multi AHB bridge converting AXI4 protocol to AHB-Lite protocol:
  - 3x AXI to 32-bit AHB bridges connected to AHB bus matrix
  - 1x AXI to 64-bit AHB bridge connected to the embedded Flash memory
- A multi-AHB Bus-Matrix
  - The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS, LCD-TFT, and DMA2D) and the slaves (Flash memory, RAM,

FMC, Quad-SPI, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 3. STM32F777xx, STM32F778Ax and STM32F779xx AXI-AHB bus matrix architecture(1)



1. The above figure has large wires for 64-bits bus and thin wires for 32-bits bus.

2.7 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. The configuration is made by software and the transfer sizes between the source and the destination are independent.

The DMA can be used with the main peripherals:

- SPI and I^2S
- I^2C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDMMC
- Cryptographic acceleration
- Camera interface (DCMI)
- ADC
- SAI
- SPDIFRX
- Quad-SPI
- HDMI-CEC
- JPEG codec
- DFSDM1

2.8 Flexible memory controller (FMC)

The Flexible memory controller (FMC) includes three memory controllers:

- The NOR/PSRAM memory controller
- The NAND/memory controller
- The Synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) controller

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR Flash memory/OneNAND Flash memory
  - PSRAM (4 memory banks)
  - NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) memories
- 8-,16-,32-bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is HCLK/2

LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

2.9 Quad-SPI memory interface (QUADSPI)

All the devices embed a Quad-SPI memory interface, which is a specialized communication interface targetting Single, Dual or Quad-SPI Flash memories. It can work in:

- Direct mode through registers
- External Flash status register polling mode
- Memory mapped mode.

Up to 256 Mbytes external Flash are memory mapped, supporting 8, 16 and 32-bit access. Code execution is supported.

The opcode and the frame format are fully programmable. The communication can be either in Single Data Rate or Dual Data Rate.

2.10 LCD-TFT controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 display layers with dedicated FIFO (64x32-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events

2.11 Chrom-ART Accelerator™ (DMA2D)

The Chrom-Art Accelerator™ (DMA2D) is a graphic accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion

Various image format codings are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

2.12 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 110 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M7 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.