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STM32H753xI

32-bit Arm® Cortex®-M7 400MHz MCUs, up to 2MB Flash, 1MB RAM, 46 com. and analog interfaces, crypto

Datasheet - production data

Features

Core

- 32-bit Arm® Cortex®-M7 core with double-precision FPU and L1 cache: 16 Kbytes of data and 16 Kbytes of instruction cache; frequency up to 400 MHz, MPU, 856 DMIPS/ 2.14 DMIPS/MHz (Dhrystone 2.1), and DSP instructions

Memories

- Up to 2 Mbytes of Flash memory with read-while-write support
- 1 Mbyte of RAM: 192 Kbytes of TCM RAM (inc. 64 Kbytes of ITCM RAM + 128 Kbytes of DTCM RAM for time critical routines), 864 Kbytes of user SRAM, and 4 Kbytes of SRAM in Backup domain
- Dual mode Quad-SPI memory interface running up to 133 MHz
- Flexible external memory controller with up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPSDR SDRAM, NOR/NAND Flash memory clocked up to 133 MHz in Synchronous mode
- CRC calculation unit

Security

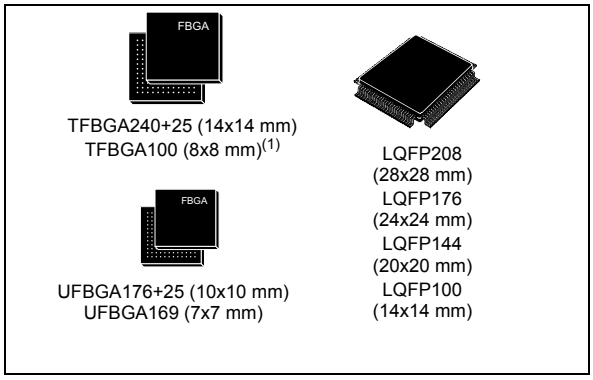
- ROP, PC-ROP, active tamper, secure firmware upgrade support, Secure access mode

General-purpose input/outputs

- Up to 168 I/O ports with interrupt capability

Reset and power management

- 3 separate power domains which can be independently clock-gated or switched off:
  - D1: high-performance capabilities
  - D2: communication peripherals and timers
  - D3: reset/clock control/power management



- 1.62 to 3.6 V application supply and I/Os
- POR, PDR, PVD and BOR
- Dedicated USB power embedding a 3.3 V internal regulator to supply the internal PHYs
- Embedded regulator (LDO) with configurable scalable output to supply the digital circuitry
- Voltage scaling in Run and Stop mode (5 configurable ranges)
- Backup regulator (~0.9 V)
- Voltage reference for analog peripheral/V_{REF+}
- Low-power modes: Sleep, Stop, Standby and V_{BAT} supporting battery charging

Low-power consumption

- Total current consumption down to 4 µA

Clock management

- Internal oscillators: 64 MHz HSI, 48 MHz HSI48, 4 MHz CSI, 32 kHz LSI
- External oscillators: 4-48 MHz HSE, 32.768 kHz LSE
- 3× PLLs (1 for the system clock, 2 for kernel clocks) with Fractional mode

Interconnect matrix

- 3 bus matrices (1 AXI and 2 AHB)
- Bridges (5× AHB2-APB, 2× AXI2-AHB)

4 DMA controllers to unload the CPU

- 1× high-speed master direct memory access controller (MDMA) with linked list support
- 2× dual-port DMAs with FIFO
- 1× basic DMA with request router capabilities

Up to 35 communication peripherals

- 4× I2Cs FM+ interfaces (SMBus/PMBus)
- 4× USARTs/4x UARTs (ISO7816 interface, LIN, IrDA, up to 12.5 Mbit/s) and 1x LPUART
- 6× SPIs, 3 with muxed duplex I2S audio class accuracy via internal audio PLL or external clock, 1x I2S in LP domain (up to 133 MHz)
- 4x SAIs (serial audio interface)
- SPDIFRX interface
- SWPMI single-wire protocol master I/F
- MDIO Slave interface
- 2× SD/SDIO/MMC interfaces (up to 125 MHz)
- 2× CAN controllers: 2 with CAN FD, 1 with time-triggered CAN (TT-CAN)
- 2× USB OTG interfaces (1FS, 1HS/FS) crystal-less solution with LPM and BCD
- Ethernet MAC interface with DMA controller
- HDMI-CEC
- 8- to 14-bit camera interface (up to 80 MHz)

11 analog peripherals

- 3× ADCs with 16-bit max. resolution (up to 36 channels, 4.5 MSPS at 12 bits)
- 1× temperature sensor
- 2× 12-bit D/A converters (1 MHz)
- 2× ultra-low-power comparators
- 2× operational amplifiers (8 MHz bandwidth)
- 1× digital filters for sigma delta modulator (DFSDM) with 8 channels/4 filters

Graphics

- LCD-TFT controller up to XGA resolution
- Chrom-ART graphical hardware Accelerator™ (DMA2D) to reduce CPU load
- Hardware JPEG Codec

Up to 22 timers and watchdogs

- 1× high-resolution timer (2.5 ns max resolution)
- 2× 32-bit timers with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input (up to 200 MHz)
- 2× 16-bit advanced motor control timers (up to 200 MHz)
- 10× 16-bit general-purpose timers (up to 200 MHz)
- 5× 16-bit low-power timers (up to 200 MHz)
- 2× watchdogs (independent and window)
- 1× SysTick timer
- RTC with sub-second accuracy & HW calendar

Cryptographic acceleration

- AES 128, 192, 256, TDES,
- HASH (MD5, SHA-1, SHA-2), HMAC
- True random number generators

Debug mode

- SWD & JTAG interfaces
- 4-Kbyte Embedded Trace Buffer

96-bit unique ID

All packages are ECOPACK®2 compliant

Table 1. Device summary

Reference	Part number
STM32H753xI	STM32H753VI, STM32H753ZI, STM32H753II, STM32H753BI, STM32H753XI, STM32H753AI

Contents

List of tables

List of figures

1 Introduction

This document provides information on STM32H53xI microcontrollers, such as description, functional overview, pin assignment and definition, electrical characteristics, packaging, and ordering information.

This document should be read in conjunction with the STM32H53xI reference manual (RM0433), available from the STMicroelectronics website *www.st.com*.

For information on the Arm®(a) Cortex®-M7 core, please refer to the Cortex®-M7 Technical Reference Manual, available from the http://www.arm.com website.

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2 Description

STM32H753xI devices are based on the high-performance Arm® Cortex®-M7 32-bit RISC core operating at up to 400 MHz. The Cortex® -M7 core features a floating point unit (FPU) which supports Arm® double-precision (IEEE 754 compliant) and single-precision data-processing instructions and data types. STM32H753xI devices support a full set of DSP instructions and a memory protection unit (MPU) to enhance application security.

STM32H753xI devices incorporate high-speed embedded memories with a dual-bank Flash memory up to 2 Mbytes, 1 Mbyte of RAM (including 192 Kbytes of TCM RAM, 864 Kbytes of user SRAM and 4 Kbytes of backup SRAM), as well as an extensive range of enhanced I/Os and peripherals connected to APB buses, AHB buses, 2x32-bit multi-AHB bus matrix and a multi layer AXI interconnect supporting internal and external memory access.

All the devices offer three ADCs, two DACs, two ultra-low power comparators, a low-power RTC, a high-resolution timer, 12 general-purpose 16-bit timers, two PWM timers for motor control, five low-power timers, a true random number generator (RNG), and a cryptographic acceleration cell. The devices support four digital filters for external sigma-delta modulators (DFSDM). They also feature standard and advanced communication interfaces.

- Standard peripherals
  - Four I^2Cs
  - Four USARTs, four UARTs and one LPUART
  - Six SPIs, three I^2Ss in Half-duplex mode. To achieve audio class accuracy, the I^2S peripherals can be clocked by a dedicated internal audio PLL or by an external clock to allow synchronization.
  - Four SAI serial audio interfaces
  - One SPDIFRX interface
  - One SWPMI (Single Wire Protocol Master Interface)
  - Management Data Input/Output (MDIO) slaves
  - Two SDMMC interfaces
  - A USB OTG full-speed and a USB OTG high-speed interface with full-speed capability (with the ULPI)
  - One FDCAN plus one TT-CAN interface
  - An Ethernet interface
  - Chrom-ART Accelerator™
  - HDMI-CEC
- Advanced peripherals including
  - A flexible memory control (FMC) interface
  - A Quad-SPI Flash memory interface
  - A camera interface for CMOS sensors
  - An LCD-TFT display controller
  - A JPEG hardware compressor/decompressor

Refer to *Table 2: STM32H753xI features and peripheral counts* for the list of peripherals available on each part number.

STM32H753xI devices operate in the –40 to +85 °C temperature range from a 1.62 to 3.6 V power supply. The supply voltage can drop down to 1.62 V by using an external power supervisor (see *Section 3.5.2: Power supply supervisor)* and connecting the PDR_ON pin to V_{SS}. Otherwise the supply voltage must stay above 1.71 V with the embedded power voltage detector enabled.

Dedicated supply inputs for USB (OTG_FS and OTG_HS) are available on all packages except LQFP100 to allow a greater power supply choice.

A comprehensive set of power-saving modes allows the design of low-power applications.

STM32H753xI devices are offered in 8 packages ranging from 100 pins to 240 pins/balls. The set of included peripherals changes with the device chosen.

These features make STM32H753xI microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile applications, Internet of Things
- Wearable devices: smart watches.

Figure 1 shows the general block diagram of the device family.

Table 2. STM32H753xI features and peripheral counts

Peripherals		STM32H753VI	STM32H753ZI	STM32H753AI	STM32H753II	STM32H753BI	STM32H753XI
Flash memory in Kbytes		2048					
SRAM in Kbytes	SRAM mapped onto AXI bus	512					
	SRAM1 (D2 domain)	128					
	SRAM2 (D2 domain)	128					
	SRAM3 (D2 domain)	32					
	SRAM4 (D3 domain)	64					
TCM RAM in Kbytes	ITCM RAM (instruction)	64					
	DTCM RAM (data)	128					
Backup SRAM (Kbytes)		4					
FMC		Yes					
Quad-SPI		Yes					
Ethernet		Yes					

Table 2. STM32H753xI features and peripheral counts (continued)

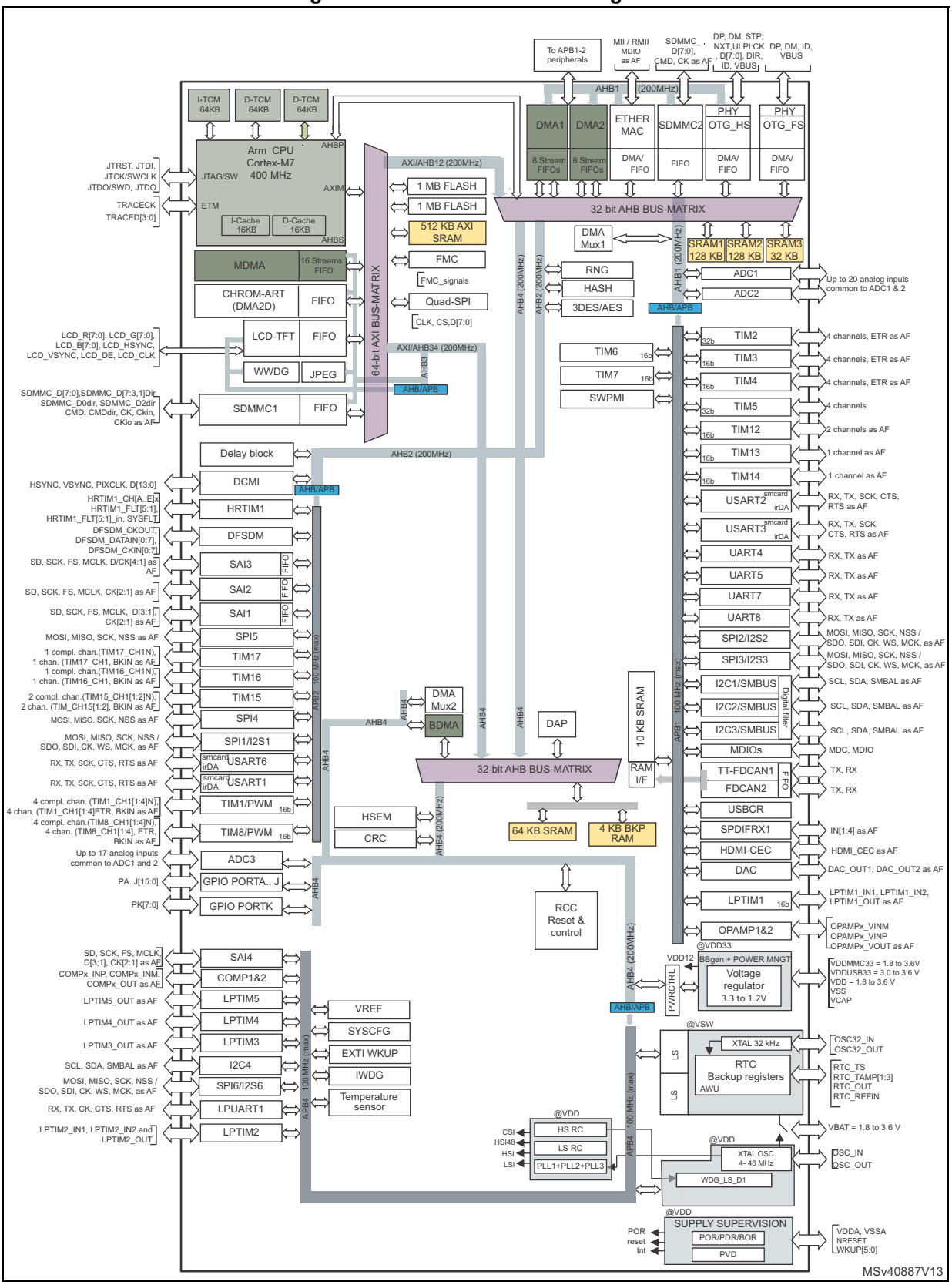
Peripherals		STM32H 753VI	STM32H 753ZI	STM32H 753AI	STM32H 753II	STM32H 753BI	STM32H 753XI
Timers	High-resolution	1					
	General-purpose	10					
	Advanced-control (PWM)	2					
	Basic	2					
	Low-power	5					
Random number generator		Yes					
Cryptographic accelerator		Yes					
Communication interfaces	SPI / I^2S	6/3(1)					
	I^2C	4					
	USART/UART/ LPUART	4/4 /1					
	SAI	4					
	SPDIFRX	4 inputs					
	SWPMI	Yes					
	MDIO	Yes					
	SDMMC	2					
	FDCAN/TT-CAN	1/1					
	USB OTG_FS	Yes					
	USB OTG_HS	Yes					
Ethernet and camera interface		Yes					
LCD-TFT		Yes					
JPEG Codec		Yes					
Chrom-ART Accelerator™ (DMA2D)		Yes					
GPIOs		82	114	131	140	168	
16-bit ADCs Number of channels		3 Up to 36					
12-bit DAC Number of channels		Yes 2					
Comparators		2					
Operational amplifiers		2					
DFSDM		Yes					
Maximum CPU frequency		400 MHz					
Operating voltage		1.71 to 3.6 V(2)	1.62 to 3.6 V(3)				

Table 2. STM32H753xI features and peripheral counts (continued)

Peripherals	STM32H 753VI	STM32H 753ZI	STM32H 753AI	STM32H 753II	STM32H 753BI	STM32H 753XI
Operating temperatures	Ambient temperatures: –40 up to +85 °C(4)					
	Junction temperature: –40 to + 125 °C					
Package	LQFP100 TFBGA100(5)	LQFP144	UFBGA 169(5)	LQFP176 UFBGA 176+25	LQFP208	TFBGA 240+25

1. The SPI1, SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
2. Since the LQFP100 package does not feature the PDR_ON pin (tied internally to V_{DD}), the minimum V_{DD} value for this package is 1.71 V.
3. V_{DD}/V_{DDA} can drop down to 1.62 V by using an external power supervisor (see *Section 3.5.2: Power supply supervisor*) and connecting PDR_ON pin to V_{SS}. Otherwise the supply voltage must stay above 1.71 V with the embedded power voltage detector enabled.
4. The product junction temperature must be kept within the –40 to +125 °C temperature range.
5. This package is under development. Please contact STMicroelectronics for details.

Figure 1. STM32H753xI block diagram



3 Functional overview

3.1 Arm® Cortex®-M7 with FPU

The Arm® Cortex®-M7 with double-precision FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and optimized power consumption, while delivering outstanding computational performance and low interrupt latency.

The Cortex®-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard architecture with L1 caches (16 Kbytes of I-cache and 16 Kbytes of D-cache)
- 64-bit AXI interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The following memory interfaces are supported:

- Separate Instruction and Data buses (Harvard Architecture) to optimize CPU latency
- Tightly Coupled Memory (TCM) interface designed for fast and deterministic SRAM accesses
- AXI Bus interface to optimize Burst transfers
- Dedicated low-latency AHB-Lite peripheral bus (AHBP) to connect to peripherals.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

It also supports single and double precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

Figure 1 shows the general block diagram of the STM32H753xI family.

Note: Cortex®-M7 with FPU core is binary compatible with the Cortex®-M4 core.

3.2 Memory protection unit (MPU)

The memory protection unit (MPU) manages the CPU access rights and the attributes of the system resources. It has to be programmed and enabled before use. Its main purposes are to prevent an untrusted user program to accidentally corrupt data used by the OS and/or by a privileged task, but also to protect data processes or read-protect memory regions.

The MPU defines access rules for privileged accesses and user program accesses. It allows defining up to 16 protected regions that can in turn be divided into up to 8 independent subregions, where region address, size, and attributes can be configured. The protection area ranges from 32 bytes to 4 Gbytes of addressable memory.

When an unauthorized access is performed, a memory management exception is generated.

3.3 Memories

3.3.1 Embedded Flash memory

The STM32H753xI devices embed up to 2 Mbytes of Flash memory that can be used for storing programs and data.

The Flash memory is organized as 266-bit Flash words memory that can be used for storing both code and data constants. Each word consists of:

- One Flash word (8 words, 32 bytes or 256 bits)
- 10 ECC bits.

The Flash memory is divided into two independent banks. Each bank is organized as follows:

- A 1-Mbyte user Flash memory block containing eight user sectors of 128 Kbytes(4 K Flash words)
- 128 Kbytes of System Flash memory from which the device can boot
- 2 Kbytes (64 Flash words) of user option bytes for user configuration

3.3.2 Secure access mode

In addition to other typical memory protection mechanism (RDP, PCROP), STM32H753xI devices introduce the Secure access mode, a new enhanced security feature. This mode allows developing user-defined secure services by ensuring, on the one hand code and data protection and on the other hand code safe execution.

Two types of secure services are available:

- STMicroelectronics Root Secure Services:

  These services are embedded in System memory. They provide a secure solution for firmware and third-party modules installation. These services rely on cryptographic algorithms based on a device unique private key.
- User-defined secure services:

  These services are embedded in user Flash memory. Examples of user secure services are proprietary user firmware update solution, secure Flash integrity check or any other sensitive applications that require a high level of protection.

  The secure firmware is embedded in specific user Flash memory areas configured through option bytes.

Secure services are executed just after a reset and preempt all other applications to guarantee protected and safe execution. Once executed, the corresponding code and data are no more accessible.

The above secure services are available only for Cortex®-M7 core operating in Secure access mode. The other masters cannot access the option bytes involved in Secure access mode settings or the Flash secured areas.

3.3.3 Embedded SRAM

All devices feature:

- 512 Kbytes of AXI-SRAM mapped onto AXI bus on D1 domain.
- SRAM1 mapped on D2 domain: 128 Kbytes
- SRAM2 mapped on D2 domain: 128 Kbytes
- SRAM3 mapped on D2 domain: 32 Kbytes
- SRAM4 mapped on D3 domain: 64 Kbytes
- 4 Kbytes of backup SRAM

  The content of this area is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.
- RAM mapped to TCM interface (ITCM and DTCM):

  Both ITCM and DTCM RAMs are 0 wait state memories. either They can be accessed either from the CPU or the MDMA (even in Sleep mode) through a specific AHB slave of the CPU(AHBP):

  – 64 Kbytes of ITCM-RAM (instruction RAM)

    This RAM is connected to ITCM 64-bit interface designed for execution of critical real-times routines by the CPU.

  – 128 Kbytes of DTCM-RAM (2x 64-Kbyte DTCM-RAMs on 2x32-bit DTCM ports)

    The DTCM-RAM could be used for critical real-time data, such as interrupt service routines or stack/heap memory. Both DTCM-RAMs can be used in parallel (for load/store operations) thanks to the Cortex®-M7 dual issue capability.

  The MDMA can be used to load code or data in ITCM or DTCM RAMs.

Error code correction (ECC)

Over the product lifetime, and/or due to external events such as radiations, invalid bits in memories may occur. They can be detected and corrected by ECC. This is an expected behavior that has to be managed at final-application software level in order to ensure data integrity through ECC algorithms implementation.

SRAM data are protected by ECC:

- 7 ECC bits are added per 32-bit word.
- 8 ECC bits are added per 64-bit word for AXI-SRAM and ITCM-RAM.

The ECC mechanism is based on the SECDED algorithm. It supports single-error correction and double-error detection.

3.4 Boot modes

At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDx option bytes, allowing to program any boot memory address from 0x0000 0000 to 0x3FFF FFFF which includes:

- All Flash address space
- All RAM address space: ITCM, DTCM RAMs and SRAMs
- The System memory bootloader

The boot loader is located in non-user System memory. It is used to reprogram the Flash memory through a serial interface (USART, I2C, SPI, USB-DFU). Refer to *STM32 microcontroller System memory Boot mode* application note (AN2606) for details.

3.5 Power supply management

3.5.1 Power supply scheme

STM32H53xI power supply voltages are the following:

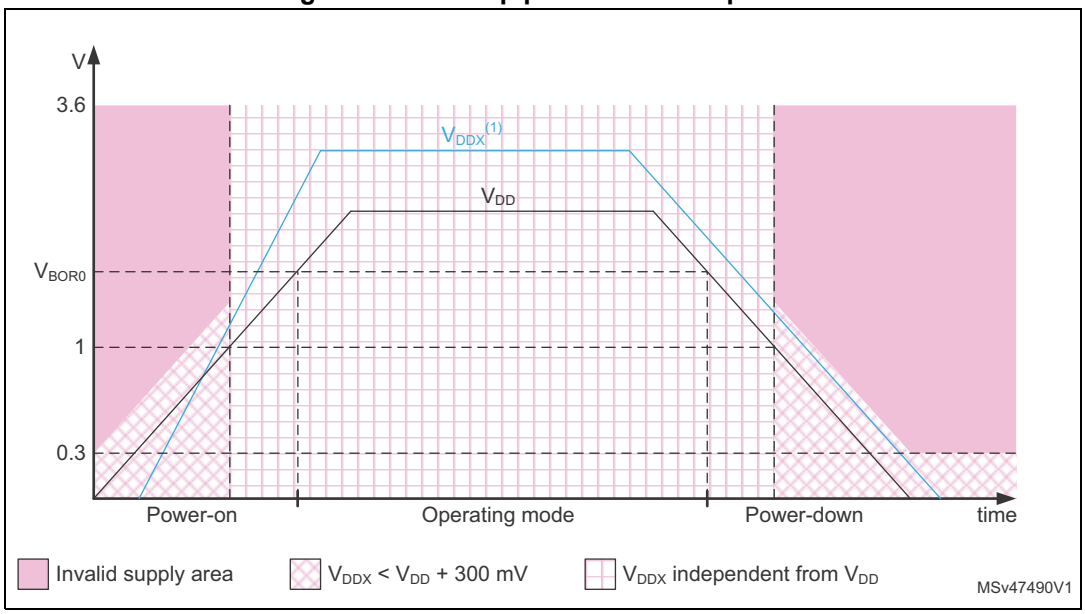
- V_{DD} = 1.62 to 3.6 V: external power supply for I/Os, provided externally through V_{DD} pins.
- V_{DDLDO} = 1.62 to 3.6 V: supply voltage for the internal regulator supplying V_{CORE}
- V_{DDA} = 1.62 to 3.6 V: external analog power supplies for ADC, DAC, COMP and OPAMP.
- $V_{DD33USB}$ and $V_{DD50USB}$:
  $V_{DD50USB}$ can be supplied through the USB cable to generate the $V_{DD33USB}$ via the USB internal regulator. This allows supporting a V_{DD} supply different from 3.3 V.
  The USB regulator can be bypassed to supply directly $V_{DD33USB}$ if V_{DD} = 3.3 V.
- V_{BAT} = 1.2 to 3.6 V: power supply for the V_{SW} domain when V_{DD} is not present.
- V_{CAP}: V_{CORE} supply voltage, which values depend on voltage scaling (0.7 V, 0.9 V, 1.0 V, 1.1 V or 1.2 V). They are configured through VOS bits in PWR_D3CR register. The V_{CORE} domain is split into the following power domains that can be independently switch off.
  - D1 domain containing some peripherals and the Cortex®-M7 core.
  - D2 domain containing a large part of the peripherals.
  - D3 domain containing some peripherals and the system control.

During power-up and power-down phases, the following power sequence requirements must be respected (see *Figure 2*):

- When V_{DD} is below 1 V, other power supplies (V_{DDA}, $V_{DD33USB}$, $V_{DD50USB}$) must remain below V_{DD} + 300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.

During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the microcontroller remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

Figure 2. Power-up/power-down sequence



1. V_{DDx} refers to any power supply among V_{DDA}, $V_{DD33USB}$, $V_{DD50USB}$.

3.5.2 Power supply supervisor

The devices have an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry:

- Power-on reset (POR)

  The POR supervisor monitors V_{DD} power supply and compares it to a fixed threshold. The devices remain in Reset mode when V_{DD} is below this threshold,

- Power-down reset (PDR)

  The PDR supervisor monitors V_{DD} power supply. A reset is generated when V_{DD} drops below a fixed threshold.

  The PDR supervisor can be enabled/disabled through PDR_ON pin.

- Brownout reset (BOR)

  The BOR supervisor monitors V_{DD} power supply. Three BOR thresholds (from 2.1 to 2.7 V) can be configured through option bytes. A reset is generated when V_{DD} drops below this threshold.

3.5.3 Voltage regulator

The same voltage regulator supplies the 3 power domains (D1, D2 and D3). D1 and D2 can be independently switched off.

Voltage regulator output can be adjusted according to application needs through 5 power supply levels:

- Run mode (VOS1 to VOS3)
  - Scale 1: high performance
  - Scale 2: medium performance and consumption
  - Scale 3: optimized performance and low-power consumption
- Stop mode (SVOS3 to SVOS5)
  - Scale 3: peripheral with wakeup from Stop mode capabilities (UART, SPI, I2C, LPTIM) are operational
  - Scale 4 and 5 where the peripheral with wakeup from Stop mode is disabled

    The peripheral functionality is disabled but wakeup from Stop mode is possible through GPIO or asynchronous interrupt.

3.6 Low-power strategy

There are several ways to reduce power consumption on STM32H753xI:

- Decrease dynamic power consumption by slowing down the system clocks even in Run mode and individually clock gating the peripherals that are not used.
- Save power consumption when the CPU is idle, by selecting among the available low-power mode according to the user application needs. This allows achieving the best compromise between short startup time, low-power consumption, as well as available wakeup sources.

The devices feature several low-power modes:

- CSleep (CPU clock stopped)
- CStop (CPU sub-system clock stopped)
- DStop (Domain bus matrix clock stopped)
- Stop (System clock stopped)
- DStandby (Domain powered down)
- Standby (System powered down)

CSleep and CStop low-power modes are entered by the MCU when executing the WFI (Wait for Interrupt) or WFE (Wait for Event) instructions, or when the SLEEPONEXIT bit of the Cortex®-Mx core is set after returning from an interrupt service routine.

A domain can enter low-power mode (DStop or DStandby) when the processor, its subsystem and the peripherals allocated in the domain enter low-power mode.

If part of the domain is not in low-power mode, the domain remains in the current mode.

Finally the system can enter Stop or Standby when all EXTI wakeup sources are cleared and the power domains are in DStop or DStandby mode.

Table 3. System vs domain low-power mode

System power mode	D1 domain power mode	D2 domain power mode	D3 domain power mode
Run	DRun/DStop/DStandby	DRun/DStop/DStandby	DRun
Stop	DStop/DStandby	DStop/DStandby	DStop
Standby	DStandby	DStandby	DStandby

3.7 Reset and clock controller (RCC)

The clock and reset controller is located in D3 domain. The RCC manages the generation of all the clocks, as well as the clock gating and the control of the system and peripheral resets. It provides a high flexibility in the choice of clock sources and allows to apply clock ratios to improve the power consumption. In addition, on some communication peripherals that are capable to work with two different clock domains (either a bus interface clock or a kernel peripheral clock), the system frequency can be changed without modifying the baudrate.

3.7.1 Clock management

The devices embed four internal oscillators, two oscillators with external crystal or resonator, two internal oscillators with fast startup time and three PLLs.

The RCC receives the following clock source inputs:

- Internal oscillators:
  - 64 MHz HSI clock
  - 48 MHz RC oscillator
  - 4 MHz CSI clock
  - 32 kHz LSI clock
- External oscillators:
  - 4-48 MHz HSE clock
  - 32.768 kHz LSE clock

The RCC provides three PLLs: one for system clock, two for kernel clocks.

The system starts on the HSI clock. The user application can then select the clock configuration.

3.7.2 System reset sources

Power-on reset initializes all registers while system reset reinitializes the system except for the debug, part of the RCC and power controller status registers, as well as the backup power domain.

A system reset is generated in the following cases:

- Power-on reset (pwr_por_rst)
- Brownout reset
- Low level on NRST pin (external reset)
- Window watchdog
- Independent watchdog
- Software reset
- Low-power mode security reset
- Exit from Standby

3.8 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

After reset, all GPIOs (except debug pins) are in Analog mode to reduce power consumption (refer to GPIOs register reset values in the device reference manual).

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.9 Bus-interconnect matrix

The devices feature an AXI bus matrix, two AHB bus matrices and bus bridges that allow interconnecting bus masters with bus slaves (see *Figure 3*).