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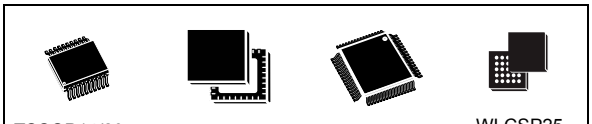
STM32L011x3 STM32L011x4

Access line ultra-low-power 32-bit MCU ARM®-based Cortex®-M0+, up to 16KB Flash, 2KB SRAM, 512B EEPROM, ADC

Datasheet - production data

Features

- Ultra-low-power platform
  - 1.65 V to 3.6 V power supply
  - -40 to 125 °C temperature range
  - 0.23 µA Standby mode (2 wakeup pins)
  - 0.29 µA Stop mode (16 wakeup lines)
  - 0.54 µA Stop mode + RTC + 2 KB RAM retention
  - Down to 76 µA/MHz in Run mode
  - 5 µs wakeup time (from Flash memory)
  - 41 µA 12-bit ADC conversion at 10 ksps
- Core: ARM® 32-bit Cortex®-M0+
  - From 32 kHz to 32 MHz max.
  - 0.95 DMIPS/MHz
- Reset and supply management
  - Ultra-safe, low-power BOR (brownout reset) with 5 selectable thresholds
  - Ultralow power POR/PDR
  - Programmable voltage detector (PVD)
- Clock sources
  - 0 to 32 MHz external clock
  - 32 kHz oscillator for RTC with calibration
  - High speed internal 16 MHz factory-trimmed RC (+/- 1%)
  - Internal low-power 37 kHz RC
  - Internal multispeed low-power 65 kHz to 4.2 MHz RC
  - PLL for CPU clock
- Pre-programmed bootloader
  - USART, SPI supported
- Development support
  - Serial wire debug supported
- Up to 28 fast I/Os (23 I/Os 5V tolerant)
- Memories
  - Up to 16 KB Flash memory with ECC
  - 2 KB RAM
  - 512 B of data EEPROM with ECC
  - 20-byte backup register
  - Sector protection against R/W operation



TSSOP14/20 169 mils | UFQFPN20 3x3 mm UFQFPN28 4x4 mm UFQFPN32 5x5 mm | LQFP32 7x7 mm | WLCSP25 2.133x2.070 mm

- Rich Analog peripherals
  - 12-bit ADC 1.14 Msps up to 10 channels (down to 1.65 V)
  - 2x ultra-low-power comparators (window mode and wake up capability, down to 1.65 V)
- 5-channel DMA controller, supporting ADC, SPI, I2C, USART, Timers
- 4x peripherals communication interface
- 1x USART (ISO 7816, IrDA), 1x UART (low power)
- 1x SPI 16 Mbits/s
- 1x I2C (SMBus/PMBus)
- 7x timers: 1x 16-bit with up to 4 channels, 1x 16-bit with up to 2 channels, 1x 16-bit ultra-low-power timer, 1x SysTick, 1x RTC and 2x watchdogs (independent/window)
- CRC calculation unit, 96-bit unique ID
- All packages are ECOPACK®2

Table 1. Device summary

Reference	Part number
STM32L011x3	STM32L011G3, STM32L011K3, STM32L011E3, STM32L011F3, STM32L011D3
STM32L011x4	STM32L011G4, STM32L011K4, STM32L011E4, STM32L011F4, STM32L011D4

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1 Introduction

The ultra-low-power STM32L011x3/4 family includes devices in 7 different package types from 14 to 32 pins. The description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L011x3/4 microcontrollers suitable for a wide range of applications:

- Gas/water meters and industrial sensors
- Healthcare and fitness equipment
- Remote control and user interface
- PC peripherals, gaming, GPS equipment
- Alarm system, wired and wireless sensors, video intercom

This STM32L011x3/4 datasheet should be read in conjunction with the STM32L0x1 reference manual (RM0377).

For information on the ARM® Cortex®-M0+ core please refer to the Cortex®-M0+ Technical Reference Manual, available from the www.arm.com website.

Figure 1 shows the general block diagram of the device family.

2 Description

The access line ultra-low-power STM32L011x3/4 family incorporates the high-performance ARM® Cortex®-M0+ 32-bit RISC core operating at a 32 MHz frequency, high-speed embedded memories (up to 16 Kbytes of Flash program memory, 512 bytes of data EEPROM and 2 Kbytes of RAM) plus an extensive range of enhanced I/Os and peripherals.

The STM32L011x3/4 devices provide high power efficiency for a wide range of performance. It is achieved with a large choice of internal and external clock sources, an internal voltage adaptation and several low-power modes.

The STM32L011x3/4 devices offer several analog features, one 12-bit ADC with hardware oversampling, two ultra-low-power comparators, several timers, one low-power timer (LPTIM), three general-purpose 16-bit timers, one RTC and one SysTick which can be used as timebases. They also feature two watchdogs, one watchdog with independent clock and window capability and one window watchdog based on bus clock.

Moreover, the STM32L011x3/4 devices embed standard and advanced communication interfaces: one I2C, one SPI, one USART, and a low-power UART (LPUART).

The STM32L011x3/4 also include a real-time clock and a set of backup registers that remain powered in Standby mode.

The ultra-low-power STM32L011x3/4 devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +125 °C temperature range. A comprehensive set of power-saving modes allows the design of low-power applications.

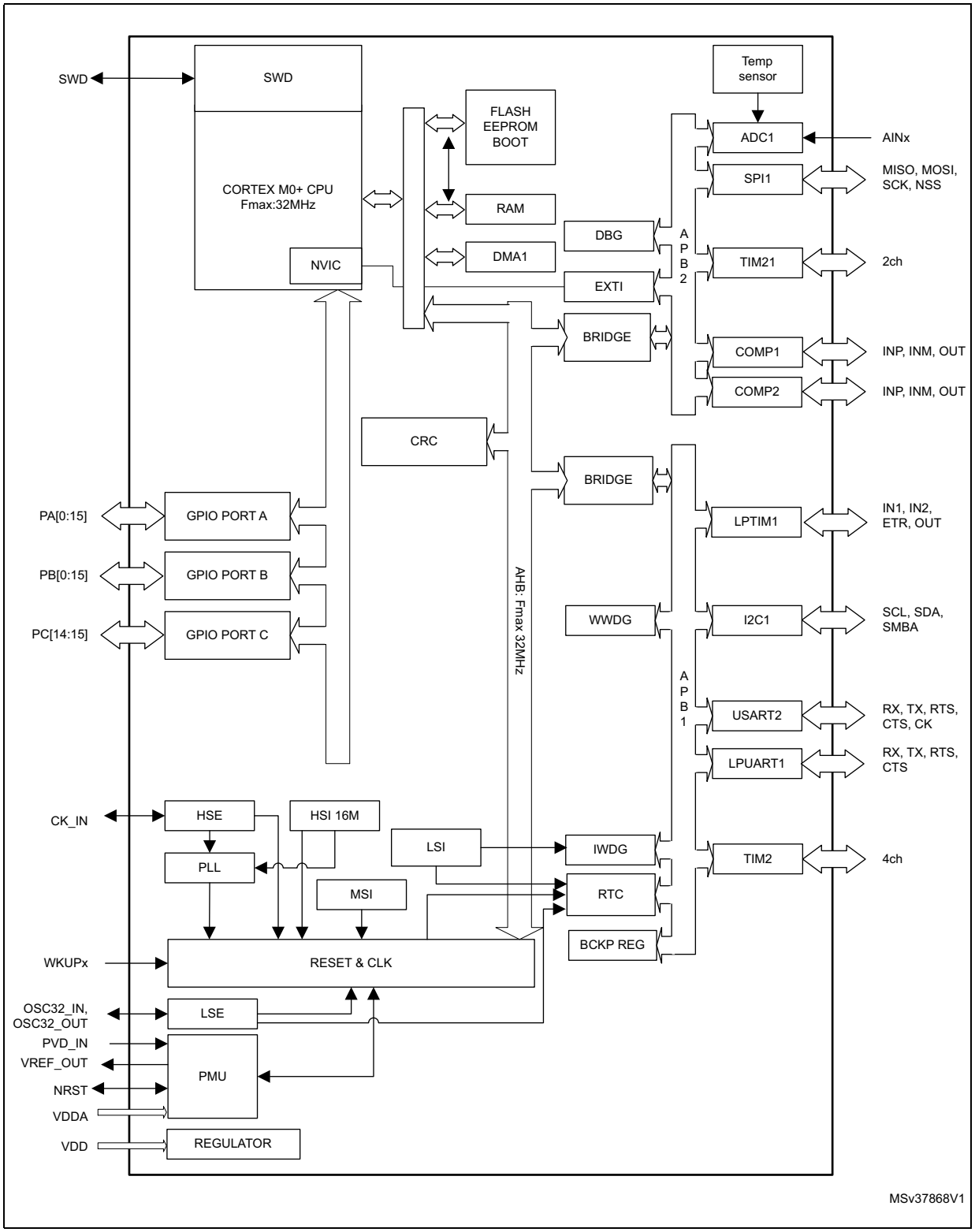
2.1 Device overview

Table 2. Ultra-low-power STM32L011x3/x4 device features and peripheral counts

Peripheral		STM32 L011D3	STM32 L011F3	STM32 L011E3	STM32 L011G3	STM32 L011K3	STM32 L011D4	STM32 L011F4	STM32 L011E4	STM32 L011G4	STM32 L011K4
Flash (Kbytes)		8					16				
Data EEPROM (bytes)		512									
RAM (Kbytes)		2									
Timers	General-purpose	2									
	LPTIM	1									
RTC/SYSTICK/IWDG/ WWDG		1/1/1/1									
Communi-cation interfaces	SPI	1									
	I^2C	1									
	USART	1									
	LPUART	1									
GPIOs		11	16	21	24	26/28(1)	11	16	21	24	26/28(1)
Clocks: HSE(2)/LSE/HSI/MSI/LSI		1/1/1/1/1									
12b synchronized ADC Number of channels		1 4	1 7/9(3)	1 10			1 4	1 7/9(3)	1 10		
Comparators		2									
Max. CPU frequency		32 MHz									
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V without BOR option									
Operating temperatures		Ambient temperature: –40 to +125 °C Junction temperature: –40 to +130 °C									
Packages		TSSOP 14	TSSOP/ UFQFPN 20	WLCSP 25	UFQFPN 28	LQFP/ UFQFPN 32	TSSOP 14	TSSOP/ UFQFPN 20	WLCSP 25	UFQFPN 28	LQFP/, UFQFPN 32

1. The devices feature 26 and 28 GPIOs on LQFP32 and UFQFPN32, respectively.
2. HSE available only as external clock input (HSE bypass).
3. The devices feature 7 and 9 ADC channels on UFQFPN20 and TSSOP20, respectively.

Figure 1. STM32L011x3/4 block diagram



2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of core and features, from 8-bit proprietary core up to ARM® Cortex®-M4, including ARM® Cortex®-M3 and ARM® Cortex®-M0+. The STM32Lx series are the best choice to answer your needs in terms of ultra-low-power features. The STM32 Ultra-low-power series are the best solution for applications such as gas/water meter, keyboard/mouse or fitness and healthcare application. Several built-in features like LCD drivers, dual-bank memory, low-power Run mode, operational amplifiers, 128-bit AES, DAC, crystal-less USB and many other definitely help you building a highly cost optimized application by reducing BOM cost. STMicroelectronics, as a reliable and long-term manufacturer, ensures as much as possible pin-to-pin compatibility between all STM8Lx and STM32Lx on one hand, and between all STM32Lx and STM32Fx on the other hand. Thanks to this unprecedented scalability, your legacy application can be upgraded to respond to the latest market feature and efficiency requirements.

3 Functional overview

3.1 Low-power modes

The ultra-low-power STM32L011x3/4 supports dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 (V_{DD} range limited to 1.71-3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full V_{DD} range), with a maximum CPU frequency of 16 MHz
- Range 3 (full V_{DD} range), with a maximum CPU frequency limited to 4.2 MHz

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

- **Low-power run mode**

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the low-speed clock (max 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In Low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

- **Low-power sleep mode**

  This mode is achieved by entering Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

  When wakeup is triggered by an event or an interrupt, the system reverts to the Run mode with the regulator on.

- **Stop mode with RTC**

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSE and HSI RC oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

  Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

  The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event

(if internal reference voltage is on), it can be the RTC alarm/tamper/timestamp/wakeup events, the USART/I2C/LPUART/LPTIM wakeup events.

- **Stop mode without RTC**

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillator are disabled.

  Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

  The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on). It can also be wakened by the USART/I2C/LPUART/LPTIM wakeup events.

- **Standby mode with RTC**

  The Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSE bypass and HSI RC oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby mode without RTC**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillator are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

Operating power supply range	Functionalities depending on the operating power supply range		
	ADC operation	Dynamic voltage scaling range	I/O operation
V_{DD} = 1.65 to 1.71 V	ADC only, conversion time up to 570 ksps	Range 2 or range 3	Degraded speed performance
V_{DD} = 1.71 to 1.8 V(1)	ADC only, conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Degraded speed performance

Table 3. Functionalities depending on the operating power supply range (continued)

Operating power supply range	Functionalities depending on the operating power supply range		
	ADC operation	Dynamic voltage scaling range	I/O operation
V_{DD} = 1.8 to 2.0 V(1)	Conversion time up to 1.14 Msps	Range1, range 2 or range 3	Degraded speed performance
V_{DD} = 2.0 to 2.4 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation
V_{DD} = 2.4 to 3.6 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation

1. CPU frequency changes from initial to final must respect the condition: $f_{CPU\ initial} < 4f_{CPU\ initial}$. It must also respect 5 µs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5 µs, then switch from 16 MHz to 32 MHz.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
32 kHz to 4.2 MHz (0ws)	Range 3

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (1)(2)

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
CPU	Y	-	Y	-	-	-	-	-
Flash memory	O	O	O	O	-	-	-	-
RAM	Y	Y	Y	Y	Y	-	-	-
Backup registers	Y	Y	Y	Y	Y	-	Y	-
EEPROM	O	O	O	O	-	-	-	-
Brown-out reset (BOR)	O	O	O	O	O	O	O	O
DMA	O	O	O	O	-	-	-	-

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)[1][2]

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	-	-
Power-on/down reset (POR/PDR)	Y	Y	Y	Y	Y	Y	Y	Y
High Speed Internal (HSI)	O	O	-	-	[3]	-	-	-
High Speed External (HSE)	O	O	O	O	-	-	-	-
Low Speed Internal (LSI)	O	O	O	O	O	-	O	-
Low Speed External (LSE)	O	O	O	O	O	-	O	-
Multi-Speed Internal (MSI)	O	O	Y	Y	-	-	-	-
Inter-Connect Controller	Y	Y	Y	Y	Y	-	-	-
RTC	O	O	O	O	O	O	O	-
RTC Tamper	O	O	O	O	O	O	O	O
Auto WakeUp (AWU)	O	O	O	O	O	-	O	O
USART	O	O	O	O	O[4]	O	-	-
LPUART	O	O	O	O	O[4]	O	-	-
SPI	O	O	O	O	-		-	-
I2C	O	O	O	O	O[5]	O	-	-
ADC	O	O	-	-	-	-	-	-
Temperature sensor	O	O	O	O	O	-	-	-
Comparators	O	O	O	O	O	O	-	-
16-bit timers	O	O	O	O	-	-	-	-
LPTIM	O	O	O	O	O	O	-	-
IWDG	O	O	O	O	O	O	O	O
WWDG	O	O	O	O	-	-	-	-
SysTick Timer	O	O	O	O	-	-	-	-
GPIOs	O	O	O	O	O	O	-	2 pins

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)(1)(2)

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
Wakeup time to Run mode	0 µs	6 CPU cycles	3 µs	7 CPU cycles	5 µs		65 µs	
Consumption V_{DD}=1.8 to 3.6 V (Typ)	Down to 128 µA/MHz (from Flash)	Down to 31 µA/MHz (from Flash)	Down to 7 µA	Down to 3.8 µA	0.29 µA (No RTC) V_{DD}=1.8 V		0.18 µA (No RTC) V_{DD}=1.8 V	
					0.54 µA (with RTC) V_{DD}=1.8 V		0.41 µA (with RTC) V_{DD}=1.8 V	
					0.34 µA (No RTC) V_{DD}=3.0 V		0.23 µA (No RTC) V_{DD}=3.0 V	
					0.67 µA (with RTC) V_{DD}=3.0 V		0.53 µA (with RTC) V_{DD}=3.0 V	

1. Legend:
   “Y” = Yes (enable).
   “O” = Optional, can be enabled/disabled by software)
   “-” = Not available
2. The consumption values given in this table are preliminary data given for indication. They are subject to slight changes.
3. Some peripherals with wakeup from Stop capability can request HSI to be enabled. In this case, HSI is woken up by the peripheral, and only feeds the peripheral which requested it. HSI is automatically put off when the peripheral does not need it anymore.
4. UART and LPUART reception is functional in Stop mode. It generates a wakeup interrupt on Start.To generate a wakeup on address match or received frame event, the LPUART can run on LSE clock while the UART has to wake up or keep running the HSI clock.
5. I2C address detection is functional in Stop mode. It generates a wakeup interrupt in case of address match. It will wake up the HSI during reception.

3.2 Interconnect matrix

Several peripherals are directly interconnected. This allows autonomous communication between peripherals, thus saving CPU resources and power consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, Low-power run, Low-power sleep and Stop modes.

Table 6. STM32L011x3/4 peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
COMPx	TIM2,TIM21	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	-
	LPTIM1	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	Y

Table 6. STM32L011x3/4 peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
TIMx	TIMx	Timer triggered by other timer	Y	Y	Y	Y	-
RTC	TIM21	Timer triggered by Auto wake-up	Y	Y	Y	Y	-
	LPTIM1	Timer triggered by RTC event	Y	Y	Y	Y	Y
All clock source	TIMx	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-
GPIO	TIMx	Timer input channel and trigger	Y	Y	Y	Y	-
	LPTIM1	Timer input channel and trigger	Y	Y	Y	Y	Y
	ADC	Conversion trigger	Y	Y	Y	Y	-

3.3 ARM® Cortex®-M0+ core

The Cortex-M0+ processor is an entry-level 32-bit ARM Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- a simple architecture that is easy to learn and program
- ultra-low power, energy-efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family
- platform security robustness.

The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to its embedded ARM core, the STM32L011x3/4 are compatible with all ARM tools and software.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L011x3/4 embed a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels and 4 priority levels.

The Cortex-M0+ processor closely integrates a configurable Nested Vectored Interrupt Controller (NVIC), to deliver industry-leading interrupt performance. The NVIC:

- includes a Non-Maskable Interrupt (NMI)
- provides zero jitter interrupt option
- provides four interrupt priority levels

The tight integration of the processor core and NVIC provides fast execution of Interrupt Service Routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to abandon and restart load-multiple and store-multiple operations. Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that include a deep sleep function that enables the entire device to enter rapidly stop or standby mode.

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.4 Reset and supply management

3.4.1 Power supply schemes

- V_{DD} = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively. On TSSOP14 package, V_{DDA} is internally connected to V_{DD}.

3.4.2 Power supply supervisor

The devices feature an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

Two versions are available:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the VDD min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The devices feature an embedded programmable voltage detector (PVD) that monitors the $V_{DD/VDDA}$ power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when $V_{DD/VDDA}$ drops below the V_{PVD} threshold and/or when $V_{DD/VDDA}$ is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.4.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32 KHz oscillator, RCC_CSR).

3.4.4 Boot modes

At startup, BOOT0 pin and nBOOT0, nBOOT1 and nBOOT_SEL option bits are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using SPI1 (PA4, PA7, PA13 and PA14 on TSSOP14 package or PA4, PA5, PA6 and PA7 on other packages) or USART2 (PA2, PA3 and PA9, PA10). See STM32™ microcontroller system memory boot mode AN2606 for details.

3.5 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**

  To get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.

- **Safe clock switching**

  Clock sources can be changed safely on the fly in Run mode through a configuration register.

- **Clock management**

  To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.

- **System clock source**

  Three different clock sources can be used to drive the master clock SYSCLK:

  – 0-32 MHz high-speed external (HSE bypass), that can supply a PLL
  – 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
  – Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz). When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.

- **Auxiliary clock source**

  Two ultra-low-power clock sources that can be used to drive the real-time clock:

  – 32.768 kHz low-speed external crystal (LSE)
  – 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.

- **RTC clock sources**

  The LSI, LSE or HSE sources can be chosen to clock the RTC, whatever the system clock.

- **Startup clock**

  After reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.

- **Clock security system (CSS)**

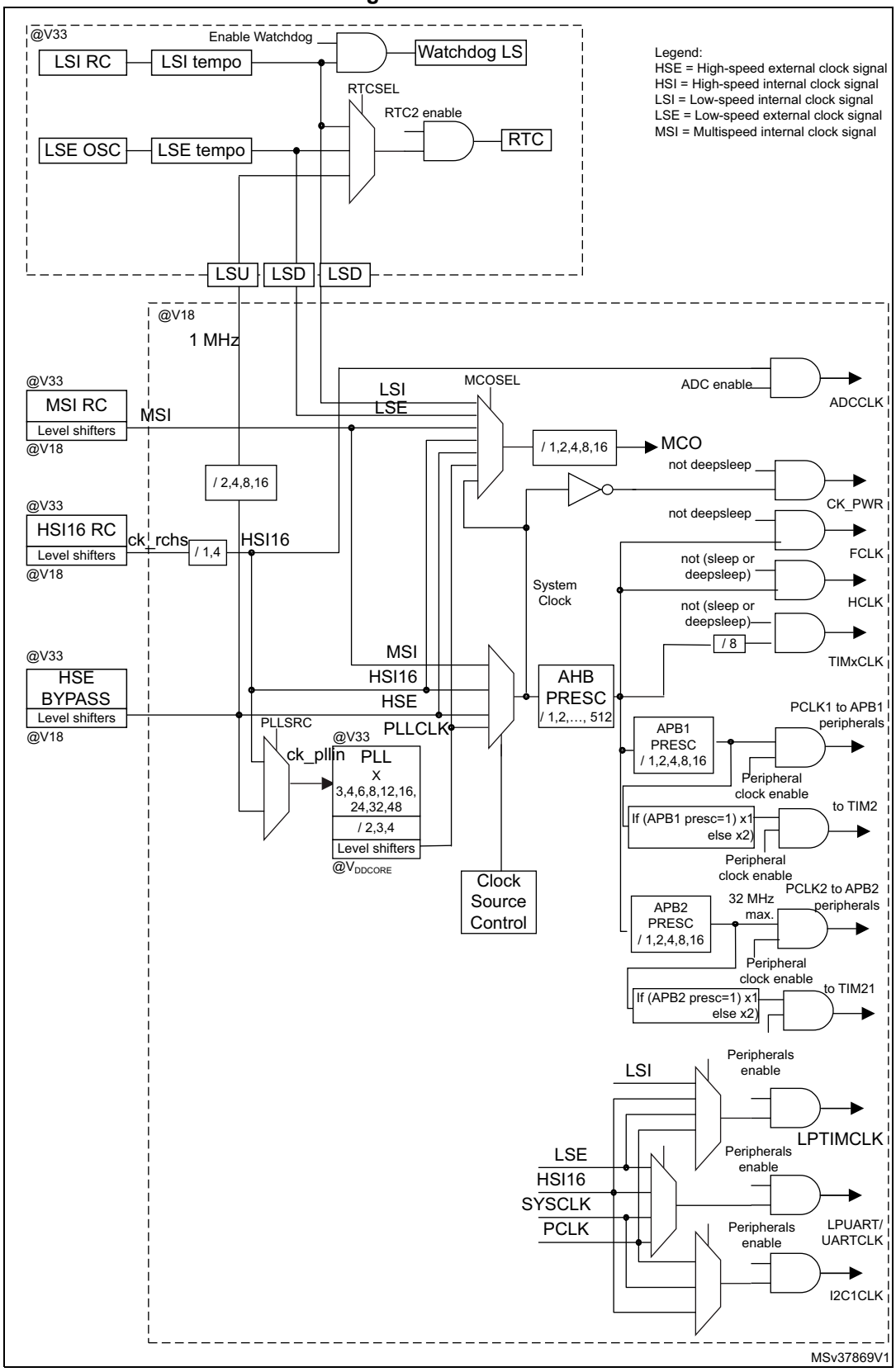
  This feature can be enabled by software. If an LSE clock failure occurs, it provides an interrupt or wakeup event which is generated assuming it has been previously enabled. This feature is not available on the HSE clock.

- **Clock-out capability (MCO: microcontroller clock output)**

  It outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

Figure 2. Clock tree



3.6 Low-power real-time clock and backup registers

The real time clock (RTC) and the 5 backup registers are supplied in all modes including standby mode. The backup registers are five 32-bit registers used to store 20 bytes of user application data. They are not reset by a system reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month
- Two programmable alarms with wake up from Stop and Standby mode capability
- Periodic wakeup from Stop and Standby with programmable resolution and period
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 37 kHz)
- The high-speed external clock

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated alternate function registers. All GPIOs are high current capable. Each GPIO output, speed can be slowed (40 MHz, 10 MHz, 2 MHz, 400 kHz). The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to a dedicated IO bus with a toggling speed of up to 32 MHz.

The BOOT0 pin is shared with PB9 GPIO pin. This pin is an input-only pin. If nBOOT_SEL option bit is reset, sampling this pin on NRST rising edge gives the internal BOOT0 state. This pin then works as PB9 pin. The input voltage characteristics of this pin are specific for BOOT0 pin type (see *Table 50: I/O static characteristics*).

Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 26 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event

(rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 38 GPIOs can be connected to the 16 configurable interrupt/event lines. The 10 other lines are connected to PVD, RTC, USART, I2C, LPUART, LPTIM or comparator events.

3.8 Memories

The STM32L011x3/4 devices have the following features:

- 2 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 8 or 16 Kbytes of embedded Flash program memory
  - 512 bytes of data EEPROM
  - Information block containing 32 user and factory options bytes plus 4 Kbytes of system memory

The user options bytes are used to write-protect or read-out protect the memory (with 4 Kbyte granularity) and/or readout-protect the whole memory with the following options:

- **Level 0**: no protection
- **Level 1**: memory readout protected.

  The Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- **Level 2**: chip readout protected, debug features (Cortex-M0+ serial wire) and boot in RAM selection disabled (debugline fuse)

The whole non-volatile memory embeds the error correction code (ECC) feature.

3.9 Direct memory access (DMA)

The flexible 5-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, LPUART, general-purpose timers, and ADC.