



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

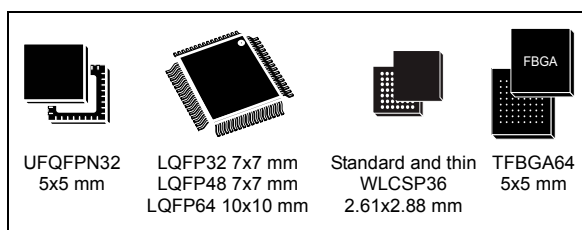


Access line ultra-low-power 32-bit MCU ARM[®]-based Cortex[®]-M0+, up to 64 KB Flash, 8 KB SRAM, 2 KB EEPROM, ADC

Datasheet - production data

Features

- Ultra-low-power platform
 - 1.65 V to 3.6 V power supply
 - -40 to 125 °C temperature range
 - 0.27 µA Standby mode (2 wakeup pins)
 - 0.4 µA Stop mode (16 wakeup lines)
 - 0.8 µA Stop mode + RTC + 8 KB RAM retention
 - 88 µA/MHz in Run mode
 - 3.5 µs wakeup time (from RAM)
 - 5 µs wakeup time (from Flash memory)
- Core: ARM[®] 32-bit Cortex[®]-M0+ with MPU
 - From 32 kHz up to 32 MHz max.
 - 0.95 DMIPS/MHz
- Reset and supply management
 - Ultra-safe, low-power BOR (brownout reset) with 5 selectable thresholds
 - Ultra-low-power POR/PDR
 - Programmable voltage detector (PVD)
- Clock sources
 - 1 to 25 MHz crystal oscillator
 - 32 kHz oscillator for RTC with calibration
 - High speed internal 16 MHz factory-trimmed RC (+/- 1%)
 - Internal low-power 37 kHz RC
 - Internal multispeed low-power 65 kHz to 4.2 MHz RC
 - PLL for CPU clock
- Pre-programmed bootloader
 - USART, SPI supported
- Development support
 - Serial wire debug supported
- Up to 51 fast I/Os (45 I/Os 5V tolerant)
- Memories
 - Up to 64 KB Flash memory with ECC
 - 8KB RAM
 - 2 KB of data EEPROM with ECC
 - 20-byte backup register
 - Sector protection against R/W operation



- Rich Analog peripherals
 - 12-bit ADC 1.14 Msps up to 16 channels (down to 1.65 V)
 - 2x ultra-low-power comparators (window mode and wake up capability, down to 1.65 V)
- 7-channel DMA controller, supporting ADC, SPI, I2C, USART, Timers
- 7x peripheral communication interfaces
 - 2x USART (ISO 7816, IrDA), 1x UART (low power)
 - Up to 4x SPI 16 Mbits/s
 - 2x I2C (SMBus/PMBus)
- 9x timers: 1x 16-bit with up to 4 channels, 2x 16-bit with up to 2 channels, 1x 16-bit ultra-low-power timer, 1x SysTick, 1x RTC, 1x 16-bit basic, and 2x watchdogs (independent/window)
- CRC calculation unit, 96-bit unique ID
- All packages are ECOPACK[®]2

Table 1. Device summary

Reference	Part number
STM32L051x6	STM32L051C6, STM32L051K6, STM32L051R6, STM32L051T6
STM32L051x8	STM32L051C8, STM32L051K8, STM32L051R8, STM32L051T8

Contents

1	Introduction	9
2	Description	10
2.1	Device overview	11
2.2	Ultra-low-power device continuum	13
3	Functional overview	14
3.1	Low-power modes	14
3.2	Interconnect matrix	18
3.3	ARM® Cortex®-M0+ core with MPU	19
3.4	Reset and supply management	20
3.4.1	Power supply schemes	20
3.4.2	Power supply supervisor	20
3.4.3	Voltage regulator	21
3.5	Clock management	21
3.6	Low-power real-time clock and backup registers	24
3.7	General-purpose inputs/outputs (GPIOs)	24
3.8	Memories	25
3.9	Boot modes	25
3.10	Direct memory access (DMA)	26
3.11	Analog-to-digital converter (ADC)	26
3.12	Temperature sensor	26
3.12.1	Internal voltage reference (V_{REFINT})	27
3.13	Ultra-low-power comparators and reference voltage	27
3.14	System configuration controller	28
3.15	Timers and watchdogs	28
3.15.1	General-purpose timers (TIM2, TIM21 and TIM22)	28
3.15.2	Low-power Timer (LPTIM)	29
3.15.3	Basic timer (TIM6)	29
3.15.4	SysTick timer	29
3.15.5	Independent watchdog (IWDG)	29
3.15.6	Window watchdog (WWDG)	29

3.16 Communication interfaces 30

 3.16.1 I2C bus 30

 3.16.2 Universal synchronous/asynchronous receiver transmitter (USART) .. 31

 3.16.3 Low-power universal asynchronous receiver transmitter (LPUART) ... 31

 3.16.4 Serial peripheral interface (SPI)/Inter-integrated sound (I2S) 32

3.17 Cyclic redundancy check (CRC) calculation unit 32

3.18 Serial wire debug port (SW-DP) 32

4 Pin descriptions 33

5 Memory mapping 46

6 Electrical characteristics 47

 6.1 Parameter conditions 47

 6.1.1 Minimum and maximum values 47

 6.1.2 Typical values 47

 6.1.3 Typical curves 47

 6.1.4 Loading capacitor 47

 6.1.5 Pin input voltage 47

 6.1.6 Power supply scheme 48

 6.1.7 Current consumption measurement 48

 6.2 Absolute maximum ratings 49

 6.3 Operating conditions 51

 6.3.1 General operating conditions 51

 6.3.2 Embedded reset and power control block characteristics 53

 6.3.3 Embedded internal reference voltage 54

 6.3.4 Supply current characteristics 55

 6.3.5 Wakeup time from low-power mode 66

 6.3.6 External clock source characteristics 67

 6.3.7 Internal clock source characteristics 71

 6.3.8 PLL characteristics 74

 6.3.9 Memory characteristics 74

 6.3.10 EMC characteristics 76

 6.3.11 Electrical sensitivity characteristics 78

 6.3.12 I/O current injection characteristics 79

 6.3.13 I/O port characteristics 80

 6.3.14 NRST pin characteristics 84

	6.3.15	12-bit ADC characteristics	85
	6.3.16	Temperature sensor characteristics	90
	6.3.17	Comparators	91
	6.3.18	Timer characteristics	92
	6.3.19	Communications interfaces	92
7		Package information	101
	7.1	LQFP64 package information	101
	7.2	TFBGA64 package information	105
	7.3	LQFP48 package information	108
	7.4	Standard WLCSP36 package information	111
	7.5	Thin WLCSP36 package information	114
	7.6	LQFP32 package information	116
	7.7	UFQFPN32 package information	119
	7.8	Thermal characteristics	122
	7.8.1	Reference document	123
8		Part numbering	124
9		Revision history	125

List of tables

Table 1.	Device summary	1
Table 2.	Ultra-low-power STM32L051x6/x8 device features and peripheral counts.	11
Table 3.	Functionalities depending on the operating power supply range	15
Table 5.	Functionalities depending on the working mode (from Run/active down to standby)	16
Table 4.	CPU frequency range depending on dynamic voltage scaling	16
Table 6.	STM32L0xx peripherals interconnect matrix	18
Table 7.	Temperature sensor calibration values.	27
Table 8.	Internal voltage reference measured values.	27
Table 9.	Timer feature comparison.	28
Table 10.	Comparison of I2C analog and digital filters.	30
Table 11.	STM32L051x6/8 I ² C implementation	30
Table 12.	USART implementation	31
Table 13.	SPI/I2S implementation	32
Table 14.	Legend/abbreviations used in the pinout table	37
Table 15.	STM32L051x6/8 pin definitions	37
Table 16.	Alternate function port A	43
Table 17.	Alternate function port B	44
Table 18.	Alternate function port C	45
Table 19.	Alternate function port D	45
Table 20.	Voltage characteristics	49
Table 21.	Current characteristics	50
Table 22.	Thermal characteristics.	50
Table 23.	General operating conditions	51
Table 24.	Embedded reset and power control block characteristics.	53
Table 25.	Embedded internal reference voltage calibration values	54
Table 26.	Embedded internal reference voltage.	54
Table 27.	Current consumption in Run mode, code with data processing running from Flash.	56
Table 28.	Current consumption in Run mode vs code type, code with data processing running from Flash	56
Table 29.	Current consumption in Run mode, code with data processing running from RAM	58
Table 30.	Current consumption in Run mode vs code type, code with data processing running from RAM	58
Table 31.	Current consumption in Sleep mode	59
Table 32.	Current consumption in Low-power run mode	60
Table 33.	Current consumption in Low-power sleep mode	61
Table 34.	Typical and maximum current consumptions in Stop mode	62
Table 35.	Typical and maximum current consumptions in Standby mode	63
Table 36.	Average current consumption during Wakeup	63
Table 37.	Peripheral current consumption in Run or Sleep mode	64
Table 38.	Peripheral current consumption in Stop and Standby mode	65
Table 39.	Low-power mode wakeup timings	66
Table 40.	High-speed external user clock characteristics.	67
Table 41.	Low-speed external user clock characteristics	68
Table 42.	HSE oscillator characteristics	69
Table 43.	LSE oscillator characteristics	70
Table 44.	16 MHz HSI16 oscillator characteristics	71
Table 45.	LSI oscillator characteristics	72

Table 46.	MSI oscillator characteristics	72
Table 47.	PLL characteristics	74
Table 48.	RAM and hardware registers	74
Table 49.	Flash memory and data EEPROM characteristics	74
Table 50.	Flash memory and data EEPROM endurance and retention	75
Table 51.	EMS characteristics	76
Table 52.	EMI characteristics	77
Table 53.	ESD absolute maximum ratings	78
Table 54.	Electrical sensitivities	78
Table 55.	I/O current injection susceptibility	79
Table 56.	I/O static characteristics	80
Table 57.	Output voltage characteristics	82
Table 58.	I/O AC characteristics	83
Table 59.	NRST pin characteristics	84
Table 60.	ADC characteristics	85
Table 61.	R_{AIN} max for $f_{ADC} = 16$ MHz	87
Table 62.	ADC accuracy	87
Table 63.	Temperature sensor calibration values	90
Table 64.	Temperature sensor characteristics	90
Table 65.	Comparator 1 characteristics	91
Table 66.	Comparator 2 characteristics	91
Table 67.	TIMx characteristics	92
Table 68.	I2C analog filter characteristics	93
Table 69.	USART/LPUART characteristics	93
Table 70.	SPI characteristics in voltage Range 1	94
Table 71.	SPI characteristics in voltage Range 2	95
Table 72.	SPI characteristics in voltage Range 3	96
Table 73.	I2S characteristics	99
Table 74.	LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data	102
Table 75.	TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data	105
Table 76.	TFBGA64 recommended PCB design rules (0.5 mm pitch BGA)	106
Table 77.	LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data	109
Table 78.	Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale mechanical data	111
Table 79.	Standard WLCSP36 recommended PCB design rules	112
Table 80.	Thin WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale package mechanical data	115
Table 81.	WLCSP36 recommended PCB design rules	116
Table 82.	LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data	117
Table 83.	UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data	120
Table 84.	Thermal characteristics	122
Table 85.	STM32L051x6/8 ordering information scheme	124
Table 86.	Document revision history	125

List of figures

Figure 1.	STM32L051x6/8 block diagram	12
Figure 2.	Clock tree	23
Figure 3.	STM32L051x6/8 LQFP64 pinout - 10 x 10 mm	33
Figure 4.	STM32L051x6/8 TFBGA64 ballout - 5x 5 mm	34
Figure 5.	STM32L051x6/8 LQFP48 pinout - 7 x 7 mm	35
Figure 6.	STM32L051x6/8 WLCSP36 ballout	35
Figure 7.	STM32L051x6/8 LQFP32 pinout	36
Figure 8.	STM32L051x6/8 UFQFPN32 pinout	36
Figure 9.	Memory map	46
Figure 10.	Pin loading conditions	47
Figure 11.	Pin input voltage	47
Figure 12.	Power supply scheme	48
Figure 13.	Current consumption measurement scheme	48
Figure 14.	IDD vs VDD, at TA= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSE, 1WS	57
Figure 15.	IDD vs VDD, at TA= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSI16, 1WS	57
Figure 16.	IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS	61
Figure 17.	IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive	62
Figure 18.	IDD vs VDD, at TA= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks OFF	62
Figure 19.	High-speed external clock source AC timing diagram	67
Figure 20.	Low-speed external clock source AC timing diagram	68
Figure 21.	HSE oscillator circuit diagram	69
Figure 22.	Typical application with a 32.768 kHz crystal	70
Figure 23.	HSI16 minimum and maximum value versus temperature	71
Figure 24.	VIH/VIL versus VDD (CMOS I/Os)	81
Figure 25.	VIH/VIL versus VDD (TTL I/Os)	81
Figure 26.	I/O AC characteristics definition	84
Figure 27.	Recommended NRST pin protection	85
Figure 28.	ADC accuracy characteristics	88
Figure 29.	Typical connection diagram using the ADC	89
Figure 30.	Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})	89
Figure 31.	Power supply and reference decoupling (V_{REF+} connected to V_{DDA})	90
Figure 32.	SPI timing diagram - slave mode and CPHA = 0	97
Figure 33.	SPI timing diagram - slave mode and CPHA = 1 ⁽¹⁾	97
Figure 34.	SPI timing diagram - master mode ⁽¹⁾	98
Figure 35.	I ² S slave timing diagram (Philips protocol) ⁽¹⁾	100
Figure 36.	I ² S master timing diagram (Philips protocol) ⁽¹⁾	100
Figure 37.	LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline	101
Figure 38.	LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint	103
Figure 39.	LQFP64 marking example (package top view)	104
Figure 40.	TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch thin profile fine pitch ball grid array package outline	105
Figure 41.	TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball ,grid array recommended footprint	106

Figure 42.	TFBGA64 marking example (package top view)	107
Figure 43.	LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline	108
Figure 44.	LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint	109
Figure 45.	LQFP48 marking example (package top view)	110
Figure 46.	Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale package outline.	111
Figure 47.	Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale recommended footprint.	112
Figure 48.	Standard WLCSP36 marking example (package top view)	113
Figure 49.	Thin WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale package outline.	114
Figure 50.	Thin WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale package recommended footprint	115
Figure 51.	LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline	116
Figure 52.	LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat recommended footprint	117
Figure 53.	LQFP32 marking example (package top view)	118
Figure 54.	UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline.	119
Figure 55.	UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat recommended footprint.	120
Figure 56.	UFQFPN32 marking example (package top view)	121
Figure 57.	Thermal resistance	123

1 Introduction

The ultra-low-power STM32L051x6/8 are offered in 7 different package types: from 32 pins to 64 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L051x6/8 microcontrollers suitable for a wide range of applications:

- Gas/water meters and industrial sensors
- Healthcare and fitness equipment
- Remote control and user interface
- PC peripherals, gaming, GPS equipment
- Alarm system, wired and wireless sensors, video intercom

This STM32L051x6/8 datasheet should be read in conjunction with the STM32L0x1xx reference manual (RM0377).

For information on the ARM® Cortex®-M0+ core please refer to the Cortex®-M0+ Technical Reference Manual, available from the www.arm.com website.

Figure 1 shows the general block diagram of the device family.

2 Description

The access line ultra-low-power STM32L051x6/8 microcontrollers incorporate the high-performance ARM® Cortex®-M0+ 32-bit RISC core operating at a 32 MHz frequency, a memory protection unit (MPU), high-speed embedded memories (64 Kbytes of Flash program memory, 2 Kbytes of data EEPROM and 8 Kbytes of RAM) plus an extensive range of enhanced I/Os and peripherals.

The STM32L051x6/8 devices provide high power efficiency for a wide range of performance. It is achieved with a large choice of internal and external clock sources, an internal voltage adaptation and several low-power modes.

The STM32L051x6/8 devices offer several analog features, one 12-bit ADC with hardware oversampling, two ultra-low-power comparators, several timers, one low-power timer (LPTIM), three general-purpose 16-bit timers and one basic timer, one RTC and one SysTick which can be used as timebases. They also feature two watchdogs, one watchdog with independent clock and window capability and one window watchdog based on bus clock.

Moreover, the STM32L051x6/8 devices embed standard and advanced communication interfaces: up to two I2C, two SPIs, one I2S, two USARTs, a low-power UART (LPUART), .

The STM32L051x6/8 also include a real-time clock and a set of backup registers that remain powered in Standby mode.

The ultra-low-power STM32L051x6/8 devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +125 °C temperature range. A comprehensive set of power-saving modes allows the design of low-power applications.



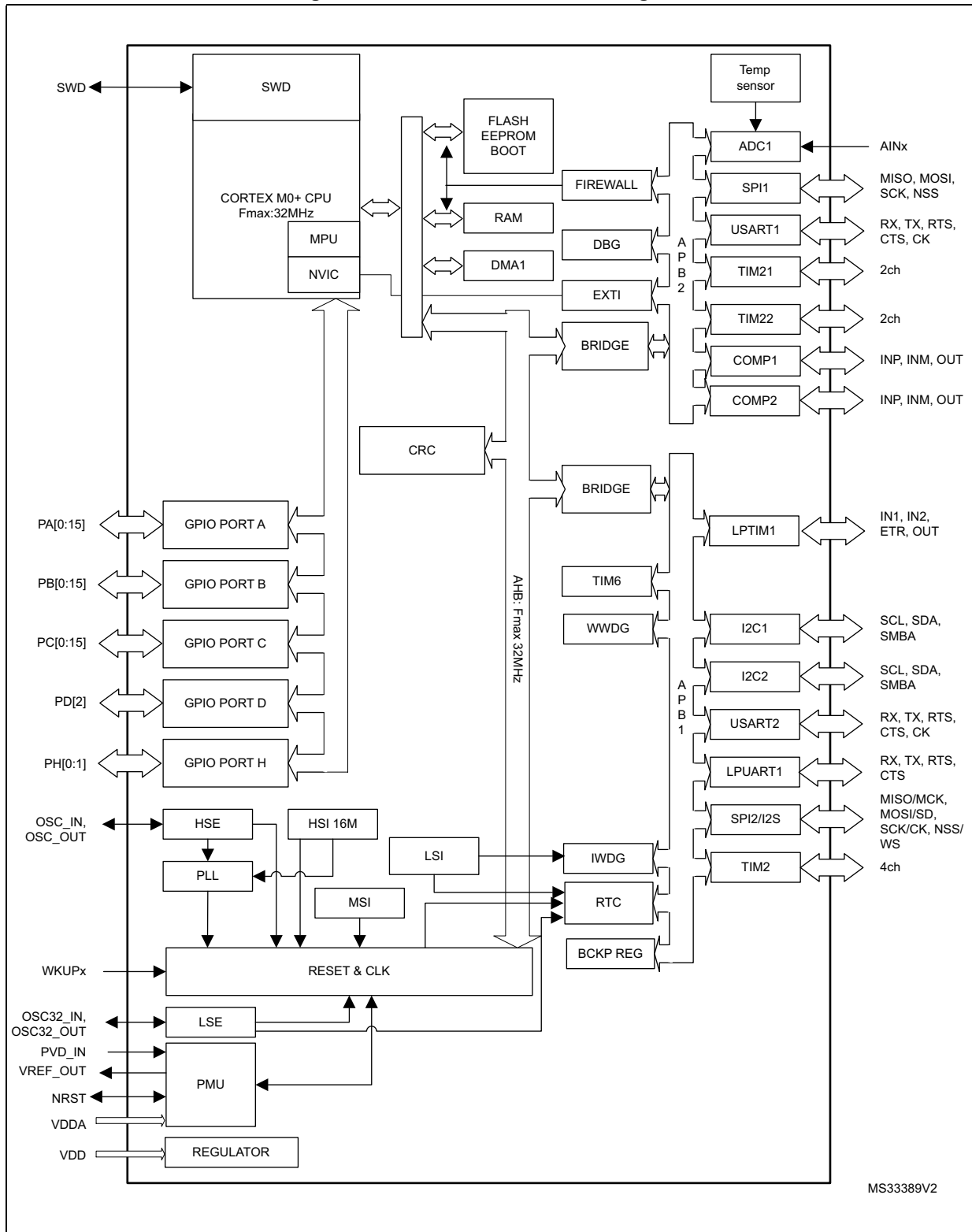
2.1 Device overview

Table 2. Ultra-low-power STM32L051x6/x8 device features and peripheral counts

Peripheral		STM32 L051K6	STM32L051T6	STM32 L051C6	STM32 L051R6	STM32 L051K8	STM32L051T8	STM32 L051C8	STM32 L051R8
Flash (Kbytes)		32				64			
Data EEPROM (Kbytes)		2				2			
RAM (Kbytes)		8				8			
Timers	General-purpose	3				3			
	Basic	1				1			
	LPTIMER	1				1			
RTC/SYSTICK/IWDG/ WWDG		1/1/1/1				1/1/1/1			
Communication interfaces	SPI/I2S	3(2) ⁽¹⁾ /0	3(2) ⁽¹⁾ /0	4(2) ⁽¹⁾ /1	4(2) ⁽¹⁾ /1	3(2) ⁽¹⁾ /0	3(2) ⁽¹⁾ /0	4(2) ⁽¹⁾ /1	4(2) ⁽¹⁾ /1
	I ² C	1	2	2	2	1	2	2	2
	USART	2				2			
	LPUART	0	1	1	1	0	1	1	1
GPIOs		27 ⁽²⁾	29	37	51 ⁽³⁾	27 ⁽²⁾	29	37	51 ⁽³⁾
Clocks: HSE/LSE/HSI/MSI/LSI		0/1/1/1/1	0/1/1/1/1	1/1/1/1/1	1/1/1/1/1	0/1/1/1/1	0/1/1/1/1	1/1/1/1/1	1/1/1/1/1
12-bit synchronized ADC Number of channels		1 10	1 10	1 10	1 16 ⁽³⁾	1 10	1 10	1 10	1 16 ⁽³⁾
Comparators		2				2			
Max. CPU frequency		32 MHz							
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V without BOR option							
Operating temperatures		Ambient temperature: -40 to +125 °C Junction temperature: -40 to +130 °C							
Packages		LQFP32, UFQFPN 32	WLCSP 36	LQFP48	LQFP64 TFBGA 64	LQFP32, UFQFPN 32	WLCSP 36	LQFP48	LQFP64 TFBGA 64

- 2 SPI interfaces are USARTs operating in SPI master mode.
- LQFP32 has two GPIOs, less than UFQFPN32 (27).
- TFBGA64 has one GPIO, one ADC input and one capacitive sensing channel less than LQFP64.

Figure 1. STM32L051x6/8 block diagram



2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of core and features, from 8-bit proprietary core up to ARM® Cortex®-M4, including ARM® Cortex®-M3 and ARM® Cortex®-M0+. The STM32Lx series are the best choice to answer your needs in terms of ultra-low-power features. The STM32 ultra-low-power series are the best solution for applications such as gaz/water meter, keyboard/mouse or fitness and healthcare application. Several built-in features like LCD drivers, dual-bank memory, low-power run mode, operational amplifiers, 128-bit AES, DAC, crystal-less USB and many other definitely help you building a highly cost optimized application by reducing BOM cost. STMicroelectronics, as a reliable and long-term manufacturer, ensures as much as possible pin-to-pin compatibility between all STM8Lx and STM32Lx on one hand, and between all STM32Lx and STM32Fx on the other hand. Thanks to this unprecedented scalability, your legacy application can be upgraded to respond to the latest market feature and efficiency requirements.

3 Functional overview

3.1 Low-power modes

The ultra-low-power STM32L051x6/8 support dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 (V_{DD} range limited to 1.71-3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full V_{DD} range), with a maximum CPU frequency of 16 MHz
- Range 3 (full V_{DD} range), with a maximum CPU frequency limited to 4.2 MHz

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

- **Low-power run mode**

This mode is achieved with the multispeed internal (MSI) RC oscillator set to the low-speed clock (max 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In Low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

- **Low-power sleep mode**

This mode is achieved by entering Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

When wakeup is triggered by an event or an interrupt, the system reverts to the Run mode with the regulator on.

- **Stop mode with RTC**

The Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSE crystal and HSI RC oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

The device can be woken up from Stop mode by any of the EXTI line, in 3.5 μ s, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on), it can be the RTC alarm/tamper/timestamp/wakeup events, the USART/I2C/LPUART/LPTIMER wakeup events.

- **Stop mode without RTC**

The Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are disabled.

Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 3.5 μ s, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on). It can also be wakened by the USART/I2C/LPUART/LPTIMER wakeup events.

- **Standby mode with RTC**

The Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSE crystal and HSI RC oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

The device exits Standby mode in 60 μ s when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby mode without RTC**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

The device exits Standby mode in 60 μ s when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

Operating power supply range	Functionalities depending on the operating power supply range		
	ADC operation	Dynamic voltage scaling range	I/O operation
$V_{DD} = 1.65$ to 1.71 V	ADC only, conversion time up to 570 ksps	Range 2 or range 3	Degraded speed performance
$V_{DD} = 1.71$ to 1.8 V ⁽¹⁾	ADC only, conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Degraded speed performance
$V_{DD} = 1.8$ to 2.0 V ⁽¹⁾	Conversion time up to 1.14 Msps	Range1, range 2 or range 3	Degraded speed performance

Table 3. Functionalities depending on the operating power supply range (continued)

Operating power supply range	Functionalities depending on the operating power supply range		
	ADC operation	Dynamic voltage scaling range	I/O operation
V _{DD} = 2.0 to 2.4 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation
V _{DD} = 2.4 to 3.6 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation

1. CPU frequency changes from initial to final must respect "fcpu initial <4*fcpu final". It must also respect 5 μs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5 μs, then switch from 16 MHz to 32 MHz.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
32 kHz to 4.2 MHz (0ws)	Range 3

Table 5. Functionalities depending on the working mode (from Run/active down to standby) ⁽¹⁾

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
					Wakeup capability	Wakeup capability		
CPU	Y	--	Y	--	--		--	
Flash memory	O	O	O	O	--		--	
RAM	Y	Y	Y	Y	Y		--	
Backup registers	Y	Y	Y	Y	Y		Y	
EEPROM	O	O	O	O	--		--	
Brown-out reset (BOR)	O	O	O	O	O	O	O	O
DMA	O	O	O	O	--		--	
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	-	
Power-on/down reset (POR/PDR)	Y	Y	Y	Y	Y	Y	Y	Y
High Speed Internal (HSI)	O	O	--	--	(2)		--	

Table 5. Functionalities depending on the working mode (from Run/active down to standby)⁽¹⁾

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
					Wakeup capability	Wakeup capability		
High Speed External (HSE)	O	O	O	O	--		--	
Low Speed Internal (LSI)	O	O	O	O	O		O	
Low Speed External (LSE)	O	O	O	O	O		O	
Multi-Speed Internal (MSI)	O	O	Y	Y	--		--	
Inter-Connect Controller	Y	Y	Y	Y	Y		--	
RTC	O	O	O	O	O	O	O	
RTC Tamper	O	O	O	O	O	O	O	O
Auto WakeUp (AWU)	O	O	O	O	O	O	O	O
USART	O	O	O	O	O ⁽³⁾	O	--	
LPUART	O	O	O	O	O ⁽³⁾	O	--	
SPI	O	O	O	O	--		--	
I2C	O	O	O	O	O ⁽⁴⁾	O	--	
ADC	O	O	--	--	--		--	
Temperature sensor	O	O	O	O	O		--	
Comparators	O	O	O	O	O	O	--	
16-bit timers	O	O	O	O	--		--	
LPTIMER	O	O	O	O	O	O		
IWDG	O	O	O	O	O	O	O	O
WWDG	O	O	O	O	--		--	
SysTick Timer	O	O	O	O			--	
GPIOs	O	O	O	O	O	O		2 pins
Wakeup time to Run mode	0 μs	0.36 μs	3 μs	32 μs	3.5 μs		50 μs	

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)⁽¹⁾

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop	Standby
					Wakeup capability	Wakeup capability
Consumption V _{DD} =1.8 to 3.6 V (Typ)	Down to 140 µA/MHz (from Flash memory)	Down to 37 µA/MHz (from Flash memory)	Down to 8 µA	Down to 4.5 µA	0.4 µA (No RTC) V _{DD} =1.8 V	0.28 µA (No RTC) V _{DD} =1.8 V
					0.8 µA (with RTC) V _{DD} =1.8 V	0.65 µA (with RTC) V _{DD} =1.8 V
					0.4 µA (No RTC) V _{DD} =3.0 V	0.29 µA (No RTC) V _{DD} =3.0 V
					1 µA (with RTC) V _{DD} =3.0 V	0.85 µA (with RTC) V _{DD} =3.0 V

- Legend:
 "Y" = Yes (enable).
 "O" = Optional can be enabled/disabled by software)
 "-" = Not available
- Some peripherals with wakeup from Stop capability can request HSI to be enabled. In this case, HSI is woken up by the peripheral, and only feeds the peripheral which requested it. HSI is automatically put off when the peripheral does not need it anymore.
- UART and LPUART reception is functional in Stop mode. It generates a wakeup interrupt on Start. To generate a wakeup on address match or received frame event, the LPUART can run on LSE clock while the UART has to wake up or keep running the HSI clock.
- I2C address detection is functional in Stop mode. It generates a wakeup interrupt in case of address match. It will wake up the HSI during reception.

3.2 Interconnect matrix

Several peripherals are directly interconnected. This allows autonomous communication between peripherals, thus saving CPU resources and power consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, Low-power run, Low-power sleep and Stop modes.

Table 6. STM32L0xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
COMPx	TIM2, TIM21, TIM22	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	-
	LPTIM	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	Y
TIMx	TIMx	Timer triggered by other timer	Y	Y	Y	Y	-

Table 6. STM32L0xx peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
RTC	TIM21	Timer triggered by Auto wake-up	Y	Y	Y	Y	-
	LPTIM	Timer triggered by RTC event	Y	Y	Y	Y	Y
All clock source	TIMx	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-
GPIO	TIMx	Timer input channel and trigger	Y	Y	Y	Y	-
	LPTIM	Timer input channel and trigger	Y	Y	Y	Y	Y
	ADC	Conversion trigger	Y	Y	Y	Y	-

3.3 ARM[®] Cortex[®]-M0+ core with MPU

The Cortex-M0+ processor is an entry-level 32-bit ARM Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- a simple architecture that is easy to learn and program
- ultra-low power, energy-efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family
- platform security robustness, with integrated Memory Protection Unit (MPU).

The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to its embedded ARM core, the STM32L051x6/8 are compatible with all ARM tools and software.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L051x6/8 embed a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels and 4 priority levels.

The Cortex-M0+ processor closely integrates a configurable Nested Vectored Interrupt Controller (NVIC), to deliver industry-leading interrupt performance. The NVIC:

- includes a Non-Maskable Interrupt (NMI)
- provides zero jitter interrupt option
- provides four interrupt priority levels

The tight integration of the processor core and NVIC provides fast execution of Interrupt Service Routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to abandon and restart load-multiple and store-multiple operations. Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that include a deep sleep function that enables the entire device to enter rapidly stop or standby mode.

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.4 Reset and supply management

3.4.1 Power supply schemes

- $V_{DD} = 1.65$ to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- $V_{SSA}, V_{DDA} = 1.65$ to 3.6 V: external analog power supplies for ADC reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.

3.4.2 Power supply supervisor

The devices have an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

Two versions are available:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the V_{DD} min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the

internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The devices feature an embedded programmable voltage detector (PVD) that monitors the $V_{DD/VDDA}$ power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when $V_{DD/VDDA}$ drops below the V_{PVD} threshold and/or when $V_{DD/VDDA}$ is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.4.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wake-up logic, IWDG, RTC, LSI, LSE crystal 32 KHz oscillator, RCC_CSR).

3.5 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**
To get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching**
Clock sources can be changed safely on the fly in Run mode through a configuration register.
- **Clock management**
To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source**
Three different clock sources can be used to drive the master clock SYSCLK:
 - 1-25 MHz high-speed external crystal (HSE), that can supply a PLL
 - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLLMultispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz). When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a $\pm 0.5\%$ accuracy.
- **Auxiliary clock source**
Two ultra-low-power clock sources that can be used to drive the real-time clock:

- 32.768 kHz low-speed external crystal (LSE)
- 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- **RTC clock source**

The LSI, LSE or HSE sources can be chosen to clock the RTC, whatever the system clock.
- **Startup clock**

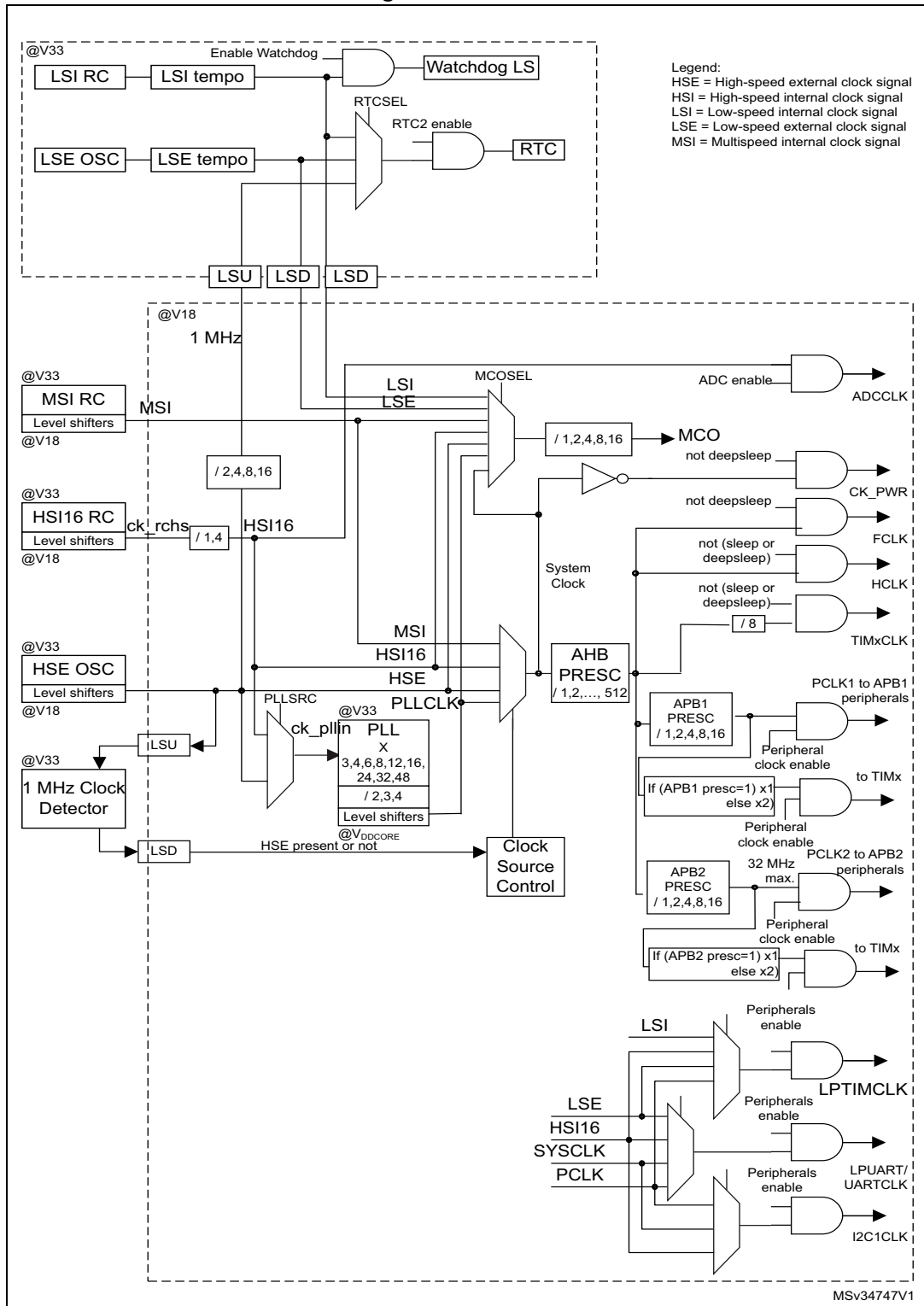
After reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS)**

This feature can be enabled by software. If an HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled. Another clock security system can be enabled, in case of failure of the LSE it provides an interrupt or wakeup event which is generated if enabled.
- **Clock-out capability (MCO: microcontroller clock output)**

It outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See [Figure 2](#) for details on the clock tree.

Figure 2. Clock tree



3.6 Low-power real-time clock and backup registers

The real time clock (RTC) and the 5 backup registers are supplied in all modes including standby mode. The backup registers are five 32-bit registers used to store 20 bytes of user application data. They are not reset by a system reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month
- Two programmable alarms with wake up from Stop and Standby mode capability
- Periodic wakeup from Stop and Standby with programmable resolution and period
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 37 kHz)
- The high-speed external clock

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated alternate function registers. All GPIOs are high current capable. Each GPIO output, speed can be slowed (40 MHz, 10 MHz, 2 MHz, 400 kHz). The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to a dedicated IO bus with a toggling speed of up to 32 MHz.

Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 28 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 51 GPIOs can be connected to the 16 configurable interrupt/event lines. The 12 other lines are connected to PVD, RTC, USARTs, LPUART, LPTIMER or comparator events.

3.8 Memories

The STM32L051x6/8 devices have the following features:

- 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
 - 32 or 64 Kbytes of embedded Flash program memory
 - 2 Kbytes of data EEPROM
 - Information block containing 32 user and factory options bytes plus 4 Kbytes of system memory

The user options bytes are used to write-protect or read-out protect the memory (with 4 Kbyte granularity) and/or readout-protect the whole memory with the following options:

- **Level 0:** no protection
- **Level 1:** memory readout protected.
The Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- **Level 2:** chip readout protected, debug features (Cortex-M0+ serial wire) and boot in RAM selection disabled (debugline fuse)

The firewall protects parts of code/data from access by the rest of the code that is executed outside of the protected area. The granularity of the protected code segment or the non-volatile data segment is 256 bytes (Flash memory or EEPROM) against 64 bytes for the volatile data segment (RAM).

The whole non-volatile memory embeds the error correction code (ECC) feature.

3.9 Boot modes

At startup, BOOT0 pin and nBOOT1 option bit are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using SPI1 (PA4, PA5, PA6, PA7) or SPI2 (PB12, PB13, PB14, PB15), USART1 (PA9, PA10) or USART2 (PA2, PA3). See STM32™ microcontroller system memory boot mode AN2606 for details.