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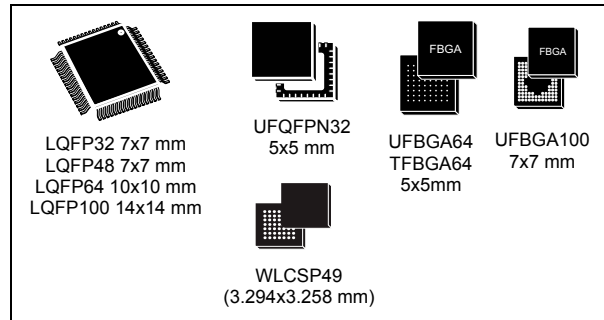


Access line ultra-low-power 32-bit MCU ARM[®]-based Cortex[®]-M0+,
up to 192KB Flash, 20KB SRAM, 6KB EEPROM, ADC

Datasheet - production data

Features

- Ultra-low-power platform
 - 1.65 V to 3.6 V power supply
 - -40 to 125 °C temperature range
 - 0.29 µA Standby mode (3 wakeup pins)
 - 0.43 µA Stop mode (16 wakeup lines)
 - 0.86 µA Stop mode + RTC + 20 KB RAM retention
 - Down to 93 µA/MHz in Run mode
 - 5 µs wakeup time (from Flash memory)
 - 41 µA 12-bit ADC conversion at 10 ksp/s
- Core: ARM[®] 32-bit Cortex[®]-M0+ with MPU
 - From 32 kHz up to 32 MHz max.
 - 0.95 DMIPS/MHz
- Reset and supply management
 - Ultra-safe, low-power BOR (brownout reset) with 5 selectable thresholds
 - Ultra-low-power POR/PDR
 - Programmable voltage detector (PVD)
- Clock sources
 - 1 to 25 MHz crystal oscillator
 - 32 kHz oscillator for RTC with calibration
 - High speed internal 16 MHz factory-trimmed RC (+/- 1%)
 - Internal low-power 37 kHz RC
 - Internal multispeed low-power 65 kHz to 4.2 MHz RC
 - PLL for CPU clock
- Pre-programmed bootloader
 - USART, I2C, SPI supported
- Development support
 - Serial wire debug supported
- Up to 84 fast I/Os (78 I/Os 5V tolerant)
- Memories
 - Up to 192 KB Flash memory with ECC(2 banks with read-while-write capability)
 - 20 KB RAM
 - 6 KB of data EEPROM with ECC
 - 20-byte backup register
 - Sector protection against R/W operation



- Rich Analog peripherals
 - 12-bit ADC 1.14 Msps up to 16 channels (down to 1.65 V)
 - 2x ultra-low-power comparators (window mode and wake up capability, down to 1.65 V)
- 7-channel DMA controller, supporting ADC, SPI, I2C, USART, Timers
- 10x peripheral communication interfaces
 - 4x USART (2 with ISO 7816, IrDA), 1x UART (low power)
 - Up to 6x SPI 16 Mbits/s
 - 3x I2C (2 with SMBus/PMBus)
- 11x timers: 2x 16-bit with up to 4 channels, 2x 16-bit with up to 2 channels, 1x 16-bit ultra-low-power timer, 1x SysTick, 1x RTC, 2x 16-bit basic, and 2x watchdogs (independent/window)
- CRC calculation unit, 96-bit unique ID
- All packages are ECOPACK^{®2}

Table 1. Device summary

Reference	Part number
STM32L071x8	STM32L071V8, STM32L071K8, STM32L071C8
STM32L071xB	STM32L071VB, STM32L071RB, STM32L071CB, STM32L071KB
STM32L071xZ	STM32L071VZ, STM32L071RZ, STM32L071CZ, STM32L071KZ

Contents

1	Introduction	9
2	Description	10
2.1	Device overview	11
2.2	Ultra-low-power device continuum	13
3	Functional overview	14
3.1	Low-power modes	14
3.2	Interconnect matrix	18
3.3	ARM® Cortex®-M0+ core with MPU	19
3.4	Reset and supply management	20
3.4.1	Power supply schemes	20
3.4.2	Power supply supervisor	20
3.4.3	Voltage regulator	21
3.5	Clock management	21
3.6	Low-power real-time clock and backup registers	24
3.7	General-purpose inputs/outputs (GPIOs)	24
3.8	Memories	25
3.9	Boot modes	25
3.10	Direct memory access (DMA)	26
3.11	Analog-to-digital converter (ADC)	26
3.12	Temperature sensor	26
3.12.1	Internal voltage reference (V_{REFINT})	27
3.13	Ultra-low-power comparators and reference voltage	27
3.14	Timers and watchdogs	28
3.14.1	General-purpose timers (TIM2, TIM3, TIM21 and TIM22)	28
3.14.2	Low-power Timer (LPTIM)	29
3.14.3	Basic timer (TIM6, TIM7)	29
3.14.4	SysTick timer	29
3.14.5	Independent watchdog (IWDG)	29
3.14.6	Window watchdog (WWDG)	29
3.15	Communication interfaces	30

3.15.1	I2C bus	30
3.15.2	Universal synchronous/asynchronous receiver transmitter (USART)	31
3.15.3	Low-power universal asynchronous receiver transmitter (LPUART)	31
3.15.4	Serial peripheral interface (SPI)/Inter-integrated sound (I2S)	32
3.16	Cyclic redundancy check (CRC) calculation unit	32
3.17	Serial wire debug port (SW-DP)	32
4	Pin descriptions	33
5	Memory mapping	52
6	Electrical characteristics	53
6.1	Parameter conditions	53
6.1.1	Minimum and maximum values	53
6.1.2	Typical values	53
6.1.3	Typical curves	53
6.1.4	Loading capacitor	53
6.1.5	Pin input voltage	53
6.1.6	Power supply scheme	54
6.1.7	Current consumption measurement	54
6.2	Absolute maximum ratings	55
6.3	Operating conditions	57
6.3.1	General operating conditions	57
6.3.2	Embedded reset and power control block characteristics	59
6.3.3	Embedded internal reference voltage	60
6.3.4	Supply current characteristics	61
6.3.5	Wakeup time from low-power mode	73
6.3.6	External clock source characteristics	75
6.3.7	Internal clock source characteristics	79
6.3.8	PLL characteristics	82
6.3.9	Memory characteristics	82
6.3.10	EMC characteristics	83
6.3.11	Electrical sensitivity characteristics	86
6.3.12	I/O current injection characteristics	87
6.3.13	I/O port characteristics	88
6.3.14	NRST pin characteristics	92
6.3.15	12-bit ADC characteristics	93

6.3.16	Temperature sensor characteristics	98
6.3.17	Comparators	99
6.3.18	Timer characteristics	100
6.3.19	Communications interfaces	100
7	Package information	108
7.1	LQFP100 package information	108
7.2	UFBGA100 package information	111
7.3	LQFP64 package information	113
7.4	TFBGA64 package information	116
7.5	WLCSP49 package information	119
7.6	LQFP48 package information	122
7.7	LQFP32 package information	125
7.8	UFQFPN32 package information	128
7.9	Thermal characteristics	131
7.9.1	Reference document	132
8	Part numbering	133
9	Revision history	134

List of tables

Table 1.	Device summary	1
Table 2.	Ultra-low-power STM32L071xx device features and peripheral counts	11
Table 3.	Functionalities depending on the operating power supply range	15
Table 4.	CPU frequency range depending on dynamic voltage scaling	16
Table 5.	Functionalities depending on the working mode (from Run/active down to standby)	16
Table 6.	STM32L0xx peripherals interconnect matrix	18
Table 7.	Temperature sensor calibration values	27
Table 8.	Internal voltage reference measured values	27
Table 9.	Timer feature comparison	28
Table 10.	Comparison of I2C analog and digital filters	30
Table 11.	STM32L071xx I ² C implementation	30
Table 12.	USART implementation	31
Table 13.	SPI/I2S implementation	32
Table 14.	Legend/abbreviations used in the pinout table	38
Table 15.	STM32L071xxx pin definition	39
Table 16.	Alternate functions port A	46
Table 17.	Alternate functions port B	47
Table 18.	Alternate functions port C	48
Table 19.	Alternate functions port D	49
Table 20.	Alternate functions port E	50
Table 21.	Alternate functions port H	51
Table 22.	Voltage characteristics	55
Table 23.	Current characteristics	56
Table 24.	Thermal characteristics	56
Table 25.	General operating conditions	57
Table 26.	Embedded reset and power control block characteristics	59
Table 27.	Embedded internal reference voltage calibration values	60
Table 28.	Embedded internal reference voltage	60
Table 29.	Current consumption in Run mode, code with data processing running from Flash memory	62
Table 30.	Current consumption in Run mode vs code type, code with data processing running from Flash memory	62
Table 31.	Current consumption in Run mode, code with data processing running from RAM	64
Table 32.	Current consumption in Run mode vs code type, code with data processing running from RAM	64
Table 33.	Current consumption in Sleep mode	65
Table 34.	Current consumption in Low-power run mode	66
Table 35.	Current consumption in Low-power sleep mode	67
Table 36.	Typical and maximum current consumptions in Stop mode	68
Table 37.	Typical and maximum current consumptions in Standby mode	69
Table 38.	Average current consumption during Wakeup	70
Table 39.	Peripheral current consumption in Run or Sleep mode	71
Table 40.	Peripheral current consumption in Stop and Standby mode	73
Table 41.	Low-power mode wakeup timings	73
Table 42.	High-speed external user clock characteristics	75
Table 43.	Low-speed external user clock characteristics	76
Table 44.	HSE oscillator characteristics	77

Table 45.	LSE oscillator characteristics	78
Table 46.	16 MHz HSI16 oscillator characteristics	79
Table 47.	LSI oscillator characteristics	80
Table 48.	MSI oscillator characteristics	80
Table 49.	PLL characteristics	82
Table 50.	RAM and hardware registers	82
Table 51.	Flash memory and data EEPROM characteristics	82
Table 52.	Flash memory and data EEPROM endurance and retention	83
Table 53.	EMS characteristics	84
Table 54.	EMI characteristics	85
Table 55.	ESD absolute maximum ratings	86
Table 56.	Electrical sensitivities	86
Table 57.	I/O current injection susceptibility	87
Table 58.	I/O static characteristics	88
Table 59.	Output voltage characteristics	90
Table 60.	I/O AC characteristics	91
Table 61.	NRST pin characteristics	92
Table 62.	ADC characteristics	93
Table 63.	R _{AIN} max for f _{ADC} = 16 MHz	95
Table 64.	ADC accuracy	95
Table 65.	Temperature sensor calibration values	98
Table 66.	Temperature sensor characteristics	98
Table 67.	Comparator 1 characteristics	99
Table 68.	Comparator 2 characteristics	99
Table 69.	TIMx characteristics	100
Table 70.	I2C analog filter characteristics	101
Table 71.	USART/LPUART characteristics	101
Table 72.	SPI characteristics in voltage Range 1	102
Table 73.	SPI characteristics in voltage Range 2	103
Table 74.	SPI characteristics in voltage Range 3	104
Table 75.	I2S characteristics	106
Table 76.	LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data	109
Table 77.	UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data	111
Table 78.	UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)	112
Table 79.	LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data	113
Table 80.	TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data	116
Table 81.	TFBGA64 recommended PCB design rules (0.5 mm pitch BGA)	117
Table 82.	WLCSP49 - 49-pin, 3.294 x 3.258 mm, 0.4 mm pitch wafer level chip scale package mechanical data	120
Table 83.	WLCSP49 recommended PCB design rules (0.4 mm pitch)	121
Table 84.	LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data	123
Table 85.	LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data	126
Table 86.	UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data	129
Table 87.	Thermal characteristics	131
Table 88.	STM32L071xx ordering information scheme	133
Table 89.	Document revision history	134

List of figures

Figure 1.	STM32L071xx block diagram	12
Figure 2.	Clock tree	23
Figure 3.	STM32L071xx LQFP100 pinout - 14 x 14 mm	33
Figure 4.	STM32L071xx UFBGA100 ballout - 7x 7 mm	34
Figure 5.	STM32L071xx LQFP64 pinout - 10 x 10 mm	34
Figure 6.	STM32L071xx TFBGA64 ballout - 5x 5 mm	35
Figure 7.	STM32L071xx WLCSP49 ballout	36
Figure 8.	STM32L071xx LQFP48 pinout - 7 x 7 mm	37
Figure 9.	STM32L071xx LQFP32 pinout	37
Figure 10.	STM32L071xx UFQFPN32 pinout	38
Figure 11.	Memory map	52
Figure 12.	Pin loading conditions	53
Figure 13.	Pin input voltage	53
Figure 14.	Power supply scheme	54
Figure 15.	Current consumption measurement scheme	54
Figure 16.	IDD vs VDD, at TA= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSE, 1WS	63
Figure 17.	IDD vs VDD, at TA= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSI16, 1WS	63
Figure 18.	IDD vs VDD, at TA= 25 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS	67
Figure 19.	IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive	68
Figure 20.	IDD vs VDD, at TA= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks off	69
Figure 21.	High-speed external clock source AC timing diagram	75
Figure 22.	Low-speed external clock source AC timing diagram	76
Figure 23.	HSE oscillator circuit diagram	77
Figure 24.	Typical application with a 32.768 kHz crystal	78
Figure 25.	HSI16 minimum and maximum value versus temperature	79
Figure 26.	VIH/VIL versus VDD (CMOS I/Os)	89
Figure 27.	VIH/VIL versus VDD (TTL I/Os)	89
Figure 28.	I/O AC characteristics definition	92
Figure 29.	Recommended NRST pin protection	93
Figure 30.	ADC accuracy characteristics	96
Figure 31.	Typical connection diagram using the ADC	97
Figure 32.	Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})	97
Figure 33.	Power supply and reference decoupling (V_{REF+} connected to V_{DDA})	98
Figure 34.	SPI timing diagram - slave mode and CPHA = 0	104
Figure 35.	SPI timing diagram - slave mode and CPHA = 1 ⁽¹⁾	105
Figure 36.	SPI timing diagram - master mode ⁽¹⁾	105
Figure 37.	I ² S slave timing diagram (Philips protocol) ⁽¹⁾	107
Figure 38.	I ² S master timing diagram (Philips protocol) ⁽¹⁾	107
Figure 39.	LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline	108
Figure 40.	LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint	110
Figure 41.	LQFP100 marking example (package top view)	110
Figure 42.	UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball	

	grid array package outline	111
Figure 43.	UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint	112
Figure 44.	LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline	113
Figure 45.	LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint	114
Figure 46.	LQFP64 marking example (package top view)	115
Figure 47.	TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch thin profile fine pitch ball grid array package outline	116
Figure 48.	TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball ,grid array recommended footprint	117
Figure 49.	TFBGA64 marking example (package top view)	118
Figure 50.	WLCSP49 - 49-pin, 3.294 x 3.258 mm, 0.4 mm pitch wafer level chip scale package outline.	119
Figure 51.	WLCSP49 - 49-pin, 3.294 x 3.258 mm, 0.4 mm pitch wafer level chip scale recommended footprint.	120
Figure 52.	WLCSP49 marking example (package top view)	121
Figure 53.	LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline	122
Figure 54.	LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint	124
Figure 55.	LQFP48 marking example (package top view)	124
Figure 56.	LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline	125
Figure 57.	LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat recommended footprint	126
Figure 58.	LQFP32 marking example (package top view)	127
Figure 59.	UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline.	128
Figure 60.	UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat recommended footprint.	129
Figure 61.	UFQFPN32 marking example (package top view)	130
Figure 62.	Thermal resistance	132

1 Introduction

The ultra-low-power STM32L071xx are offered in 9 different package types from 32 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L071xx microcontrollers suitable for a wide range of applications:

- Gas/water meters and industrial sensors
- Healthcare and fitness equipment
- Remote control and user interface
- PC peripherals, gaming, GPS equipment
- Alarm system, wired and wireless sensors, video intercom

This STM32L071xx datasheet should be read in conjunction with the STM32L0x1xx reference manual (RM0377).

For information on the ARM® Cortex®-M0+ core please refer to the Cortex®-M0+ Technical Reference Manual, available from the www.arm.com website.

Figure 1 shows the general block diagram of the device family.

2 Description

The access line ultra-low-power STM32L071xx microcontrollers incorporate the high-performance ARM® Cortex®-M0+ 32-bit RISC core operating at a 32 MHz frequency, a memory protection unit (MPU), high-speed embedded memories (up to 192 Kbytes of Flash program memory, 6 Kbytes of data EEPROM and 20 Kbytes of RAM) plus an extensive range of enhanced I/Os and peripherals.

The STM32L071xx devices provide high power efficiency for a wide range of performance. It is achieved with a large choice of internal and external clock sources, an internal voltage adaptation and several low-power modes.

The STM32L071xx devices offer several analog features, one 12-bit ADC with hardware oversampling, two ultra-low-power comparators, several timers, one low-power timer (LPTIM), four general-purpose 16-bit timers and two basic timer, one RTC and one SysTick which can be used as timebases. They also feature two watchdogs, one watchdog with independent clock and window capability and one window watchdog based on bus clock.

Moreover, the STM32L071xx devices embed standard and advanced communication interfaces: up to three I2Cs, two SPIs, one I2S, four USARTs, a low-power UART (LPUART), .

The STM32L071xx also include a real-time clock and a set of backup registers that remain powered in Standby mode.

The ultra-low-power STM32L071xx devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +125 °C temperature range. A comprehensive set of power-saving modes allows the design of low-power applications.



2.1 Device overview

Table 2. Ultra-low-power STM32L071xx device features and peripheral counts

Peripheral	STM32L071K8	STM32L071C8	STM32L071V8	STM32L071KB	STM32L071CB	STM32L071VB	STM32L071RB	STM32L071KZ	STM32L071CZ	STM32L071VZ	STM32L071RZ
Flash (Kbytes)	64 Kbytes			128 Kbytes				192 Kbytes			
Data EEPROM (Kbytes)	3 Kbytes			6 Kbytes							
RAM (Kbytes)	20 Kbytes										
Timers	General-purpose	4									
	Basic	2									
	LPTIMER	1									
RTC/SYSTICK/IWDG /WWDG	1/1/1/1										
Com. interfaces	SPI/I2S	4(3) ⁽¹⁾ /0	6(4) ⁽²⁾ /1	4(3) ⁽¹⁾ /0	6(4) ⁽²⁾ /1			4(3) ⁽¹⁾ /0	6(4) ⁽²⁾ /1		
	I ² C	2	3	2	3			2	3		
	USART	3	4	3	4			3	4		
	LPUART	1									
GPIOs	23	37	84	25 ⁽³⁾	40 ⁽⁴⁾	84	51 ⁽⁵⁾	25 ⁽³⁾	40 ⁽⁴⁾	84	51 ⁽⁵⁾
Clocks: HSE/LSE/HS/MSI/LSI	1/1/1/1/1										
12-bit synchronized ADC Number of channels	10	13	16	10	13 ⁽⁴⁾	16	16 ⁽⁵⁾	10	13 ⁽⁴⁾	16	16 ⁽⁵⁾
Comparators	2										
Max. CPU frequency	32 MHz										
Operating voltage	1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 to 3.6 V without BOR option										
Operating temperatures	Ambient temperature: -40 to +125 °C Junction temperature: -40 to +130 °C										
Packages	UFQFPN32	LQFP48	LQFP/UFBGA100	UFQFPN/LQFP32	LQFP48,WLCSP49	LQFP/UFBGA100	LQFP/TFBGA64	UFQFPN/LQFP32	LQFP48,WLCSP49	LQFP/UFBGA100	LQFP/TFBGA64

- 3 SPI interfaces are USARTs operating in SPI master mode.
- 4 SPI interfaces are USARTs operating in SPI master mode.
- UFQFPN32 has 2 GPIOs less than LQFP32.
- LQFP48 has three GPIOs less than WLCSP49.
- TFBGA64 has one GPIO, one ADC input less than LQFP64.

2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of core and features, from 8-bit proprietary core up to ARM® Cortex®-M4, including ARM® Cortex®-M3 and ARM® Cortex®-M0+. The STM32Lx series are the best choice to answer your needs in terms of ultra-low-power features. The STM32 ultra-low-power series are the best solution for applications such as gaz/water meter, keyboard/mouse or fitness and healthcare application. Several built-in features like LCD drivers, dual-bank memory, low-power run mode, operational amplifiers, 128-bit AES, DAC, crystal-less USB and many other definitely help you building a highly cost optimized application by reducing BOM cost. STMicroelectronics, as a reliable and long-term manufacturer, ensures as much as possible pin-to-pin compatibility between all STM8Lx and STM32Lx on one hand, and between all STM32Lx and STM32Fx on the other hand. Thanks to this unprecedented scalability, your legacy application can be upgraded to respond to the latest market feature and efficiency requirements.

3 Functional overview

3.1 Low-power modes

The ultra-low-power STM32L071xx support dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 (V_{DD} range limited to 1.71-3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full V_{DD} range), with a maximum CPU frequency of 16 MHz
- Range 3 (full V_{DD} range), with a maximum CPU frequency limited to 4.2 MHz

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

- **Low-power run mode**

This mode is achieved with the multispeed internal (MSI) RC oscillator set to the low-speed clock (max 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In Low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

- **Low-power sleep mode**

This mode is achieved by entering Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

When wakeup is triggered by an event or an interrupt, the system reverts to the Run mode with the regulator on.

- **Stop mode with RTC**

The Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSE crystal and HSI RC oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

The device can be woken up from Stop mode by any of the EXTI line, in 3.5 μ s, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on), it can be the RTC alarm/tamper/timestamp/wakeup events, the USART/I2C/LPUART/LPTIMER wakeup events.

- **Stop mode without RTC**

The Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are disabled.

Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 3.5 μ s, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on). It can also be wakened by the USART/I2C/LPUART/LPTIMER wakeup events.

- **Standby mode with RTC**

The Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSE crystal and HSI RC oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

The device exits Standby mode in 60 μ s when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby mode without RTC**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

The device exits Standby mode in 60 μ s when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

Operating power supply range	Functionalities depending on the operating power supply range		
	ADC operation	Dynamic voltage scaling range	I/O operation
$V_{DD} = 1.65$ to 1.71 V	ADC only, conversion time up to 570 ksps	Range 2 or range 3	Degraded speed performance
$V_{DD} = 1.71$ to 1.8 V ⁽¹⁾	ADC only, conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Degraded speed performance
$V_{DD} = 1.8$ to 2.0 V ⁽¹⁾	Conversion time up to 1.14 Msps	Range1, range 2 or range 3	Degraded speed performance

Table 3. Functionalities depending on the operating power supply range (continued)

Operating power supply range	Functionalities depending on the operating power supply range		
	ADC operation	Dynamic voltage scaling range	I/O operation
V _{DD} = 2.0 to 2.4 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation
V _{DD} = 2.4 to 3.6 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation

1. CPU frequency changes from initial to final must respect "fcpu initial <4*fcpu final". It must also respect 5 μs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5 μs, then switch from 16 MHz to 32 MHz.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
32 kHz to 4.2 MHz (0ws)	Range 3

Table 5. Functionalities depending on the working mode (from Run/active down to standby) ⁽¹⁾⁽²⁾

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
					Wakeup capability	Wakeup capability		
CPU	Y	--	Y	--	--	--	--	--
Flash memory	O	O	O	O	--	--	--	--
RAM	Y	Y	Y	Y	Y	--	--	--
Backup registers	Y	Y	Y	Y	Y	Y	Y	Y
EEPROM	O	O	O	O	--	--	--	--
Brown-out reset (BOR)	O	O	O	O	O	O	O	O
DMA	O	O	O	O	--	--	--	--
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	-	--
Power-on/down reset (POR/PDR)	Y	Y	Y	Y	Y	Y	Y	Y
High Speed Internal (HSI)	O	O	--	--	(3)	--	--	--

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)⁽¹⁾⁽²⁾

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
					Wakeup capability	Wakeup capability		
High Speed External (HSE)	O	O	O	O	--		--	
Low Speed Internal (LSI)	O	O	O	O	O		O	
Low Speed External (LSE)	O	O	O	O	O		O	
Multi-Speed Internal (MSI)	O	O	Y	Y	--		--	
Inter-Connect Controller	Y	Y	Y	Y	Y		--	
RTC	O	O	O	O	O	O	O	
RTC Tamper	O	O	O	O	O	O	O	O
Auto WakeUp (AWU)	O	O	O	O	O	O	O	O
USART	O	O	O	O	O ⁽⁴⁾	O	--	
LPUART	O	O	O	O	O ⁽⁴⁾	O	--	
SPI	O	O	O	O	--		--	
I2C	O	O	O	O	O ⁽⁵⁾	O	--	
ADC	O	O	--	--	--		--	
Temperature sensor	O	O	O	O	O		--	
Comparators	O	O	O	O	O	O	--	
16-bit timers	O	O	O	O	--		--	
LPTIMER	O	O	O	O	O	O		
IWDG	O	O	O	O	O	O	O	O
WWDG	O	O	O	O	--		--	
SysTick Timer	O	O	O	O			--	
GPIOs	O	O	O	O	O	O		2 pins
Wakeup time to Run mode	0 μs	0.36 μs	3 μs	32 μs	3.5 μs		50 μs	

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)⁽¹⁾⁽²⁾

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop	Standby
					Wakeup capability	Wakeup capability
Consumption V _{DD} =1.8 to 3.6 V (Typ)	Down to 140 µA/MHz (from Flash memory)	Down to 37 µA/MHz (from Flash memory)	Down to 8 µA	Down to 4.5 µA	0.4 µA (No RTC) V _{DD} =1.8 V	0.28 µA (No RTC) V _{DD} =1.8 V
					0.8 µA (with RTC) V _{DD} =1.8 V	0.65 µA (with RTC) V _{DD} =1.8 V
					0.4 µA (No RTC) V _{DD} =3.0 V	0.29 µA (No RTC) V _{DD} =3.0 V
					1 µA (with RTC) V _{DD} =3.0 V	0.85 µA (with RTC) V _{DD} =3.0 V

- Legend:
 "Y" = Yes (enable).
 "O" = Optional can be enabled/disabled by software
 "-" = Not available
- The consumption values given in this table are preliminary data given for indication. They are subject to slight changes.
- Some peripherals with wakeup from Stop capability can request HSI to be enabled. In this case, HSI is woken up by the peripheral, and only feeds the peripheral which requested it. HSI is automatically put off when the peripheral does not need it anymore.
- UART and LPUART reception is functional in Stop mode. It generates a wakeup interrupt on Start. To generate a wakeup on address match or received frame event, the LPUART can run on LSE clock while the UART has to wake up or keep running the HSI clock.
- I2C address detection is functional in Stop mode. It generates a wakeup interrupt in case of address match. It will wake up the HSI during reception.

3.2 Interconnect matrix

Several peripherals are directly interconnected. This allows autonomous communication between peripherals, thus saving CPU resources and power consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, Low-power run, Low-power sleep and Stop modes.

Table 6. STM32L0xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
COMPx	TIM2, TIM21, TIM22	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	-
	LPTIM	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	Y
TIMx	TIMx	Timer triggered by other timer	Y	Y	Y	Y	-

Table 6. STM32L0xx peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
RTC	TIM21	Timer triggered by Auto wake-up	Y	Y	Y	Y	-
	LPTIM	Timer triggered by RTC event	Y	Y	Y	Y	Y
All clock source	TIMx	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-
GPIO	TIMx	Timer input channel and trigger	Y	Y	Y	Y	-
	LPTIM	Timer input channel and trigger	Y	Y	Y	Y	Y
	ADC	Conversion trigger	Y	Y	Y	Y	-

3.3 ARM[®] Cortex[®]-M0+ core with MPU

The Cortex-M0+ processor is an entry-level 32-bit ARM Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- a simple architecture that is easy to learn and program
- ultra-low power, energy-efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family
- platform security robustness, with integrated Memory Protection Unit (MPU).

The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to its embedded ARM core, the STM32L071xx are compatible with all ARM tools and software.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L071xx embed a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels and 4 priority levels.

The Cortex-M0+ processor closely integrates a configurable Nested Vectored Interrupt Controller (NVIC), to deliver industry-leading interrupt performance. The NVIC:

- includes a Non-Maskable Interrupt (NMI)
- provides zero jitter interrupt option
- provides four interrupt priority levels

The tight integration of the processor core and NVIC provides fast execution of Interrupt Service Routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to abandon and restart load-multiple and store-multiple operations. Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that include a deep sleep function that enables the entire device to enter rapidly stop or standby mode.

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.4 Reset and supply management

3.4.1 Power supply schemes

- $V_{DD} = 1.65$ to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- $V_{SSA}, V_{DDA} = 1.65$ to 3.6 V: external analog power supplies for ADC reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.

3.4.2 Power supply supervisor

The devices have an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

Two versions are available:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the V_{DD} min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the

internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The devices feature an embedded programmable voltage detector (PVD) that monitors the $V_{DD/VDDA}$ power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when $V_{DD/VDDA}$ drops below the V_{PVD} threshold and/or when $V_{DD/VDDA}$ is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.4.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wake-up logic, IWDG, RTC, LSI, LSE crystal 32 KHz oscillator, RCC_CSR).

3.5 Clock management

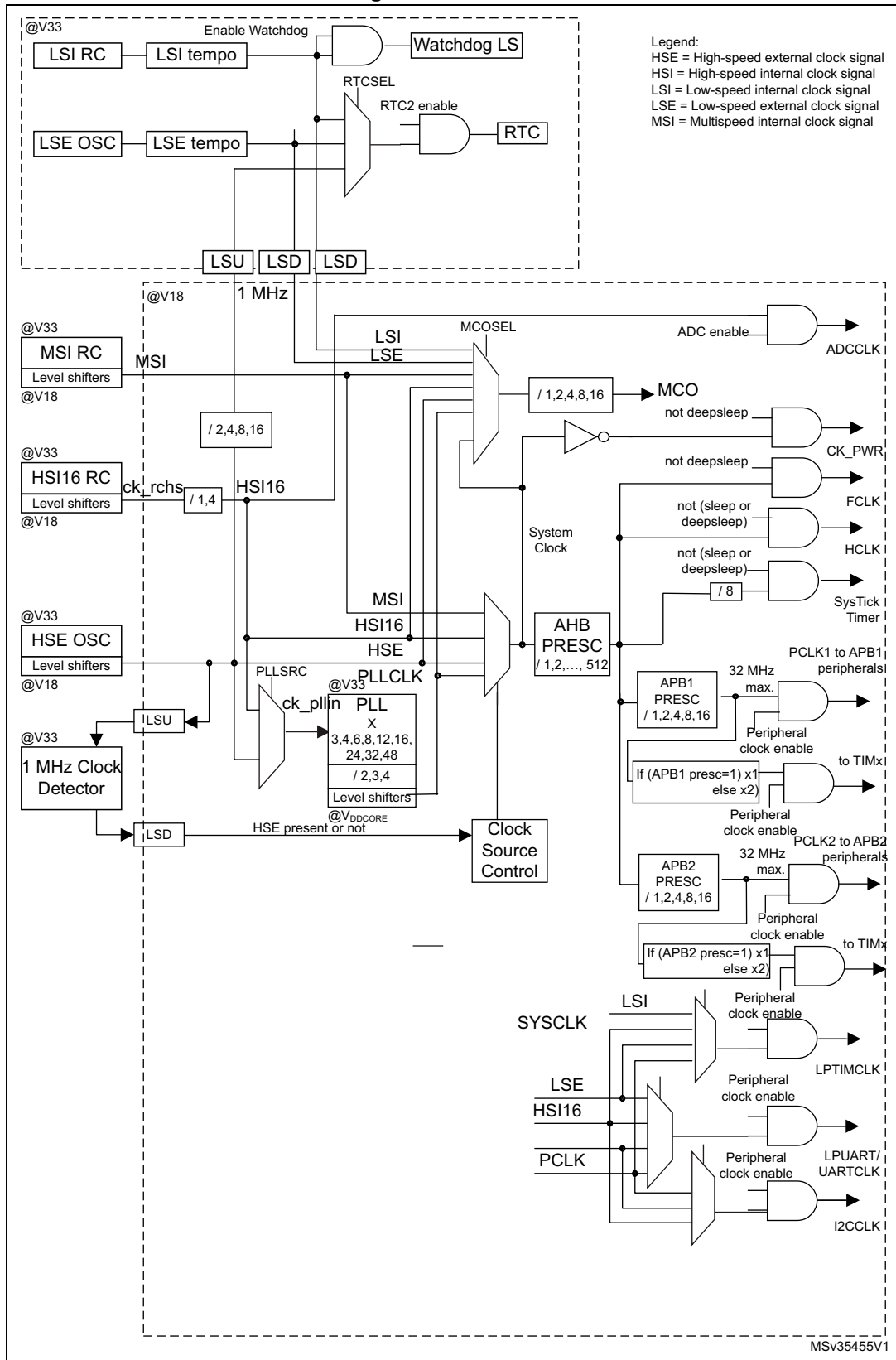
The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**
To get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching**
Clock sources can be changed safely on the fly in Run mode through a configuration register.
- **Clock management**
To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source**
Three different clock sources can be used to drive the master clock SYSCLK:
 - 1-25 MHz high-speed external crystal (HSE), that can supply a PLL
 - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLLMultispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz). When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a $\pm 0.5\%$ accuracy.
- **Auxiliary clock source**
Two ultra-low-power clock sources that can be used to drive the real-time clock:

- 32.768 kHz low-speed external crystal (LSE)
- 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- **RTC clock source**
The LSI, LSE or HSE sources can be chosen to clock the RTC, whatever the system clock.
- **Startup clock**
After reset, the microcontroller restarts by default with an internal 2.1 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS)**
This feature can be enabled by software. If an HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled. Another clock security system can be enabled, in case of failure of the LSE it provides an interrupt or wakeup event which is generated if enabled.
- **Clock-out capability (MCO: microcontroller clock output)**
It outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See [Figure 2](#) for details on the clock tree.

Figure 2. Clock tree



3.6 Low-power real-time clock and backup registers

The real time clock (RTC) and the 5 backup registers are supplied in all modes including standby mode. The backup registers are five 32-bit registers used to store 20 bytes of user application data. They are not reset by a system reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month
- Two programmable alarms with wake up from Stop and Standby mode capability
- Periodic wakeup from Stop and Standby with programmable resolution and period
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 37 kHz)
- The high-speed external clock

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated alternate function registers. All GPIOs are high current capable. Each GPIO output, speed can be slowed (40 MHz, 10 MHz, 2 MHz, 400 kHz). The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to a dedicated IO bus with a toggling speed of up to 32 MHz.

Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 29 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 84 GPIOs can be connected to the 16 configurable interrupt/event lines. The 13 other lines are connected to PVD, RTC, USARTs, I2C, LPUART, LPTIMER or comparator events.

3.8 Memories

The STM32L071xx devices have the following features:

- 20 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
 - 64, 128 or 192 Kbytes of embedded Flash program memory
 - 6 Kbytes of data EEPROM
 - Information block containing 32 user and factory options bytes plus 8 Kbytes of system memory

Flash program and data EEPROM are divided into two banks. This allows writing in one bank while running code or reading data from the other bank.

The user options bytes are used to write-protect or read-out protect the memory (with 4 Kbyte granularity) and/or readout-protect the whole memory with the following options:

- **Level 0:** no protection
- **Level 1:** memory readout protected.
The Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- **Level 2:** chip readout protected, debug features (Cortex-M0+ serial wire) and boot in RAM selection disabled (debugline fuse)

The firewall protects parts of code/data from access by the rest of the code that is executed outside of the protected area. The granularity of the protected code segment or the non-volatile data segment is 256 bytes (Flash memory or EEPROM) against 64 bytes for the volatile data segment (RAM).

The whole non-volatile memory embeds the error correction code (ECC) feature.

3.9 Boot modes

At startup, BOOT0 pin and nBOOT1 option bit are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using SPI1 (PA4, PA5, PA6, PA7) or SPI2 (PB12, PB13, PB14, PB15), I2C1 (PB6, PB7) or I2C2 (PB10, PB11), USART1 (PA9, PA10) or USART2 (PA2, PA3). See STM32™ microcontroller system memory boot mode AN2606 for details.