



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

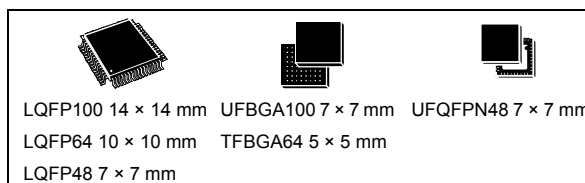


Ultra-low-power 32-bit MCU ARM[®]-based Cortex[®]-M3, 128KB Flash, 16KB SRAM, 4KB EEPROM, LCD, USB, ADC, DAC

Datasheet - production data

Features

- Ultra-low-power platform
 - 1.65 V to 3.6 V power supply
 - -40°C to 85°C/105°C temperature range
 - 0.3 µA Standby mode (3 wakeup pins)
 - 0.9 µA Standby mode + RTC
 - 0.57 µA Stop mode (16 wakeup lines)
 - 1.2 µA Stop mode + RTC
 - 9 µA Low-power run mode
 - 214 µA/MHz Run mode
 - 10 nA ultra-low I/O leakage
 - < 8 µs wakeup time
- Core: ARM[®] Cortex[®]-M3 32-bit CPU
 - From 32 kHz up to 32 MHz max
 - 1.25 DMIPS/MHz (Dhrystone 2.1)
 - Memory protection unit
- Reset and supply management
 - Ultra-safe, low-power BOR (brownout reset) with 5 selectable thresholds
 - Ultra-low-power POR/PDR
 - Programmable voltage detector (PVD)
- Clock sources
 - 1 to 24 MHz crystal oscillator
 - 32 kHz oscillator for RTC with calibration
 - High Speed Internal 16 MHz factory-trimmed RC (+/- 1%)
 - Internal low-power 37 kHz RC
 - Internal multispeed low-power 65 kHz to 4.2 MHz
 - PLL for CPU clock and USB (48 MHz)
- Pre-programmed bootloader
 - USART supported
- Development support
 - Serial wire debug supported
 - JTAG and trace supported
- Up to 83 fast I/Os (73 I/Os 5V tolerant), all mappable on 16 external interrupt vectors
- Memories
 - Up to 128 Kbytes Flash memory with ECC
 - Up to 16 Kbytes RAM



- Up to 4 Kbytes of true EEPROM with ECC
- 80-byte backup register
- LCD Driver (except STM32L151x6/8/B devices) for up to 8x40 segments
 - Support contrast adjustment
 - Support blinking mode
 - Step-up converter on board
- Rich analog peripherals (down to 1.8 V)
 - 12-bit ADC 1 Msps up to 24 channels
 - 12-bit DAC 2 channels with output buffers
 - 2x ultra-low-power-comparators (window mode and wake up capability)
- DMA controller 7x channels
- 8x peripheral communication interfaces
 - 1x USB 2.0 (internal 48 MHz PLL)
 - 3x USARTs (ISO 7816, IrDA)
 - 2x SPIs 16 Mbit/s
 - 2x I2Cs (SMBus/PMBus)
- 10x timers: 6x 16-bit with up to 4 IC/OC/PWM channels, 2x 16-bit basic timers, 2x watchdog timers (independent and window)
- Up to 20 capacitive sensing channels supporting touchkey, linear and rotary touch sensors
- CRC calculation unit, 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM32L151x6/8/B	STM32L151CB, STM32L151C8, STM32L151C6, STM32L151RB, STM32L151R8, STM32L151R6, STM32L151VB, STM32L151V8
STM32L152x6/8/B	STM32L152CB, STM32L152C8, STM32L152C6, STM32L152RB, STM32L152R8, STM32L152R6, STM32L152VB, STM32L152V8

Contents

1	Introduction	9
2	Description	10
2.1	Device overview	11
2.2	Ultra-low-power device continuum	12
2.2.1	Performance	12
2.2.2	Shared peripherals	12
2.2.3	Common system strategy	12
2.2.4	Features	12
3	Functional overview	13
3.1	Low power modes	14
3.2	ARM [®] Cortex [®] -M3 core with MPU	18
3.3	Reset and supply management	19
3.3.1	Power supply schemes	19
3.3.2	Power supply supervisor	19
3.3.3	Voltage regulator	20
3.3.4	Boot modes	20
3.4	Clock management	21
3.5	Low power real-time clock and backup registers	23
3.6	GPIOs (general-purpose inputs/outputs)	23
3.7	Memories	24
3.8	DMA (direct memory access)	24
3.9	LCD (liquid crystal display)	24
3.10	ADC (analog-to-digital converter)	25
3.10.1	Temperature sensor	25
3.10.2	Internal voltage reference (V _{REFINT})	25
3.11	DAC (digital-to-analog converter)	25
3.12	Ultra-low-power comparators and reference voltage	26
3.13	Routing interface	26
3.14	Touch sensing	26
3.15	Timers and watchdogs	27

3.15.1	General-purpose timers (TIM2, TIM3, TIM4, TIM9, TIM10 and TIM11)	28
3.15.2	Basic timers (TIM6 and TIM7)	28
3.15.3	SysTick timer	28
3.15.4	Independent watchdog (IWDG)	28
3.15.5	Window watchdog (WWDG)	29
3.16	Communication interfaces	29
3.16.1	I ² C bus	29
3.16.2	Universal synchronous/asynchronous receiver transmitter (USART)	29
3.16.3	Serial peripheral interface (SPI)	29
3.16.4	Universal serial bus (USB)	29
3.17	CRC (cyclic redundancy check) calculation unit	30
3.18	Development support	30
4	Pin descriptions	31
5	Memory mapping	48
6	Electrical characteristics	49
6.1	Parameter conditions	49
6.1.1	Minimum and maximum values	49
6.1.2	Typical values	49
6.1.3	Typical curves	49
6.1.4	Loading capacitor	49
6.1.5	Pin input voltage	49
6.1.6	Power supply scheme	50
6.1.7	Optional LCD power supply scheme	51
6.1.8	Current consumption measurement	51
6.2	Absolute maximum ratings	52
6.3	Operating conditions	53
6.3.1	General operating conditions	53
6.3.2	Embedded reset and power control block characteristics	54
6.3.3	Embedded internal reference voltage	56
6.3.4	Supply current characteristics	57
6.3.5	Wake-up time from Low power mode	69
6.3.6	External clock source characteristics	70
6.3.7	Internal clock source characteristics	75
6.3.8	PLL characteristics	77

6.3.9	Memory characteristics	78
6.3.10	EMC characteristics	79
6.3.11	Electrical sensitivity characteristics	80
6.3.12	I/O current injection characteristics	81
6.3.13	I/O port characteristics	82
6.3.14	NRST pin characteristics	85
6.3.15	TIM timer characteristics	86
6.3.16	Communication interfaces	87
6.3.17	12-bit ADC characteristics	93
6.3.18	DAC electrical specifications	99
6.3.19	Temperature sensor characteristics	101
6.3.20	Comparator	102
6.3.21	LCD controller (STM32L152xx only)	104
7	Package information	105
7.1	LQFP100 14 x 14 mm, 100-pin low-profile quad flat package information	105
7.2	LQFP64 10 x 10 mm, 64-pin low-profile quad flat package information	108
7.3	LQFP48 7 x 7 mm, 48-pin low-profile quad flat package information	111
7.4	UFQFPN48 7 x 7 mm, 0.5 mm pitch, package information	114
7.5	UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package information	117
7.6	TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package information	120
7.7	Thermal characteristics	123
7.7.1	Reference document	124
8	Ordering information	125
9	Revision history	126

List of tables

Table 1.	Device summary	1
Table 2.	Ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B device features and peripheral counts	11
Table 3.	Functionalities depending on the operating power supply range	15
Table 4.	CPU frequency range depending on dynamic voltage scaling	16
Table 5.	Working mode-dependent functionalities (from Run/active down to standby)	17
Table 6.	Timer feature comparison	27
Table 7.	Legend/abbreviations used in the pinout table	36
Table 8.	STM32L151x6/8/B and STM32L152x6/8/B pin definitions	37
Table 9.	Alternate function input/output	43
Table 10.	Voltage characteristics	52
Table 11.	Current characteristics	52
Table 12.	Thermal characteristics	53
Table 13.	General operating conditions	53
Table 14.	Embedded reset and power control block characteristics	54
Table 15.	Embedded internal reference voltage calibration values	56
Table 16.	Embedded internal reference voltage	56
Table 17.	Current consumption in Run mode, code with data processing running from Flash	58
Table 18.	Current consumption in Run mode, code with data processing running from RAM	59
Table 19.	Current consumption in Sleep mode	60
Table 20.	Current consumption in Low power run mode	62
Table 21.	Current consumption in Low power sleep mode	63
Table 22.	Typical and maximum current consumptions in Stop mode	64
Table 23.	Typical and maximum current consumptions in Standby mode	66
Table 24.	Peripheral current consumption	67
Table 25.	Low-power mode wakeup timings	69
Table 26.	High-speed external user clock characteristics	70
Table 27.	Low-speed external user clock characteristics	71
Table 28.	HSE oscillator characteristics	72
Table 29.	LSE oscillator characteristics ($f_{LSE} = 32.768$ kHz)	73
Table 30.	HSI oscillator characteristics	75
Table 31.	LSI oscillator characteristics	75
Table 32.	MSI oscillator characteristics	76
Table 33.	PLL characteristics	77
Table 34.	RAM and hardware registers	78
Table 35.	Flash memory and data EEPROM characteristics	78
Table 36.	Flash memory, data EEPROM endurance and data retention	78
Table 37.	EMS characteristics	79
Table 38.	EMI characteristics	80
Table 39.	ESD absolute maximum ratings	80
Table 40.	Electrical sensitivities	81
Table 41.	I/O current injection susceptibility	81
Table 42.	I/O static characteristics	82
Table 43.	Output voltage characteristics	83
Table 44.	I/O AC characteristics	84
Table 45.	NRST pin characteristics	85
Table 46.	TIMx characteristics	86
Table 47.	I ² C characteristics	87

Table 48.	SCL frequency ($f_{PCLK1} = 32$ MHz, $V_{DD} = V_{DD_I2C} = 3.3$ V)	88
Table 49.	SPI characteristics	89
Table 50.	USB startup time	91
Table 51.	USB DC electrical characteristics	92
Table 52.	USB: full speed electrical characteristics	92
Table 53.	ADC clock frequency	93
Table 54.	ADC characteristics	93
Table 55.	ADC accuracy	95
Table 56.	Maximum source impedance R_{AIN} max	97
Table 57.	DAC characteristics	99
Table 58.	Temperature sensor calibration values	101
Table 59.	Temperature sensor characteristics	101
Table 60.	Comparator 1 characteristics	102
Table 61.	Comparator 2 characteristics	103
Table 62.	LCD controller characteristics	104
Table 63.	LQPF100 14 x 14 mm, 100-pin low-profile quad flat package mechanical data	106
Table 64.	LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical data	108
Table 65.	LQFP48 7 x 7 mm, 48-pin low-profile quad flat package mechanical data	112
Table 66.	UFQFPN48 7 x 7 mm, 0.5 mm pitch, package mechanical data	115
Table 67.	UFBGA100 7 x 7 mm, 0.5 mm pitch, package mechanical data	117
Table 68.	UFBGA100 7 x 7 mm, 0.5 mm pitch, recommended PCB design rules	118
Table 69.	TFBGA64 5 x 5 mm, 0.5 mm pitch, package mechanical data	120
Table 70.	TFBGA64 5 x 5 mm, 0.5 mm pitch, recommended PCB design rules	121
Table 71.	Thermal characteristics	123
Table 72.	Ordering information scheme	125
Table 73.	Document revision history	126

List of figures

Figure 1.	Ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B block diagram	13
Figure 2.	Clock tree	22
Figure 3.	STM32L15xVx UFBGA100 ballout	31
Figure 4.	STM32L15xVx LQFP100 pinout	32
Figure 5.	STM32L15xRx TFBGA64 ballout	33
Figure 6.	STM32L15xRx LQFP64 pinout	34
Figure 7.	STM32L15xCx LQFP48 pinout	34
Figure 8.	STM32L15xCx UFQFPN48 pinout	35
Figure 9.	Memory map	48
Figure 10.	Pin loading conditions	49
Figure 11.	Pin input voltage	49
Figure 12.	Power supply scheme	50
Figure 13.	Optional LCD power supply scheme	51
Figure 14.	Current consumption measurement scheme	51
Figure 15.	High-speed external clock source AC timing diagram	70
Figure 16.	Low-speed external clock source AC timing diagram	71
Figure 17.	HSE oscillator circuit diagram	73
Figure 18.	Typical application with a 32.768 kHz crystal	74
Figure 19.	I/O AC characteristics definition	85
Figure 20.	Recommended NRST pin protection	86
Figure 21.	I ² C bus AC waveforms and measurement circuit	88
Figure 22.	SPI timing diagram - slave mode and CPHA = 0	90
Figure 23.	SPI timing diagram - slave mode and CPHA = 1 ⁽¹⁾	90
Figure 24.	SPI timing diagram - master mode ⁽¹⁾	91
Figure 25.	USB timings: definition of data signal rise and fall time	92
Figure 26.	ADC accuracy characteristics	96
Figure 27.	Typical connection diagram using the ADC	96
Figure 28.	Maximum dynamic current consumption on V _{REF+} supply pin during ADC conversion	97
Figure 29.	Power supply and reference decoupling (V _{REF+} not connected to V _{DDA})	98
Figure 30.	Power supply and reference decoupling (V _{REF+} connected to V _{DDA})	98
Figure 31.	12-bit buffered /non-buffered DAC	101
Figure 32.	LQFP100 14 x 14 mm, 100-pin low-profile quad flat package outline	105
Figure 33.	LQFP100 14 x 14 mm, 100-pin low-profile quad flat package recommended footprint	107
Figure 34.	LQFP100 14 x 14 mm, 100-pin package top view example	107
Figure 35.	LQFP64 10 x 10 mm, 64-pin low-profile quad flat package outline	108
Figure 36.	LQFP64 10 x 10 mm, 64-pin low-profile quad flat package recommended footprint	109
Figure 37.	LQFP64 10 x 10 mm, 64-pin low-profile quad flat package top view example	110
Figure 38.	LQFP48 7 x 7 mm, 48-pin low-profile quad flat package outline	111
Figure 39.	LQFP48 7 x 7 mm, 48-pin low-profile quad flat recommended footprint	112
Figure 40.	LQFP48 7 x 7 mm, 48-pin low-profile quad flat package top view example	113
Figure 41.	UFQFPN48 7 x 7 mm, 0.5 mm pitch, package outline	114
Figure 42.	UFQFPN48 7 x 7 mm, 0.5 mm pitch, package recommended footprint	115
Figure 43.	UFQFPN48 7 x 7 mm, 0.5 mm pitch, package top view example	116
Figure 44.	UFBGA100, 7 x 7 mm, 0.5 mm pitch, package outline	117
Figure 45.	UFBGA100 7 x 7 mm, 0.5 mm pitch, package recommended footprint	118
Figure 46.	UFBGA100 7 x 7 mm, 0.5 mm pitch, package top view example	119
Figure 47.	TFBGA64 5 x 5 mm, 0.5 mm pitch, package outline	120

Figure 48. TFBGA64, 5 x 5 mm, 0.5 mm pitch, recommended footprint	121
Figure 49. TFBGA64 5 x 5 mm, 0.5 mm pitch, package top view example	122
Figure 50. Thermal resistance	124

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L151x6/8/B and STM32L152x6/8/B ultra-low-power ARM[®] Cortex[®]-M3 based microcontrollers product line.

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B family includes devices in 3 different package types: from 48 to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B microcontroller family suitable for a wide range of applications:

- Medical and handheld equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, Wired and wireless sensors, Video intercom
- Utility metering

This STM32L151x6/8/B and STM32L152x6/8/B datasheet should be read in conjunction with the STM32L1xxxx reference manual (RM0038).

The document "Getting started with STM32L1xxxx hardware development" AN3216 gives a hardware implementation overview. Both documents are available from the STMicroelectronics website www.st.com.

For information on the ARM[®] Cortex[®]-M3 core please refer to the Cortex[®]-M3 Technical Reference Manual, available from the www.arm.com website.

Figure 1 shows the general block diagram of the device family.

Caution: This datasheet does not apply to STM32L15xx6/8/B-A covered by a separate datasheet.

2 Description

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices incorporate the connectivity power of the universal serial bus (USB) with the high-performance ARM[®] Cortex[®]-M3 32-bit RISC core operating at 32 MHz frequency (33.3 DMIPS), a memory protection unit (MPU), high-speed embedded memories (Flash memory up to 128 Kbytes and RAM up to 16 Kbytes) and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

All the devices offer a 12-bit ADC, 2 DACs and 2 ultra-low-power comparators, six general-purpose 16-bit timers and two basic timers, which can be used as time bases.

Moreover, the STM32L151x6/8/B and STM32L152x6/8/B devices contain standard and advanced communication interfaces: up to two I²Cs and SPIs, three USARTs and a USB. The STM32L151x6/8/B and STM32L152x6/8/B devices offer up to 20 capacitive sensing channels to simply add touch sensing functionality to any application.

They also include a real-time clock and a set of backup registers that remain powered in Standby mode.

Finally, the integrated LCD controller (except STM32L151x6/8/B devices) has a built-in LCD voltage generator that allows to drive up to 8 multiplexed LCDs with contrast independent of the supply voltage.

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. It is available in the -40 to +85 °C temperature range, extended to 105°C in low power dissipation state. A comprehensive set of power-saving modes allows the design of low-power applications.



2.1 Device overview

Table 2. Ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B device features and peripheral counts

Peripheral		STM32L15xCx			STM32L15xRx			STM32L15xVx		
Flash (Kbytes)		32	64	128	32	64	128	64	128	
Data EEPROM (Kbytes)		4								
RAM (Kbytes)		10	10	16	10	10	16	10	16	
Timers	General-purpose	6								
	Basic	2								
Communication interfaces	SPI	2								
	I ² C	2								
	USART	3								
	USB	1								
GPIOs		37			51			83		
12-bit synchronized ADC Number of channels		1 14 channels			1 20 channels			1 24 channels		
12-bit DAC Number of channels		2 2								
LCD (STM32L152xx Only) COM x SEG		4x18			4x32 8x28			4x44 8x40		
Comparator		2								
Capacitive sensing channels		13			20					
Max. CPU frequency		32 MHz								
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V without BOR option								
Operating temperatures		Ambient temperatures: -40 to +85 °C Junction temperature: -40 to + 105 °C								
Packages		LQFP48, UFQFPN48			LQFP64, BGA64			LQFP100, BGA100		

2.2 Ultra-low-power device continuum

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices are fully pin-to-pin and software compatible. Besides the full compatibility within the family, the devices are part of STMicroelectronics microcontrollers ultra-low-power strategy which also includes STM8L101xx and STM8L15xx devices. The STM8L and STM32L families allow a continuum of performance, peripherals, system architecture and features.

They are all based on STMicroelectronics ultra-low leakage process.

Note: The ultra-low-power STM32L and general-purpose STM32Fxxxx families are pin-to-pin compatible. The STM8L15xxx devices are pin-to-pin compatible with the STM8L101xx devices. Please refer to the STM32F and STM8L documentation for more information on these devices.

2.2.1 Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM® Cortex®-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-low-power performance to range from 5 up to 33.3 DMIPs.

2.2.2 Shared peripherals

STM8L15xxx and STM32L1xxxx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC, DAC and comparators
- Digital peripherals: RTC and some communication interfaces

2.2.3 Common system strategy

To offer flexibility and optimize performance, the STM8L15xx and STM32L1xxxx families use a common architecture:

- Same power supply range from 1.65 V to 3.6 V, (1.65 V at power down only for STM8L15xx devices)
- Architecture optimized to reach ultra-low consumption both in low power modes and Run mode
- Fast startup strategy from low power modes
- Flexible system clock
- Ultrasafe reset: same reset strategy including power-on reset, power-down reset, brownout reset and programmable voltage detector.

2.2.4 Features

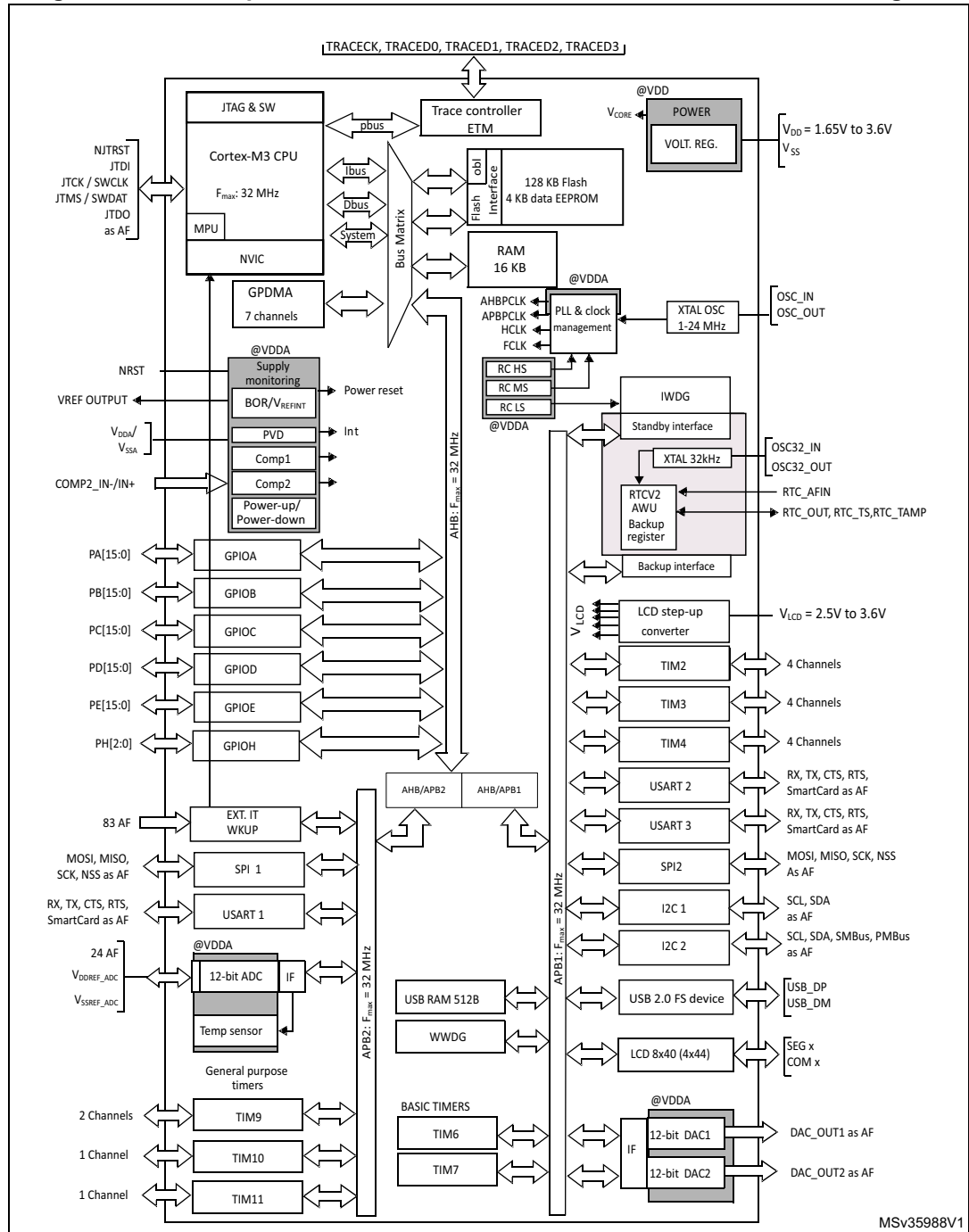
ST ultra-low-power continuum also lies in feature compatibility:

- More than 10 packages with pin count from 20 to 144 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 384 Kbytes

3 Functional overview

Figure 1 shows the block diagram.

Figure 1. Ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B block diagram



1. AF = alternate function on I/O port pin.



3.1 Low power modes

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices support dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply:

- In Range 1 (V_{DD} range limited to 1.71-3.6 V), the CPU runs at up to 32 MHz (refer to [Table 17](#) for consumption).
- In Range 2 (full V_{DD} range), the CPU runs at up to 16 MHz (refer to [Table 17](#) for consumption)
- In Range 3 (full V_{DD} range), the CPU runs at up to 4 MHz (generated only with the multispeed internal RC oscillator clock source). Refer to [Table 17](#) for consumption.

Seven low power modes are provided to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**
In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
Sleep mode power consumption: refer to [Table 19](#).
- **Low power run mode**
This mode is achieved with the multispeed internal (MSI) RC oscillator set to the minimum clock (65 kHz), execution from SRAM or Flash memory, and internal regulator in low power mode to minimize the regulator's operating current. In the Low power run mode, the clock frequency and the number of enabled peripherals are both limited.
Low power run mode consumption: refer to [Table 20: Current consumption in Low power run mode](#).
- **Low power sleep mode**
This mode is achieved by entering the Sleep mode with the internal voltage regulator in Low power mode to minimize the regulator's operating current. In the Low power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.
When wakeup is triggered by an event or an interrupt, the system reverts to the run mode with the regulator on.
Low power sleep mode consumption: refer to [Table 21: Current consumption in Low power sleep mode](#).
- **Stop mode with RTC**
Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSI RC and HSE crystal oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low power mode.
The device can be woken up from Stop mode by any of the EXTI line, in 8 μ s. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on), it can be the RTC alarm(s), the USB wakeup, the RTC tamper events, the RTC timestamp event or the RTC wakeup.
- **Stop mode without RTC**
Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, LSE and

HSE crystal oscillators are disabled. The voltage regulator is in the low power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8 μ s. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.

Stop mode consumption: refer to [Table 22: Typical and maximum current consumptions in Stop mode](#).

- **Standby mode with RTC**

Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

The device exits Standby mode in 60 μ s when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby mode without RTC**

Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

The device exits Standby mode in 60 μ s when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Standby mode consumption: refer to [Table 23](#).

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering the Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

Operating power supply range	Functionalities depending on the operating power supply range			
	DAC and ADC operation	USB	Dynamic voltage scaling range	I/O operation
$V_{DD} = 1.65$ to 1.71 V	Not functional	Not functional	Range 2 or Range 3	Degraded speed performance
$V_{DD} = 1.71$ to 1.8 V ⁽¹⁾	Not functional	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance
$V_{DD} = 1.8$ to 2.0 V ⁽¹⁾	Conversion time up to 500 Ksps	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance

Table 3. Functionalities depending on the operating power supply range (continued)

Operating power supply range	Functionalities depending on the operating power supply range			
	DAC and ADC operation	USB	Dynamic voltage scaling range	I/O operation
V _{DD} = 2.0 to 2.4 V	Conversion time up to 500 Ksps	Functional ⁽²⁾	Range 1, Range 2 or Range 3	Full speed operation
V _{DD} = 2.4 to 3.6 V	Conversion time up to 1 Msps	Functional ⁽²⁾	Range 1, Range 2 or Range 3	Full speed operation

1. The CPU frequency changes from initial to final must respect "F_{CPU} initial < 4*F_{CPU} final" to limit V_{CORE} drop due to current consumption peak when frequency increases. It must also respect 5 μs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5 μs, then switch from 16 MHz to 32 MHz.
2. Should be USB compliant from I/O voltage standpoint, the minimum V_{DD} is 3.0 V.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
2.1 MHz to 4.2 MHz (1ws) 32 kHz to 2.1 MHz (0ws)	Range 3

Table 5. Working mode-dependent functionalities (from Run/active down to standby)

Ips	Run/Active	Sleep	Low-power Run	Low-power Sleep	Stop		Standby	
					Wakeup capability	Wakeup capability		
CPU	Y	-	Y	-	-	-	-	-
Flash	Y	Y	Y	Y	-	-	-	-
RAM	Y	Y	Y	Y	Y	-	-	-
Backup Registers	Y	Y	Y	Y	Y	-	Y	-
EEPROM	Y	-	Y	Y	Y	-	-	-
Brown-out rest (BOR)	Y	Y	Y	Y	Y	Y	Y	-
DMA	Y	Y	Y	Y	-	-	-	-
Programmable Voltage Detector (PVD)	Y	Y	Y	Y	Y	Y	Y	-
Power On Reset (POR)	Y	Y	Y	Y	Y	Y	Y	-
Power Down Rest (PDR)	Y	Y	Y	Y	Y	-	Y	-
High Speed Internal (HSI)	Y	Y	-	-	-	-	-	-
High Speed External (HSE)	Y	Y	-	-	-	-	-	-
Low Speed Internal (LSI)	Y	Y	Y	Y	Y	-	Y	-
Low Speed External (LSE)	Y	Y	Y	Y	Y	-	Y	-
Multi-Speed Internal (MSI)	Y	Y	Y	Y	-	-	-	-
Inter-Connect Controller	Y	Y	Y	Y	-	-	-	-
RTC	Y	Y	Y	Y	Y	Y	Y	-
RTC Tamper	Y	Y	Y	Y	Y	Y	Y	Y
Auto Wakeup (AWU)	Y	Y	Y	Y	Y	Y	Y	Y
LCD	Y	Y	Y	Y	Y	-	-	-
USB	Y	Y	-	-	-	Y	-	-
USART	Y	Y	Y	Y	Y	(1)	-	-
SPI	Y	Y	Y	Y	-	-	-	-
I2C	Y	Y	Y	Y	-	(1)	-	-
ADC	Y	Y	-	-	-	-	-	-

Table 5. Working mode-dependent functionalities (from Run/active down to standby) (continued)

Ips	Run/Active	Sleep	Low-power Run	Low-power Sleep	Stop		Standby	
					Wakeup capability	Wakeup capability		
DAC	Y	Y	Y	Y	Y	-	-	-
Temperature sensor	Y	Y	Y	Y	Y	-	-	-
Comparators	Y	Y	Y	Y	Y	Y	-	-
16-bit and 32-bit Timers	Y	Y	Y	Y	-	-	-	-
IWDG	Y	Y	Y	Y	Y	Y	Y	Y
WWDG	Y	Y	Y	Y	-	-	-	-
Touch sensing	Y	-	-	-	-	-	-	-
Systick Timer	Y	Y	Y	Y	-	-	-	-
GPIOs	Y	Y	Y	Y	Y	Y	-	3 Pins
Wakeup time to Run mode	0 μs	0.36 μs	3 μs	32 μs	< 8 μs		50 μs	
Consumption V _{DD} =1.8V to 3.6V (Typ)	Down to 214 μA/MHz (from Flash)	Down to 50 μA/MHz (from Flash)	Down to 9 μA	Down to 4.4 μA	0.5 μA (No RTC) V _{DD} =1.8V		0.3 μA (No RTC) V _{DD} =1.8V	
					1.4 μA (with RTC) V _{DD} =1.8V		1 μA (with RTC) V _{DD} =1.8V	
					0.5 μA (No RTC) V _{DD} =3.0V		0.3 μA (No RTC) V _{DD} =3.0V	
					1.6 μA (with RTC) V _{DD} =3.0V		1.3 μA (with RTC) V _{DD} =3.0V	

1. The startup on communication line wakes the CPU which was made possible by an EXTI, this induces a delay before entering run mode.

3.2 ARM[®] Cortex[®]-M3 core with MPU

The ARM[®] Cortex[®]-M3 processor is the industry leading processor for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM[®] Cortex[®]-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The memory protection unit (MPU) improves system reliability by defining the memory attributes (such as read/write access permissions) for different memory regions. It provides up to eight different regions and an optional predefined background region.

Owing to its embedded ARM core, the STM32L151x6/8/B and STM32L152x6/8/B devices are compatible with all ARM tools and software.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L151x6/8/B and STM32L152x6/8/B devices embed a nested vectored interrupt controller able to handle up to 45 maskable interrupt channels (not including the 16 interrupt lines of Cortex[®]-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving*, higher-priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.3 Reset and supply management

3.3.1 Power supply schemes

- $V_{DD} = 1.65$ to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA} , $V_{DDA} = 1.65$ to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

The device exists in two versions:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the V_{DD} min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wake-up logic, IWDG, RTC, LSI, LSE crystal 32K osc, RCC_CSR).

3.3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from Flash memory
- Boot from System Memory
- Boot from embedded RAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1 or USART2. See STM32™ microcontroller system memory boot mode AN2606 for details.

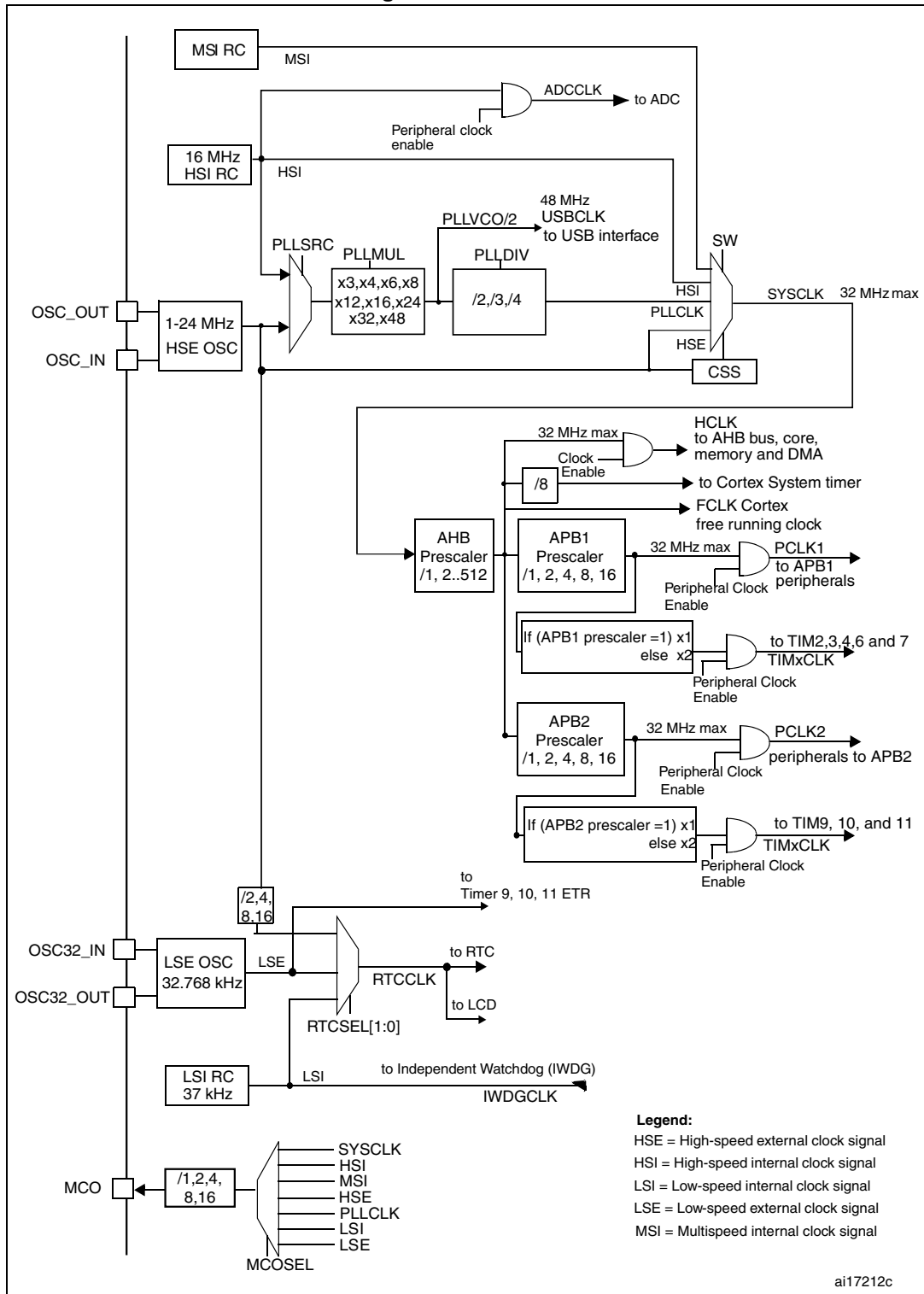
3.4 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Master clock source:** three different clock sources can be used to drive the master clock:
 - 1-24 MHz high-speed external crystal (HSE), that can supply a PLL
 - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
 - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz) with a consumption proportional to speed, down to 750 nA typical. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a $\pm 0.5\%$ accuracy.
- **Auxiliary clock source:** two ultra-low-power clock sources that can be used to drive the LCD controller and the real-time clock:
 - 32.768 kHz low-speed external crystal (LSE)
 - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- **RTC and LCD clock sources:** the LSI, LSE or HSE sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **USB clock source:** the embedded PLL has a dedicated 48 MHz clock output to supply the USB interface.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 2.1 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.
- **Clock-out capability (MCO: microcontroller clock output):** it outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See [Figure 2](#) for details on the clock tree.

Figure 2. Clock tree



3.5 Low power real-time clock and backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are made automatically. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes.

- The programmable wakeup time ranges from 120 μ s to 36 hours
- Stop mode consumption with LSI and Auto-wakeup: 1.2 μ A (at 1.8 V) and 1.4 μ A (at 3.0 V)
- Stop mode consumption with LSE, calendar and Auto-wakeup: 1.3 μ A (at 1.8V), 1.6 μ A (at 3.0 V)

The RTC can be calibrated with an external 512 Hz output, and a digital compensation circuit helps reduce drift due to crystal deviation.

There are twenty 32-bit backup registers provided to store 80 bytes of user application data. They are cleared in case of tamper detection.

3.6 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated AFIO registers. All GPIOs are high current capable. The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to the AHB with a toggling speed of up to 16 MHz.

External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 83 GPIOs can be connected to the 16 external interrupt lines. The 7 other lines are connected to RTC, PVD, USB or Comparator events.

3.7 Memories

The STM32L151x6/8/B and STM32L152x6/8/B devices have the following features:

- Up to 16 Kbytes of embedded RAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
 - 32, 64 or 128 Kbytes of embedded Flash program memory
 - 4 Kbytes of data EEPROM
 - Options bytes

The options bytes are used to write-protect the memory (with 4 Kbytes granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no readout protection
- Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- Level 2: chip readout protection, debug features (Cortex[®]-M3 JTAG and serial wire) and boot in RAM selection disabled (JTAG fuse)

The whole non-volatile memory embeds the error correction code (ECC) feature.

3.8 DMA (direct memory access)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I²C, USART, general-purpose timers and ADC.

3.9 LCD (liquid crystal display)

The LCD drives up to 8 common terminals and 44 segment terminals to drive up to 320 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD} . This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode

3.10 ADC (analog-to-digital converter)

A 12-bit analog-to-digital converters is embedded into STM32L151x6/8/B and STM32L152x6/8/B devices with up to 24 external channels, performing conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start trigger and injection trigger, to allow the application to synchronize A/D conversions and timers. An injection mode allows high priority conversions to be done by interrupting a scan mode which runs in as a background task.

The ADC includes a specific low power mode. The converter is able to operate at maximum speed even if the CPU is operating at a very low frequency and has an auto-shutdown function. The ADC's runtime and analog front-end current consumption are thus minimized whatever the MCU operating mode.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode, see [Table 58: Temperature sensor calibration values](#).

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the V_{DD} value (when no external voltage, $V_{\text{REF+}}$, is available for ADC). The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode see [Table 16: Embedded internal reference voltage](#).

3.11 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.