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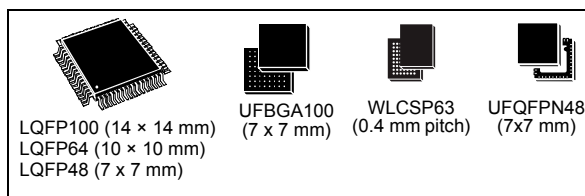


Ultra-low-power 32-bit MCU ARM[®]-based Cortex[®]-M3,
256KB Flash, 32KB SRAM, 8KB EEPROM, LCD, USB, ADC, DAC

Datasheet - production data

Features

- Ultra-low-power platform
 - 1.65 V to 3.6 V power supply
 - **-40 °C to 105 °C** temperature range
 - 0.29µA Standby mode (3 wakeup pins)
 - **1.15 µA Standby mode + RTC**
 - 0.44 µA Stop mode (16 wakeup lines)
 - 1.4 µA Stop mode + RTC
 - 8.6 µA Low-power run mode
 - 185 µA/MHz Run mode
 - 10 nA ultra-low I/O leakage
 - 8 µs wakeup time
- Core: ARM[®] Cortex[®]-M3 32-bit CPU
 - From 32 kHz up to 32 MHz max
 - 1.25 DMIPS/MHz (Dhrystone 2.1)
 - Memory protection unit
- Reset and supply management
 - Low-power, ultrasafe BOR (brownout reset) with 5 selectable thresholds
 - Ultra-low-power POR/PDR
 - Programmable voltage detector (PVD)
- Clock sources
 - 1 to 24 MHz crystal oscillator
 - 32 kHz oscillator for RTC with calibration
 - High Speed Internal 16 MHz factory-trimmed RC (+/- 1%)
 - Internal Low-power 37 kHz RC
 - Internal multispeed low-power 65 kHz to 4.2 MHz PLL for CPU clock and USB (48 MHz)
- Pre-programmed bootloader
 - USB and USART supported
- Development support
 - Serial wire debug supported
 - JTAG and trace supported
- Up to 83 fast I/Os (70 I/Os 5V tolerant), all mappable on 16 external interrupt vectors



- Memories
 - 256 KB Flash memory with ECC
 - 32 KB RAM
 - 8 KB of true EEPROM with ECC
 - 128-byte backup register
- LCD Driver (except STM32L151xC devices) up to 8x40 segments, contrast adjustment, blinking mode, step-up converter
- Rich analog peripherals (down to 1.8 V)
 - 2x operational amplifiers
 - 12-bit ADC 1Msps up to 25 channels
 - 12-bit DAC 2 channels with output buffers
 - 2x ultra-low-power-comparators (window mode and wake up capability)
- DMA controller 12x channels
- 9x peripheral communication interfaces
 - 1x USB 2.0 (internal 48 MHz PLL)
 - 3x USARTs
 - Up to 8x SPIs (2x I2S, 3x 16 Mbit/s)
 - 2x I2Cs (SMBus/PMBus)
- 11x timers: 1x 32-bit, 6x 16-bit with up to 4 IC/OC/PWM channels, 2x 16-bit basic timers, 2x watchdog timers (independent and window)
- Up to 23 capacitive sensing channels
- CRC calculation unit, 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM32L151CC	STM32L151CCT6, STM32L151CCU6
STM32L151RC ⁽¹⁾	STM32L151RCT6
STM32L151UC	STM32L151UCY6
STM32L151VC ⁽¹⁾	STM32L151VCT6, STM32L151VCH6
STM32L152CC	STM32L152CCT6, STM32L152CCU6
STM32L152RC ⁽¹⁾	STM32L152RCT6
STM32L152UC	STM32L152UCY6
STM32L152VC ⁽¹⁾	STM32L152VCT6, STM32L152VCH6

1. For sales types ending with "A" and STM32L15xC products in WLCSP64 package, please refer to STM32L15xC/C-A datasheet.

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L151xC and STM32L152xC ultra-low-power ARM® Cortex®-M3 based microcontroller product line with a Flash memory of 256 Kbytes.

The ultra-low-power STM32L151xC and STM32L152xC family includes devices in 6 different package types: from 48 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L151xC and STM32L152xC microcontroller family suitable for a wide range of applications:

- Medical and handheld equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, wired and wireless sensors, video intercom
- Utility metering

This STM32L151xC and STM32L152xC datasheet should be read in conjunction with the STM32L1xxx reference manual (RM0038). The application note “Getting started with STM32L1xxx hardware development” (AN3216) gives a hardware implementation overview. Both documents are available from the STMicroelectronics website www.st.com.

For information on the ARM® Cortex®-M3 core please refer to the ARM® Cortex®-M3 technical reference manual, available from the www.arm.com website. *Figure 1* shows the general block diagram of the device family.

2 Description

The ultra-low-power STM32L151xC and STM32L152xC devices incorporate the connectivity power of the universal serial bus (USB) with the high-performance ARM[®] Cortex[®]-M3 32-bit RISC core operating at a frequency of 32 MHz (33.3 DMIPS), a memory protection unit (MPU), high-speed embedded memories (Flash memory up to 256 Kbytes and RAM up to 32 Kbytes) and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The STM32L151xC and STM32L152xC devices offer two operational amplifiers, one 12-bit ADC, two DACs, two ultra-low-power comparators, one general-purpose 32-bit timer, six general-purpose 16-bit timers and two basic timers, which can be used as time bases.

Moreover, the STM32L151xC and STM32L152xC devices contain standard and advanced communication interfaces: up to two I2Cs, three SPIs, two I2S, three USARTs and an USB. The STM32L151xC and STM32L152xC devices offer up to 23 capacitive sensing channels to simply add a touch sensing functionality to any application.

They also include a real-time clock and a set of backup registers that remain powered in Standby mode.

Finally, the integrated LCD controller (except STM32L151xC devices) has a built-in LCD voltage generator that allows to drive up to 8 multiplexed LCDs with the contrast independent of the supply voltage.

The ultra-low-power STM32L151xC and STM32L152xC devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +85 °C and -40 to +105 °C temperature ranges. A comprehensive set of power-saving modes allows the design of low-power applications.



2.1 Device overview

Table 2. Ultra-low-power STM32L151xC and STM32L152xC device features and peripheral counts

Peripheral		STM32L15xCC	STM32L15xUC STM32L15xRC	STM32L15xVC
Flash (Kbytes)		256		
Data EEPROM (Kbytes)		8		
RAM (Kbytes)		32		
Timers	32 bit	1		
	General-purpose	6		
	Basic	2		
Communication interfaces	SPI	8(3) ⁽¹⁾		
	I ² S	2		
	I ² C	2		
	USART	3		
	USB	1		
GPIOs		37	51	83
Operation amplifiers		2		
12-bit synchronized ADC Number of channels		1 14	1 21	1 25
12-bit DAC Number of channels		2 2		
LCD ⁽²⁾ COM x SEG		1 4x18	1 4x32 or 8x28	1 4x44 or 8x40
Comparators		2		
Capacitive sensing channels		16	23	
Max. CPU frequency		32 MHz		
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V without BOR option		
Operating temperatures		Ambient operating temperature: -40 °C to 85 °C / -40 °C to 105 °C Junction temperature: -40 to + 110 °C		
Packages		LQFP48, UFQFPN48	LQFP64, WLCSP63	LQFP100, UFBGA100

1. 5 SPIs are USART configured in synchronous mode emulating SPI master.

2. STM32L152xx devices only.

2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of cores and features. From proprietary 8-bit to up to Cortex-M3, including the Cortex-M0+, the STM32Lx series are the best choice to answer the user needs, in terms of ultra-low-power features. The STM32 ultra-low-power series are the best fit, for instance, for gas/water meter, keyboard/mouse or fitness and healthcare, wearable applications. Several built-in features like LCD drivers, dual-bank memory, Low-power run mode, op-amp, AES 128-bit, DAC, USB crystal-less and many others will clearly allow to build very cost-optimized applications by reducing BOM.

Note: STMicroelectronics as a reliable and long-term manufacturer ensures as much as possible the pin-to-pin compatibility between any STM8Lxxxx and STM32Lxxxx devices and between any of the STM32Lx and STM32Fx series. Thanks to this unprecedented scalability, the old applications can be upgraded to respond to the latest market features and efficiency demand.

2.2.1 Performance

All the families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM Cortex-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-low-power performance to range from 5 up to 33.3 DMIPs.

2.2.2 Shared peripherals

STM8L15xxx, STM32L15xxx and STM32L162xx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC, DAC and comparators
- Digital peripherals: RTC and some communication interfaces

2.2.3 Common system strategy.

To offer flexibility and optimize performance, the STM8L15xxx, STM32L15xxx and STM32L162xx family uses a common architecture:

- Same power supply range from 1.65 V to 3.6 V
- Architecture optimized to reach ultra-low consumption both in low-power modes and Run mode
- Fast startup strategy from low-power modes
- Flexible system clock
- Ultrasafe reset: same reset strategy including power-on reset, power-down reset, brownout reset and programmable voltage detector

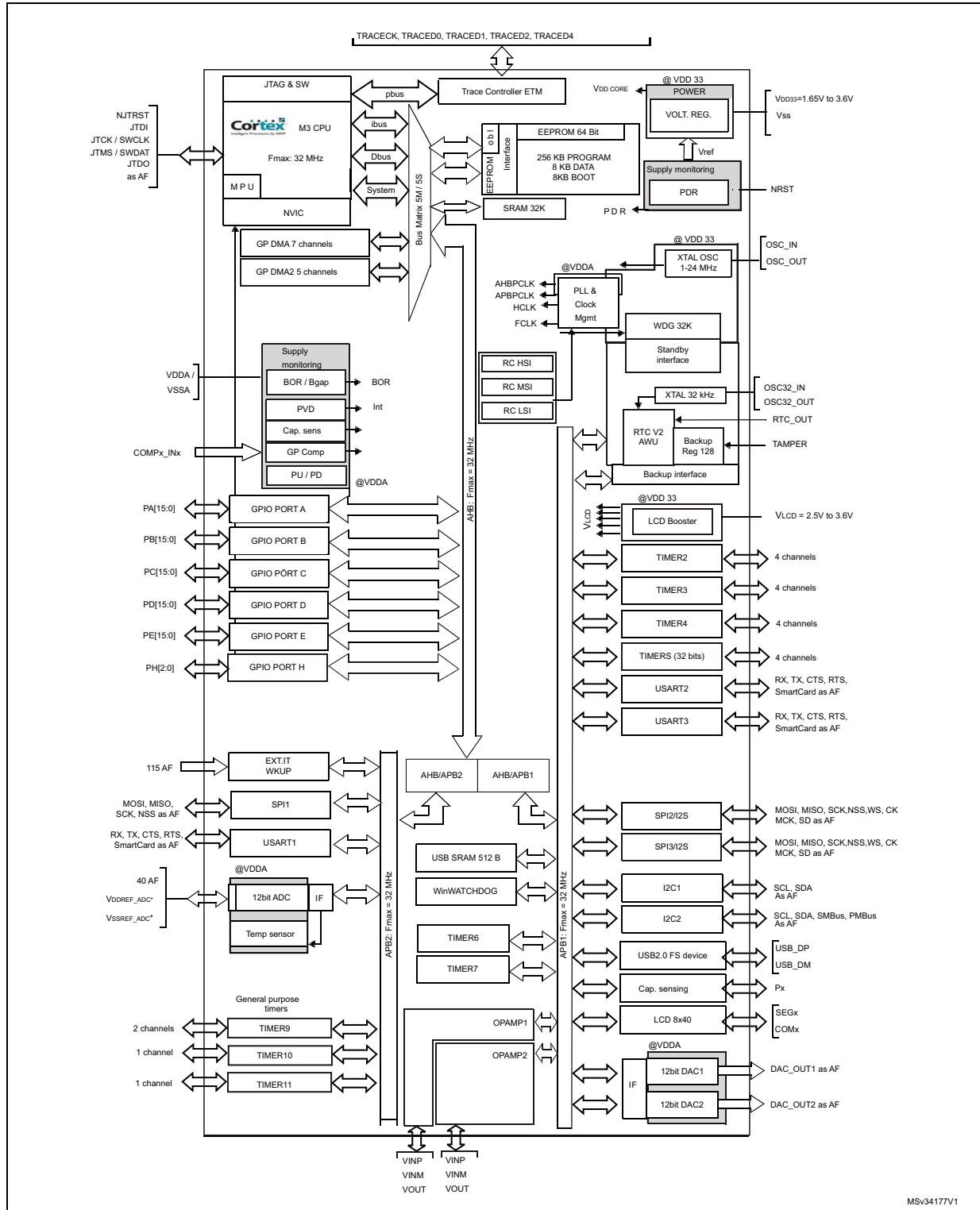
2.2.4 Features

ST ultra-low-power continuum also lies in feature compatibility:

- More than 15 packages with pin count from 20 to 144 pins and size down to 3 x 3 mm
- Memory density ranging from 2 to 512 Kbytes

3 Functional overview

Figure 1. Ultra-low-power STM32L151xC and STM32L152xC block diagram



MSx34177V1



3.1 Low-power modes

The ultra-low-power STM32L151xC and STM32L152xC devices support dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 (V_{DD} range limited to 1.71 V - 3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full V_{DD} range), with a maximum CPU frequency of 16 MHz
- Range 3 (full V_{DD} range), with a maximum CPU frequency limited to 4 MHz (generated only with the multispeed internal RC oscillator clock source)

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**
In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.
- **Low-power run mode**
This mode is achieved with the multispeed internal (MSI) RC oscillator set to the minimum clock (131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In low-power run mode, the clock frequency and the number of enabled peripherals are both limited.
- **Low-power sleep mode**
This mode is achieved by entering Sleep mode with the internal voltage regulator in Low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.
When wakeup is triggered by an event or an interrupt, the system reverts to the run mode with the regulator on.
- **Stop mode with RTC**
Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSI RC and HSE crystal oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.
The device can be woken up from Stop mode by any of the EXTI line, in 8 μ s. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on), it can be the RTC alarm(s), the USB wakeup, the RTC tamper events, the RTC timestamp event or the RTC wakeup.

- Stop mode without RTC**
 Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, LSE and HSE crystal oscillators are disabled. The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8 μs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.
- Standby mode with RTC**
 Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).
 The device exits Standby mode in 60 μs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.
- Standby mode without RTC**
 Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).
 The device exits Standby mode in 60 μs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

Operating power supply range	Functionalities depending on the operating power supply range			
	DAC and ADC operation	USB	Dynamic voltage scaling range	I/O operation
V _{DD} =V _{DDA} = 1.65 to 1.71 V	Not functional	Not functional	Range 2 or Range 3	Degraded speed performance
V _{DD} =V _{DDA} = 1.71 to 1.8 V ⁽¹⁾	Not functional	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance
V _{DD} =V _{DDA} = 1.8 to 2.0 V ⁽¹⁾	Conversion time up to 500 Ksps	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance

Table 3. Functionalities depending on the operating power supply range (continued)

Operating power supply range	Functionalities depending on the operating power supply range			
	DAC and ADC operation	USB	Dynamic voltage scaling range	I/O operation
$V_{DD}=V_{DDA} = 2.0$ to 2.4 V	Conversion time up to 500 Ksps	Functional ⁽²⁾	Range 1, Range 2 or Range 3	Full speed operation
$V_{DD}=V_{DDA} = 2.4$ to 3.6 V	Conversion time up to 1 Msp/s	Functional ⁽²⁾	Range 1, Range 2 or Range 3	Full speed operation

1. CPU frequency changes from initial to final must respect " $F_{CPU\ initial} < 4 * F_{CPU\ final}$ " to limit V_{CORE} drop due to current consumption peak when frequency increases. It must also respect 5 μ s delay between two changes. For example to switch from 4.2 MHz to 32 MHz, the user can switch from 4.2 MHz to 16 MHz, wait 5 μ s, then switch from 16 MHz to 32 MHz.
2. Should be USB compliant from I/O voltage standpoint, the minimum V_{DD} is 3.0 V.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
2.1MHz to 4.2 MHz (1ws) 32 kHz to 2.1 MHz (0ws)	Range 3

Table 5. Functionalities depending on the working mode (from Run/active down to standby)

Ips	Run/Active	Sleep	Low-power Run	Low-power Sleep	Stop		Standby	
					Wakeup capability	Wakeup capability		
CPU	Y	--	Y	--	--	--	--	--
Flash	Y	Y	Y	Y	--	--	--	--
RAM	Y	Y	Y	Y	Y	--	--	--
Backup Registers	Y	Y	Y	Y	Y	--	Y	--
EEPROM	Y	Y	Y	Y	Y	--	--	--
Brown-out rest (BOR)	Y	Y	Y	Y	Y	Y	Y	--
DMA	Y	Y	Y	Y	--	--	--	--
Programmable Voltage Detector (PVD)	Y	Y	Y	Y	Y	Y	Y	--
Power On Reset (POR)	Y	Y	Y	Y	Y	Y	Y	--
Power Down Rest (PDR)	Y	Y	Y	Y	Y	--	Y	--
High Speed Internal (HSI)	Y	Y	--	--	--	--	--	--
High Speed External (HSE)	Y	Y	--	--	--	--	--	--
Low Speed Internal (LSI)	Y	Y	Y	Y	Y	--	Y	--
Low Speed External (LSE)	Y	Y	Y	Y	Y	--	Y	--
Multi-Speed Internal (MSI)	Y	Y	Y	Y	--	--	--	--
Inter-Connect Controller	Y	Y	Y	Y	--	--	--	--
RTC	Y	Y	Y	Y	Y	Y	Y	--
RTC Tamper	Y	Y	Y	Y	Y	Y	Y	Y
Auto WakeUp (AWU)	Y	Y	Y	Y	Y	Y	Y	Y
LCD	Y	Y	Y	Y	Y	--	--	--
USB	Y	Y	--	--	--	Y	--	--
USART	Y	Y	Y	Y	Y	(1)	--	--
SPI	Y	Y	Y	Y	--	--	--	--
I2C	Y	Y	Y	Y	--	(1)	--	--

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)

Ips	Run/Active	Sleep	Low-power Run	Low-power Sleep	Stop		Standby	
					Wakeup capability	Wakeup capability		
ADC	Y	Y	--	--	--	--	--	--
DAC	Y	Y	Y	Y	Y	--	--	--
Tempsensor	Y	Y	Y	Y	Y	--	--	--
OP amp	Y	Y	Y	Y	Y	--	--	--
Comparators	Y	Y	Y	Y	Y	Y	--	--
16-bit and 32-bit Timers	Y	Y	Y	Y	--	--	--	--
IWDG	Y	Y	Y	Y	Y	Y	Y	Y
WWDG	Y	Y	Y	Y	--	--	--	--
Touch sensing	Y	Y	--	--	--	--	--	--
Systic Timer	Y	Y	Y	Y		--	--	--
GPIOs	Y	Y	Y	Y	Y	Y	--	3 pins
Wakeup time to Run mode	0 μs	0.4 μs	3 μs	46 μs	< 8 μs		58 μs	
Consumption V _{DD} =1.8 to 3.6 V (Typ)	Down to 185 μA/MHz (from Flash)	Down to 34.5 μA/MHz (from Flash)	Down to 8.6 μA	Down to 4.4 μA	0.43 μA (no RTC) V _{DD} =1.8V		0.29 μA (no RTC) V _{DD} =1.8V	
					1.15 μA (with RTC) V _{DD} =1.8V		0.9 μA (with RTC) V _{DD} =1.8V	
					0.44 μA (no RTC) V _{DD} =3.0V		0.29 μA (no RTC) V _{DD} =3.0V	
					1.4 μA (with RTC) V _{DD} =3.0V		1.15 μA (with RTC) V _{DD} =3.0V	

1. The startup on communication line wakes the CPU which was made possible by an EXTI, this induces a delay before entering run mode.

3.2 ARM[®] Cortex[®]-M3 core with MPU

The ARM[®] Cortex[®]-M3 processor is the industry leading processor for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM[®] Cortex[®]-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The memory protection unit (MPU) improves system reliability by defining the memory attributes (such as read/write access permissions) for different memory regions. It provides up to eight different regions and an optional predefined background region.

Owing to its embedded ARM core, the STM32L151xC and STM32L152xC devices are compatible with all ARM tools and software.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L151xC and STM32L152xC devices embed a nested vectored interrupt controller able to handle up to 53 maskable interrupt channels (not including the 16 interrupt lines of ARM[®] Cortex[®]-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving*, higher-priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.3 Reset and supply management

3.3.1 Power supply schemes

- $V_{DD} = 1.65$ to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA} , $V_{DDA} = 1.65$ to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

The device exists in two versions:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the V_{DD} min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the

power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wake-up logic, IWDG, RTC, LSI, LSE crystal 32K osc, RCC_CSR).

3.3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using USART1, USART2 or USB. See Application note “STM32 microcontroller system memory boot mode” (AN2606) for details.

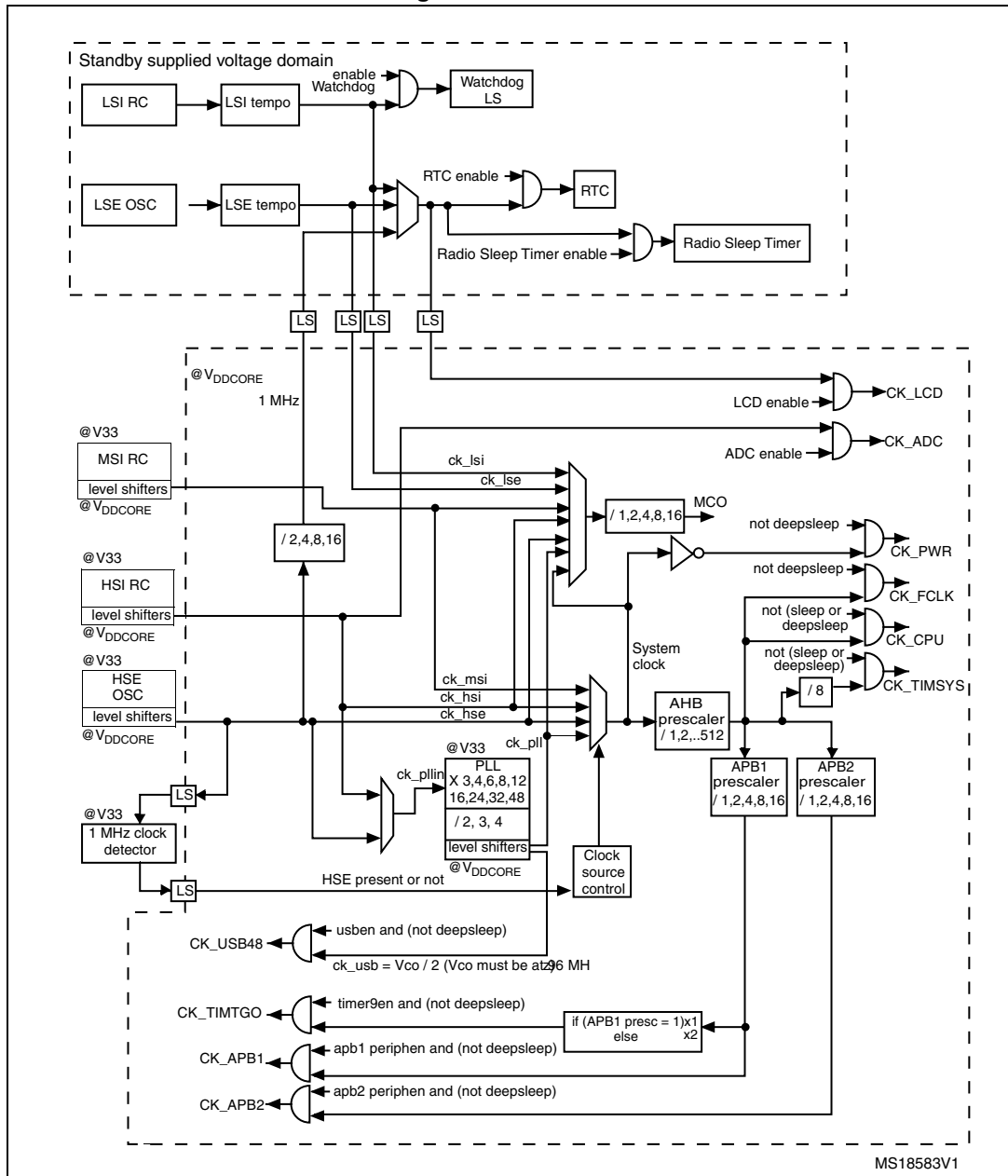
3.4 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** three different clock sources can be used to drive the master clock SYSCLK:
 - 1-24 MHz high-speed external crystal (HSE), that can supply a PLL
 - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
 - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz). When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a $\pm 0.5\%$ accuracy.
- **Auxiliary clock source:** two ultra-low-power clock sources that can be used to drive the LCD controller and the real-time clock:
 - 32.768 kHz low-speed external crystal (LSE)
 - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- **RTC and LCD clock sources:** the LSI, LSE or HSE sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **USB clock source:** the embedded PLL has a dedicated 48 MHz clock output to supply the USB interface.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.
- **Clock-out capability (MCO: microcontroller clock output):** it outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See [Figure 2](#) for details on the clock tree.

Figure 2. Clock tree



3.5 Low-power real-time clock and backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the sub-second, second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are made automatically. The RTC provides two programmable alarms and programmable periodic interrupts with wakeup from Stop and Standby modes.

The programmable wakeup time ranges from 120 μ s to 36 hours.

The RTC can be calibrated with an external 512 Hz output, and a digital compensation circuit helps reduce drift due to crystal deviation.

The RTC can also be automatically corrected with a 50/60Hz stable powerline.

The RTC calendar can be updated on the fly down to sub second precision, which enables network system synchronization.

A time stamp can record an external event occurrence, and generates an interrupt.

There are thirty-two 32-bit backup registers provided to store 128 bytes of user application data. They are cleared in case of tamper detection.

Three pins can be used to detect tamper events. A change on one of these pins can reset backup register and generate an interrupt. To prevent false tamper event, like ESD event, these three tamper inputs can be digitally filtered.

3.6 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated AFIO registers. All GPIOs are high current capable. The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to the AHB with a toggling speed of up to 16 MHz.

External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 83 GPIOs can be connected to the 16 external interrupt lines. The 8 other lines are connected to RTC, PVD, USB, comparator events or capacitive sensing acquisition.

3.7 Memories

The STM32L151xC and STM32L152xC devices have the following features:

- 32 Kbytes of embedded RAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
 - 256 Kbytes of embedded Flash program memory
 - 8 Kbytes of data EEPROM
 - Options bytes

The options bytes are used to write-protect or read-out protect the memory (with 4 Kbytes granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no readout protection
- Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- Level 2: chip readout protection, debug features (ARM Cortex-M3 JTAG and serial wire) and boot in RAM selection disabled (JTAG fuse)

The whole non-volatile memory embeds the error correction code (ECC) feature.

The user area of the Flash memory can be protected against Dbus read access by PCROP feature (see RM0038 for details).

3.8 DMA (direct memory access)

The flexible 12-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I²C, USART, general-purpose timers, DAC and ADC.

3.9 LCD (liquid crystal display)

The LCD drives up to 8 common terminals and 44 segment terminals to drive up to 320 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD} . This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode
- V_{LCD} rail decoupling capability

Table 6. V_{LCD} rail decoupling

	Bias			Pin	
	1/2	1/3	1/4		
$V_{LCDRAIL1}$	1/2 V_{LCD}	2/3 V_{LCD}	1/2 V_{LCD}	PB2	
$V_{LCDRAIL2}$	N/A	1/3 V_{LCD}	1/4 V_{LCD}	PB12	PE11
$V_{LCDRAIL3}$	N/A	N/A	3/4 V_{LCD}	PB0	PE12

3.10 ADC (analog-to-digital converter)

A 12-bit analog-to-digital converters is embedded into STM32L151xC and STM32L152xC devices with up to 25 external channels, performing conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs with up to 24 external channels in a group.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers. An injection mode allows high priority conversions to be done by interrupting a scan mode which runs in as a background task.

The ADC includes a specific low-power mode. The converter is able to operate at maximum speed even if the CPU is operating at a very low frequency and has an auto-shutdown function. The ADC's runtime and analog front-end current consumption are thus minimized whatever the MCU operating mode.