



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

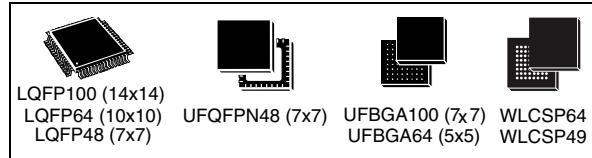


Ultra-low-power ARM[®] Cortex[®]-M4 32-bit MCU+FPU, 100DMIPS, 256KB Flash, 64KB SRAM, USB FS, LCD, analog, audio, AES

Datasheet - production data

Features

- Ultra-low-power with FlexPowerControl
 - 1.71 V to 3.6 V power supply
 - -40 °C to 85/105/125 °C temperature range
 - 200 nA in V_{BAT} mode: supply for RTC and 32x32-bit backup registers
 - 8 nA Shutdown mode (5 wakeup pins)
 - 28 nA Standby mode (5 wakeup pins)
 - 280 nA Standby mode with RTC
 - 1.0 µA Stop 2 mode, 1.28 µA Stop 2 with RTC
 - 84 µA/MHz run mode
 - Batch acquisition mode (BAM)
 - 4 µs wakeup from Stop mode
 - Brown out reset (BOR) in all modes except shutdown
 - Interconnect matrix
- Core: ARM[®] 32-bit Cortex[®]-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait-state execution from Flash memory, frequency up to 80 MHz, MPU, 100DMIPS/1.25DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Performance Benchmark
 - 1.25 DMIPS/MHz (Dhrystone 2.1)
 - 273.55 Coremark[®] (3.42 Coremark/MHz @ 80 MHz)
- Energy Benchmark
 - 176.7 ULPBench[®] score
- Clock Sources
 - 4 to 48 MHz crystal oscillator
 - 32 kHz crystal oscillator for RTC (LSE)
 - Internal 16 MHz factory-trimmed RC (±1%)
 - Internal low-power 32 kHz RC (±5%)
 - Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than ±0.25 % accuracy)
 - Internal 48 MHz with clock recovery



- 2 PLLs for system clock, USB, audio, ADC
- RTC with HW calendar, alarms and calibration
- LCD 8 × 40 or 4 × 44 with step-up converter
- Up to 21 capacitive sensing channels: support touchkey, linear and rotary touch sensors
- 11x timers: 1x 16-bit advanced motor-control, 1x 32-bit and 2x 16-bit general purpose, 2x 16-bit basic, 2x low-power 16-bit timers (available in Stop mode), 2x watchdogs, SysTick timer
- Up to 83 fast I/Os, most 5 V-tolerant
- Memories
 - 256 KB single bank Flash, proprietary code readout protection
 - 64 KB of SRAM including 16 KB with hardware parity check
 - Quad SPI memory interface
- Rich analog peripherals (independent supply)
 - 1× 12-bit ADC 5 Msps, up to 16-bit with hardware oversampling, 200 µA/Msps
 - 2x 12-bit DAC, low-power sample and hold
 - 1x operational amplifier with built-in PGA
 - 2x ultra-low-power comparators
- 15x communication interfaces
 - USB 2.0 full-speed crystal less solution with LPM and BCD
 - 1x SAI (serial audio interface)
 - 3x I2C FM+(1 Mbit/s), SMBus/PMBus
 - 4x USARTs (ISO 7816, LIN, IrDA, modem)
 - 3x SPIs (4x SPIs with the Quad SPI)
 - CAN (2.0B Active) and SDMMC interface
 - SWPMI single wire protocol master I/F
- 14-channel DMA controller
- True random number generator

- CRC calculation unit, 96-bit unique ID
- AES: 128/256-bit key encryption hardware accelerator
- Development support: serial wire debug (SWD), JTAG, Embedded Trace Macrocell™

Contents

1	Introduction	12
2	Description	13
3	Functional overview	17
3.1	ARM® Cortex®-M4 core with FPU	17
3.2	Adaptive real-time memory accelerator (ART Accelerator™)	17
3.3	Memory protection unit	17
3.4	Embedded Flash memory	18
3.5	Embedded SRAM	19
3.6	Firewall	19
3.7	Boot modes	20
3.8	Cyclic redundancy check calculation unit (CRC)	20
3.9	Power supply management	20
3.9.1	Power supply schemes	20
3.9.2	Power supply supervisor	21
3.9.3	Voltage regulator	22
3.9.4	Low-power modes	22
3.9.5	Reset mode	26
3.9.6	VBAT operation	26
3.10	Interconnect matrix	27
3.11	Clocks and startup	29
3.12	General-purpose inputs/outputs (GPIOs)	32
3.13	Direct memory access controller (DMA)	32
3.14	Interrupts and events	33
3.14.1	Nested vectored interrupt controller (NVIC)	33
3.14.2	Extended interrupt/event controller (EXTI)	33
3.15	Analog to digital converter (ADC)	34
3.15.1	Temperature sensor	34
3.15.2	Internal voltage reference (VREFINT)	35
3.15.3	VBAT battery voltage monitoring	35
3.16	Digital to analog converter (DAC)	35

3.17	Voltage reference buffer (VREFBUF)	36
3.18	Comparators (COMP)	36
3.19	Operational amplifier (OPAMP)	37
3.20	Touch sensing controller (TSC)	37
3.21	Liquid crystal display controller (LCD)	38
3.22	Random number generator (RNG)	38
3.23	Advanced encryption standard hardware accelerator (AES)	38
3.24	Timers and watchdogs	39
3.24.1	Advanced-control timer (TIM1)	40
3.24.2	General-purpose timers (TIM2, TIM15, TIM16)	40
3.24.3	Basic timers (TIM6 and TIM7)	40
3.24.4	Low-power timer (LPTIM1 and LPTIM2)	41
3.24.5	Independent watchdog (IWDG)	41
3.24.6	System window watchdog (WWDG)	41
3.24.7	SysTick timer	41
3.25	Real-time clock (RTC) and backup registers	42
3.26	Inter-integrated circuit interface (I ² C)	43
3.27	Universal synchronous/asynchronous receiver transmitter (USART) ...	44
3.28	Low-power universal asynchronous receiver transmitter (LPUART) ...	45
3.29	Serial peripheral interface (SPI)	46
3.30	Serial audio interfaces (SAI)	46
3.31	Single wire protocol master interface (SWPMI)	47
3.32	Controller area network (CAN)	47
3.33	Secure digital input/output and MultiMediaCards Interface (SDMMC) ...	48
3.34	Universal serial bus (USB)	48
3.35	Clock recovery system (CRS)	49
3.36	Quad SPI memory interface (QUADSPI)	49
3.37	Development support	50
3.37.1	Serial wire JTAG debug port (SWJ-DP)	50
3.37.2	Embedded Trace Macrocell™	50
4	Pinouts and pin description	51
5	Memory mapping	77

6	Electrical characteristics	81
6.1	Parameter conditions	81
6.1.1	Minimum and maximum values	81
6.1.2	Typical values	81
6.1.3	Typical curves	81
6.1.4	Loading capacitor	81
6.1.5	Pin input voltage	81
6.1.6	Power supply scheme	82
6.1.7	Current consumption measurement	83
6.2	Absolute maximum ratings	83
6.3	Operating conditions	85
6.3.1	General operating conditions	85
6.3.2	Operating conditions at power-up / power-down	86
6.3.3	Embedded reset and power control block characteristics	86
6.3.4	Embedded voltage reference	89
6.3.5	Supply current characteristics	91
6.3.6	Wakeup time from low-power modes and voltage scaling transition times	111
6.3.7	External clock source characteristics	114
6.3.8	Internal clock source characteristics	119
6.3.9	PLL characteristics	126
6.3.10	Flash memory characteristics	127
6.3.11	EMC characteristics	128
6.3.12	Electrical sensitivity characteristics	129
6.3.13	I/O current injection characteristics	130
6.3.14	I/O port characteristics	131
6.3.15	NRST pin characteristics	137
6.3.16	Analog switches booster	138
6.3.17	Analog-to-Digital converter characteristics	139
6.3.18	Digital-to-Analog converter characteristics	152
6.3.19	Voltage reference buffer characteristics	156
6.3.20	Comparator characteristics	158
6.3.21	Operational amplifiers characteristics	159
6.3.22	Temperature sensor characteristics	162
6.3.23	V _{BAT} monitoring characteristics	162
6.3.24	LCD controller characteristics	163
6.3.25	Timer characteristics	164

	6.3.26	Communication interfaces characteristics	165
7		Package information	178
	7.1	LQFP100 package information	178
	7.2	UFBGA100 package information	181
	7.3	LQFP64 package information	184
	7.4	UFBGA64 package information	187
	7.5	WLCSP64 package information	190
	7.6	WLCSP49 package information	193
	7.7	LQFP48 package information	196
	7.8	UFQFPN48 package information	199
	7.9	Thermal characteristics	202
		7.9.1 Reference document	202
		7.9.2 Selecting the product temperature range	203
8		Part numbering	205
9		Revision history	206

List of tables

Table 1.	STM32L443xx family device features and peripheral counts	14
Table 2.	Access status versus readout protection level and execution modes.	18
Table 3.	Functionalities depending on the working mode.	24
Table 4.	STM32L443xx peripherals interconnect matrix	27
Table 5.	DMA implementation	32
Table 6.	Temperature sensor calibration values.	35
Table 7.	Internal voltage reference calibration values	35
Table 8.	Timer feature comparison.	39
Table 9.	I2C implementation	43
Table 10.	STM32L443xx USART/LPUART features	44
Table 11.	SAI implementation.	47
Table 12.	Legend/abbreviations used in the pinout table	55
Table 13.	STM32L443xx pin definitions	55
Table 14.	Alternate function AF0 to AF7 (for AF8 to AF15 see Table 15)	66
Table 15.	Alternate function AF8 to AF15 (for AF0 to AF7 see Table 14)	71
Table 16.	STM32L443xx memory map and peripheral register boundary addresses	78
Table 17.	Voltage characteristics	83
Table 18.	Current characteristics	84
Table 19.	Thermal characteristics.	84
Table 20.	General operating conditions	85
Table 21.	Operating conditions at power-up / power-down	86
Table 22.	Embedded reset and power control block characteristics.	87
Table 23.	Embedded internal voltage reference.	89
Table 24.	Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF)	92
Table 25.	Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART disable	93
Table 26.	Current consumption in Run and Low-power run modes, code with data processing running from SRAM1	94
Table 27.	Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF)	95
Table 28.	Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART disable	96
Table 29.	Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1	96
Table 30.	Current consumption in Sleep and Low-power sleep modes, Flash ON	97
Table 31.	Current consumption in Low-power sleep modes, Flash in power-down	98
Table 32.	Current consumption in Stop 2 mode	98
Table 33.	Current consumption in Stop 1 mode	101
Table 34.	Current consumption in Stop 0	103
Table 35.	Current consumption in Standby mode	104
Table 36.	Current consumption in Shutdown mode	105
Table 37.	Current consumption in VBAT mode	107
Table 38.	Peripheral current consumption	109
Table 39.	Low-power mode wakeup timings	112
Table 40.	Regulator modes transition times	113
Table 41.	Wakeup time using USART/LPUART.	113
Table 42.	High-speed external user clock characteristics.	114

Table 43.	Low-speed external user clock characteristics	115
Table 44.	HSE oscillator characteristics	116
Table 45.	LSE oscillator characteristics ($f_{LSE} = 32.768$ kHz)	117
Table 46.	HSI16 oscillator characteristics	119
Table 47.	MSI oscillator characteristics	121
Table 48.	HSI48 oscillator characteristics	124
Table 49.	LSI oscillator characteristics	125
Table 50.	PLL, PLLSAI1 characteristics	126
Table 51.	Flash memory characteristics	127
Table 52.	Flash memory endurance and data retention	127
Table 53.	EMS characteristics	128
Table 54.	EMI characteristics	129
Table 55.	ESD absolute maximum ratings	129
Table 56.	Electrical sensitivities	130
Table 57.	I/O current injection susceptibility	130
Table 58.	I/O static characteristics	131
Table 59.	Output voltage characteristics	134
Table 60.	I/O AC characteristics	135
Table 61.	NRST pin characteristics	137
Table 62.	Analog switches booster characteristics	138
Table 63.	ADC characteristics	139
Table 64.	Maximum ADC RAIN	141
Table 65.	ADC accuracy - limited test conditions 1	143
Table 66.	ADC accuracy - limited test conditions 2	145
Table 67.	ADC accuracy - limited test conditions 3	147
Table 68.	ADC accuracy - limited test conditions 4	149
Table 69.	DAC characteristics	152
Table 70.	DAC accuracy	154
Table 71.	VREFBUF characteristics	156
Table 72.	COMP characteristics	158
Table 73.	OPAMP characteristics	159
Table 74.	TS characteristics	162
Table 75.	V_{BAT} monitoring characteristics	162
Table 76.	V_{BAT} charging characteristics	162
Table 77.	LCD controller characteristics	163
Table 78.	TIMx characteristics	164
Table 79.	IWDG min/max timeout period at 32 kHz (LSI)	164
Table 80.	WWDG min/max timeout value at 80 MHz (PCLK)	165
Table 81.	I2C analog filter characteristics	165
Table 82.	SPI characteristics	166
Table 83.	Quad SPI characteristics in SDR mode	169
Table 84.	QUADSPI characteristics in DDR mode	170
Table 85.	SAI characteristics	172
Table 86.	SD / MMC dynamic characteristics, $V_{DD} = 2.7$ V to 3.6 V	174
Table 87.	eMMC dynamic characteristics, $V_{DD} = 1.71$ V to 1.9 V	175
Table 88.	USB electrical characteristics	177
Table 89.	SWPMI electrical characteristics	177
Table 90.	LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data	178
Table 91.	UFPGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data	181
Table 92.	UFPGA100 recommended PCB design rules (0.5 mm pitch BGA)	182

Table 93.	LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data	184
Table 94.	UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package mechanical data	187
Table 95.	UFBGA64 recommended PCB design rules (0.5 mm pitch BGA)	188
Table 96.	WLCSP64 - 64-ball, 3.141 x 3.127 mm, 0.35 mm pitch wafer level chip scale package mechanical data	190
Table 97.	WLCSP64 recommended PCB design rules (0.35 mm pitch)	191
Table 98.	WLCSP49 - 49-ball, 3.141 x 3.127 mm, 0.4 mm pitch wafer level chip scale package mechanical data	194
Table 99.	WLCSP49 recommended PCB design rules (0.4 mm pitch)	195
Table 100.	LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data	197
Table 101.	UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data	200
Table 102.	Package thermal characteristics	202
Table 103.	STM32L443xx ordering information scheme	205
Table 104.	Document revision history	206

List of figures

Figure 1.	STM32L443xx block diagram	16
Figure 2.	Power supply overview	21
Figure 3.	Clock tree	31
Figure 4.	Voltage reference buffer	36
Figure 5.	STM32L443Vx LQFP100 pinout ⁽¹⁾	51
Figure 6.	STM32L443Vx UFBGA100 ballout ⁽¹⁾	52
Figure 7.	STM32L443Rx LQFP64 pinout ⁽¹⁾	52
Figure 8.	STM32L443Rx UFBGA64 ballout ⁽¹⁾	53
Figure 9.	STM32L443Rx WLCSP64 pinout ⁽¹⁾	53
Figure 10.	STM32L443Cx WLCSP49 pinout ⁽¹⁾	53
Figure 11.	STM32L443Cx LQFP48 pinout ⁽¹⁾	54
Figure 12.	STM32L443Cx UFQFPN48 pinout ⁽¹⁾	54
Figure 13.	STM32L443xx memory map	77
Figure 14.	Pin loading conditions	81
Figure 15.	Pin input voltage	81
Figure 16.	Power supply scheme	82
Figure 17.	Current consumption measurement scheme	83
Figure 18.	VREFINT versus temperature	90
Figure 19.	High-speed external clock source AC timing diagram	114
Figure 20.	Low-speed external clock source AC timing diagram	115
Figure 21.	Typical application with an 8 MHz crystal	117
Figure 22.	Typical application with a 32.768 kHz crystal	118
Figure 23.	HSI16 frequency versus temperature	120
Figure 24.	Typical current consumption versus MSI frequency	124
Figure 25.	HSI48 frequency versus temperature	125
Figure 26.	I/O input characteristics	132
Figure 27.	I/O AC characteristics definition ⁽¹⁾	137
Figure 28.	Recommended NRST pin protection	138
Figure 29.	ADC accuracy characteristics	151
Figure 30.	Typical connection diagram using the ADC	151
Figure 31.	12-bit buffered / non-buffered DAC	154
Figure 32.	SPI timing diagram - slave mode and CPHA = 0	167
Figure 33.	SPI timing diagram - slave mode and CPHA = 1	168
Figure 34.	SPI timing diagram - master mode	168
Figure 35.	Quad SPI timing diagram - SDR mode	171
Figure 36.	Quad SPI timing diagram - DDR mode	171
Figure 37.	SAI master timing waveforms	173
Figure 38.	SAI slave timing waveforms	174
Figure 39.	SDIO high-speed mode	175
Figure 40.	SD default mode	176
Figure 41.	LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline	178
Figure 42.	LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint	180
Figure 43.	LQFP100 marking (package top view)	180
Figure 44.	UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline	181
Figure 45.	UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint	182

Figure 46.	UFBGA100 marking (package top view)	183
Figure 47.	LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline	184
Figure 48.	LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint.	185
Figure 49.	LQFP64 marking (package top view)	186
Figure 50.	UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package outline.	187
Figure 51.	UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package recommended footprint	188
Figure 52.	UFBGA64 marking (package top view)	189
Figure 53.	WLCSP64 - 64-ball, 3.141 x 3.127 mm, 0.35 mm pitch wafer level chip scale package outline.	190
Figure 54.	WLCSP64 - 64-ball, 3.141 x 3.127 mm, 0.35 mm pitch wafer level chip scale package recommended footprint	191
Figure 55.	WLCSP64 marking (package top view)	192
Figure 56.	WLCSP49 - 49-ball, 3.141 x 3.127 mm, 0.4 mm pitch wafer level chip scale package outline.	193
Figure 57.	WLCSP49 - 49-ball, 3.141 x 3.127 mm, 0.4 mm pitch wafer level chip scale package recommended footprint	194
Figure 58.	WLCSP49 marking (package top view)	195
Figure 59.	LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline	196
Figure 60.	LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint.	198
Figure 61.	LQFP48 marking (package top view)	198
Figure 62.	UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline.	199
Figure 63.	UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint	200
Figure 64.	UFQFPN48 marking (package top view)	201
Figure 65.	LQFP64 P _D max vs. T _A	204

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L443xx microcontrollers.

This document should be read in conjunction with the STM32L4x3 reference manual (RM0394). The reference manual is available from the STMicroelectronics website www.st.com.

For information on the ARM® Cortex®-M4 core, please refer to the Cortex®-M4 Technical Reference Manual, available from the www.arm.com website.



2 Description

The STM32L443xx devices are the ultra-low-power microcontrollers based on the high-performance ARM[®] Cortex[®]-M4 32-bit RISC core operating at a frequency of up to 80 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32L443xx devices embed high-speed memories (256 Kbyte of Flash memory, 64 Kbyte of SRAM), a Quad SPI flash memories interface (available on all packages) and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The STM32L443xx devices embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, proprietary code readout protection and Firewall.

The devices offer a fast 12-bit ADC (5 Msps), two comparators, one operational amplifier, two DAC channels, an internal voltage reference buffer, a low-power RTC, one general-purpose 32-bit timer, one 16-bit PWM timer dedicated to motor control, four general-purpose 16-bit timers, and two 16-bit low-power timers.

In addition, up to 21 capacitive sensing channels are available. The devices also embed an integrated LCD driver 8x40 or 4x44, with internal step-up converter.

They also feature standard and advanced communication interfaces.

- Three I2Cs
- Three SPIs
- Three USARTs and one Low-Power UART.
- One SAI (Serial Audio Interfaces)
- One SDMMC
- One CAN
- One USB full-speed device crystal less
- One SWPMI (Single Wire Protocol Master Interface)

The STM32L443xx devices embed AES hardware accelerator.

The STM32L443xx operates in the -40 to +85 °C (+105 °C junction), -40 to +105 °C (+125 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported: analog independent supply input for ADC, DAC, OPAMPs and comparators, and 3.3 V dedicated supply input for USB_A VBAT input allows to backup the RTC and backup registers.

The STM32L443xx family offers eight packages from 48 to 100-pin packages.

Table 1. STM32L443xx family device features and peripheral counts

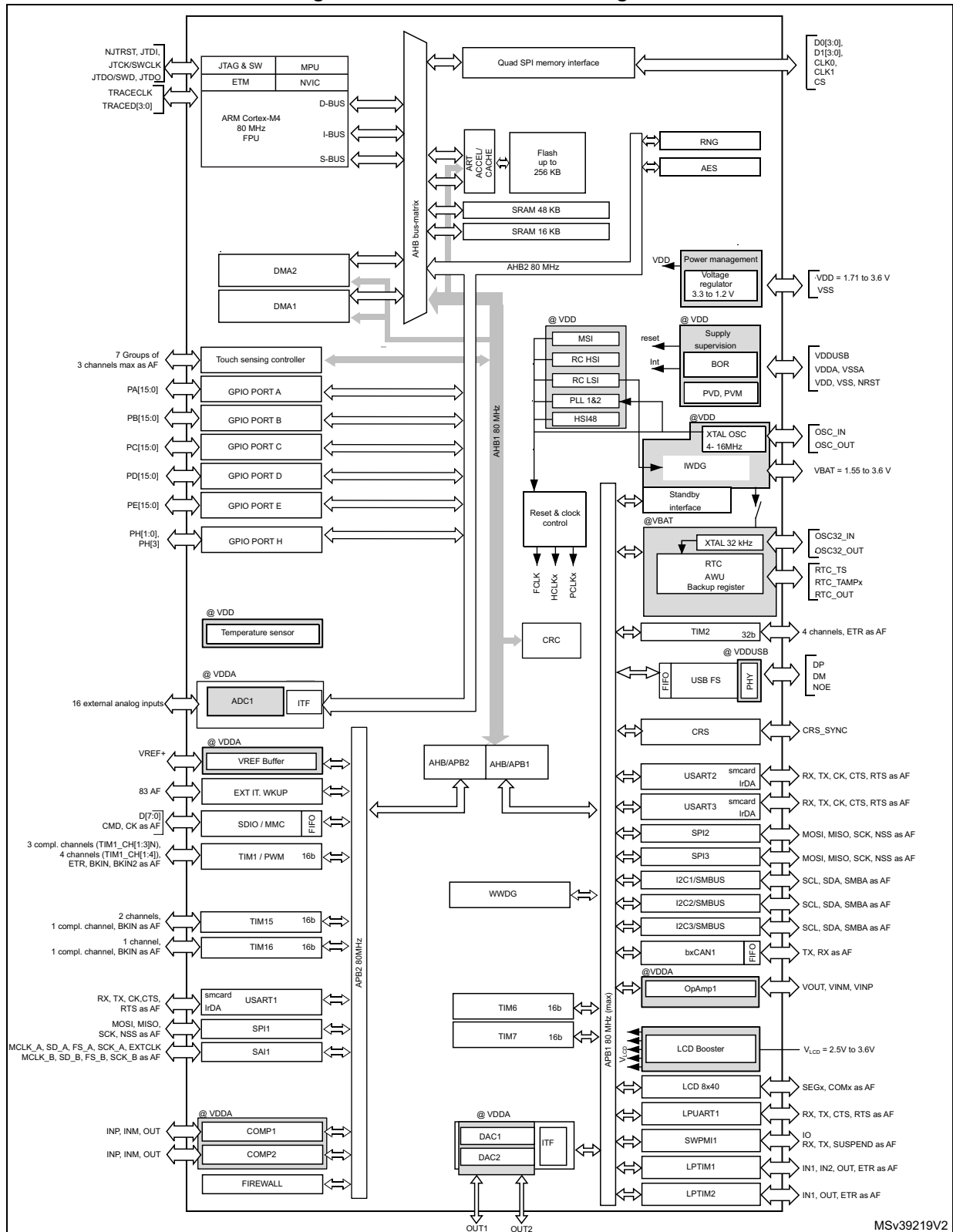
Peripheral		STM32L443Vx	STM32L443Rx	STM32L443Cx
Flash memory		256KB		
SRAM		64KB		
Quad SPI		Yes		
Timers	Advanced control	1 (16-bit)		
	General purpose	2 (16-bit) 1 (32-bit)		
	Basic	2 (16-bit)		
	Low -power	2 (16-bit)		
	SysTick timer	1		
	Watchdog timers (independent, window)	2		
Comm. interfaces	SPI	3		
	I ² C	3		
	USART LPUART	3 1		
	SAI	1		
	CAN	1		
	USB FS	Yes		
	SDMMC	Yes	No	
	SWPMI	Yes		
RTC		Yes		
Tamper pins		3	2	2
LCD COM x SEG		Yes 8x40 or 4x44	Yes 8x28 or 4x32	Yes 4x19
Random generator		Yes		
AES		Yes		
GPIOs		83	52	38 or 39 ⁽¹⁾
Wakeup pins		5	4	3
Capacitive sensing Number of channels		21	12	6
12-bit ADCs Number of channels		1 16	1 16	1 10
12-bit DAC channels		2		
Internal voltage reference buffer		Yes	No	
Analog comparator		2		
Operational amplifiers		1		

Table 1. STM32L443xx family device features and peripheral counts (continued)

Peripheral	STM32L443Vx	STM32L443Rx	STM32L443Cx
Max. CPU frequency	80 MHz		
Operating voltage	1.71 to 3.6 V		
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 105 °C / -40 to 125 °C Junction temperature: -40 to 105 °C / -40 to 125 °C / -40 to 130 °C		
Packages	LQFP100 UFBGA100	WLCSP64 LQFP64 UFBGA64	WLCSP49 LQFP48 UFQFPN48

1. For WLCSP49 package.

Figure 1. STM32L443xx block diagram



Note: AF: alternate function on I/O pins.

3 Functional overview

3.1 ARM[®] Cortex[®]-M4 core with FPU

The ARM[®] Cortex[®]-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM[®] Cortex[®]-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32L443xx family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32L443xx family devices.

3.2 Adaptive real-time memory accelerator (ART Accelerator[™])

The ART Accelerator[™] is a memory accelerator which is optimized for STM32 industry-standard ARM[®] Cortex[®]-M4 processors. It balances the inherent performance advantage of the ARM[®] Cortex[®]-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor near 100 DMIPS performance at 80MHz, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 64-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 80 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded Flash memory

STM32L443xx devices feature 256 Kbyte of embedded Flash memory available for storing programs and data in single bank architecture. The Flash memory contains 128 pages of 2 Kbyte.

Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
 - Level 0: no readout protection
 - Level 1: memory readout protection: the Flash memory cannot be read from or written to if either debug features are connected, boot in RAM or bootloader is selected
 - Level 2: chip readout protection: debug features (Cortex-M4 JTAG and serial wire), boot in RAM and bootloader selection are disabled (JTAG fuse). This selection is irreversible.

Table 2. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A ⁽¹⁾	No	No	N/A ⁽¹⁾
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	Yes ⁽¹⁾	No	No	No ⁽¹⁾
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. Erased when RDP change from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming. Two areas can be selected, with 2-Kbyte granularity.
- Proprietary code readout protection (PCROP): a part of the flash memory can be protected against read and write from third parties. The protected area is execute-only: it can only be reached by the STM32 CPU, as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited. The PCROP area granularity is 64-bit wide. An additional option bit (PCROP_RDP) allows to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- single error detection and correction
- double error detection.
- The address of the ECC fail can be read in the ECC register

3.5 Embedded SRAM

STM32L443xx devices feature 64 Kbyte of embedded SRAM. This SRAM is split into two blocks:

- 48 Kbyte mapped at address 0x2000 0000 (SRAM1)
- 16 Kbyte located at address 0x1000 0000 with hardware parity check (SRAM2).

This memory is also mapped at address 0x2000 C000, offering a contiguous address space with the SRAM1 (16 Kbyte aliased by bit band)

This block is accessed through the ICode/DCode buses for maximum performance. These 16 Kbyte SRAM can also be retained in Standby mode.

The SRAM2 can be write-protected with 1 Kbyte granularity.

The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.6 Firewall

The device embeds a Firewall which protects code sensitive and secure data from any access performed by a code executed outside of the protected areas.

Each illegal access generates a reset which kills immediately the detected intrusion.

The Firewall main features are the following:

- Three segments can be protected and defined thanks to the Firewall registers:
 - Code segment (located in Flash or SRAM1 if defined as executable protected area)
 - Non-volatile data segment (located in Flash)
 - Volatile data segment (located in SRAM1)
- The start address and the length of each segments are configurable:
 - code segment: up to 1024 Kbyte with granularity of 256 bytes
 - Non-volatile data segment: up to 1024 Kbyte with granularity of 256 bytes
 - Volatile data segment: up to 48 Kbyte with a granularity of 64 bytes
- Specific mechanism implemented to open the Firewall to get access to the protected areas (call gate entry sequence)
- Volatile data segment can be shared or not with the non-protected code
- Volatile data segment can be executed or not depending on the Firewall configuration

The Flash readout protection must be set to level 2 in order to reach the expected level of protection.

3.7 Boot modes

At startup, BOOT0 pin or nSWBOOT0 option bit, and BOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

BOOT0 value may come from the PH3-BOOT0 pin or from an option bit depending on the value of a user option bit to free the GPIO pad if needed.

A Flash empty check mechanism is implemented to force the boot from system flash if the first flash memory location is not programmed and if the boot selection is configured to boot from main flash.

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART, I2C, SPI, CAN and USB FS in Device mode through DFU (device firmware upgrade).

3.8 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.9 Power supply management

3.9.1 Power supply schemes

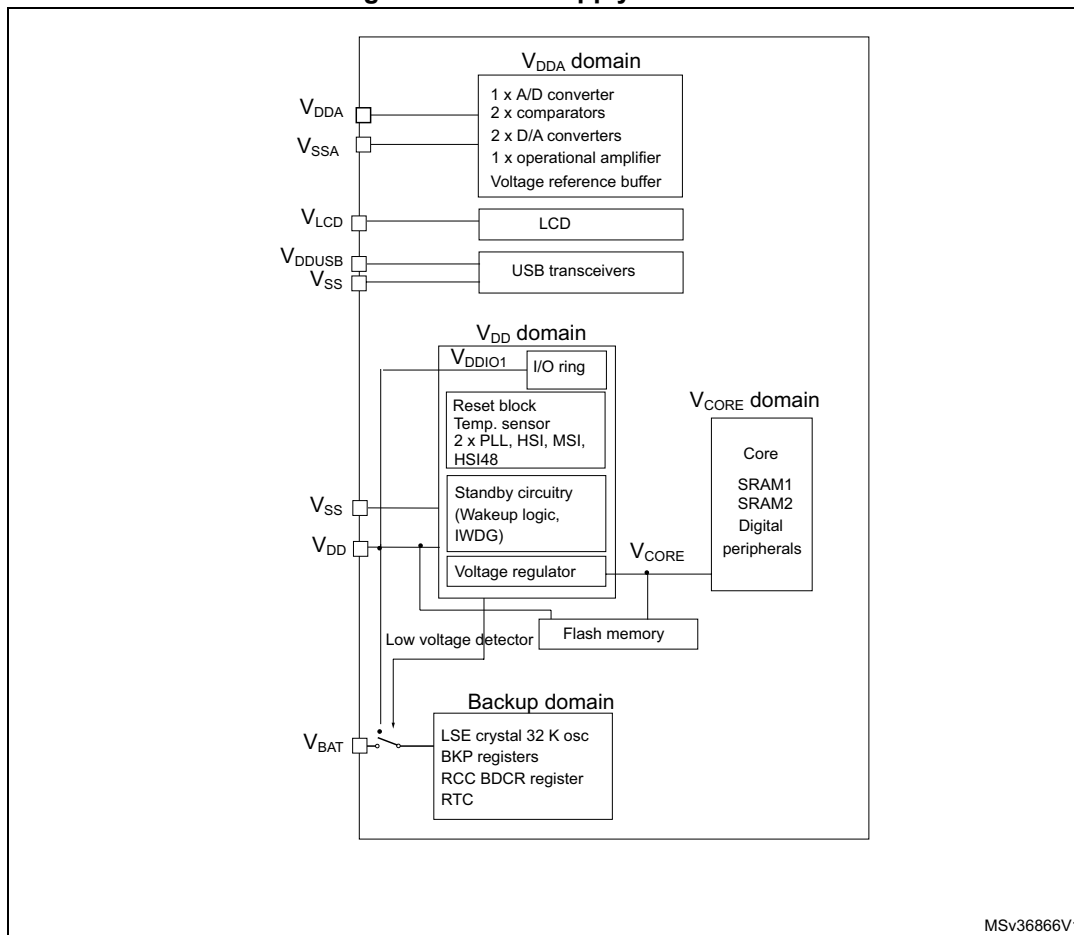
- $V_{DD} = 1.71$ to 3.6 V: external power supply for I/Os (V_{DDIO1}), the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through V_{DD} pins.
- $V_{DDA} = 1.62$ V (ADCs/COMPAs) / 1.8 (DACs/OPAMP) to 3.6 V: external analog power supply for ADCs, DACs, OPAMP, Comparators and Voltage reference buffer. The V_{DDA} voltage level is independent from the V_{DD} voltage.
- $V_{DDUSB} = 3.0$ to 3.6 V: external independent power supply for USB transceivers. The V_{DDUSB} voltage level is independent from the V_{DD} voltage.
- $V_{LCD} = 2.5$ to 3.6 V: the LCD controller can be powered either externally through VLCD pin, or internally from an internal voltage generated by the embedded step-up converter.
- $V_{BAT} = 1.55$ to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Note: When the functions supplied by V_{DDA} or V_{DDUSB} are not used, these supplies should preferably be shorted to V_{DD} .

Note: If these supplies are tied to ground, the I/Os supplied by these power supplies are not 5 V tolerant (refer to Table 17: Voltage characteristics).

Note: V_{DDIOx} is the I/Os general purpose digital functions supply. V_{DDIOx} represents V_{DDIO1} , with $V_{DDIO1} = V_{DD}$.

Figure 2. Power supply overview



3.9.2 Power supply supervisor

The device has an integrated ultra-low-power brown-out reset (BOR) active in all modes except Shutdown and ensuring proper operation after power-on and during power down. The device remains in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71V at power on, and other higher thresholds can be selected through option bytes. The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold. An interrupt can be generated when V_{DD} drops below the VPVD threshold and/or when V_{DD} is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the devices embed a Peripheral Voltage Monitor which compares the independent supply voltages V_{DDA} , V_{DDUSB} with a fixed threshold in order to ensure that the peripheral is in its functional supply range.

3.9.3 Voltage regulator

Two embedded linear voltage regulators supply most of the digital circuitries: the main regulator (MR) and the low-power regulator (LPR).

- The MR is used in the Run and Sleep modes and in the Stop 0 mode.
- The LPR is used in Low-Power Run, Low-Power Sleep, Stop 1 and Stop 2 modes. It is also used to supply the 16 Kbyte SRAM2 in Standby with RAM2 retention.
- Both regulators are in power-down in Standby and Shutdown modes: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The ultralow-power STM32L443xx supports dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the Main Regulator that supplies the logic (VCORE) can be adjusted according to the system's maximum operating frequency.

There are two power consumption ranges:

- Range 1 with the CPU running at up to 80 MHz.
- Range 2 with a maximum CPU frequency of 26 MHz. All peripheral clocks are also limited to 26 MHz.

The VCore can be supplied by the low-power regulator, the main regulator being switched off. The system is then in Low-power run mode.

- Low-power run mode with the CPU running at up to 2 MHz. Peripherals with independent clock can be clocked by HSI16.

3.9.4 Low-power modes

The ultra-low-power STM32L443xx supports seven low-power modes to achieve the best compromise between low-power consumption, short startup time, available peripherals and available wakeup sources:

By default, the microcontroller is in Run mode after a system or a power Reset. It is up to the user to select one of the low-power modes described below:

- **Sleep mode**
In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Low-power run mode**
This mode is achieved with VCore supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or from Flash, and the CPU frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16.
- **Low-power sleep mode**
This mode is entered from the low-power run mode. Only the CPU clock is stopped. When wakeup is triggered by an event or an interrupt, the system reverts to the low-power run mode.
- **Stop 0, Stop 1 and Stop 2 modes**
Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the VCore domain are stopped, the PLL, the MSI

RC, the HSI16 RC and the HSE crystal oscillators are disabled. The LSE or LSI is still running.

The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

Some peripherals with wakeup capability can enable the HSI16 RC during Stop mode to detect their wakeup condition.

Three Stop modes are available: Stop 0, Stop 1 and Stop 2 modes. In Stop 2 mode, most of the VCORE domain is put in a lower leakage mode.

Stop 1 offers the largest number of active peripherals and wakeup sources, a smaller wakeup time but a higher consumption than Stop 2. In Stop 0 mode, the main regulator remains ON, allowing a very fast wakeup time but with much higher consumption.

The system clock when exiting from Stop 0, Stop1 or Stop2 modes can be either MSI up to 48 MHz or HSI16, depending on software configuration.

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption with BOR. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are also switched off.

The RTC can remain active (Standby mode with RTC, Standby mode without RTC).

The brown-out reset (BOR) always remains active in Standby mode.

The state of each I/O during standby mode can be selected by software: I/O with internal pull-up, internal pull-down or floating.

After entering Standby mode, SRAM1 and register contents are lost except for registers in the Backup domain and Standby circuitry. Optionally, SRAM2 can be retained in Standby mode, supplied by the low-power Regulator (Standby with RAM2 retention mode).

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper) or a failure is detected on LSE (CSS on LSE).

The system clock after wakeup is MSI up to 8 MHz.

- **Shutdown mode**

The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the HSI16, the MSI, the LSI and the HSE oscillators are also switched off.

The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).

The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.

SRAM1, SRAM2 and register contents are lost except for registers in the Backup domain.

The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper).

The system clock after wakeup is MSI at 4 MHz.

Table 3. Functionalities depending on the working mode⁽¹⁾

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CPU	Y	-	Y	-	-	-	-	-	-	-	-	-	-
Flash memory (256 KB)	O ⁽²⁾	O ⁽²⁾	O ⁽²⁾	O ⁽²⁾	-	-	-	-	-	-	-	-	-
SRAM1 (48 KB)	Y	Y ⁽³⁾	Y	Y ⁽³⁾	Y	-	Y	-	-	-	-	-	-
SRAM2 (16 KB)	Y	Y ⁽³⁾	Y	Y ⁽³⁾	Y	-	Y	-	O ⁽⁴⁾	-	-	-	-
Quad SPI	O	O	O	O	-	-	-	-	-	-	-	-	-
Backup Registers	Y	Y	Y	Y	Y	-	Y	-	Y	-	Y	-	Y
Brown-out reset (BOR)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	O	O	-	-	-	-	-
Peripheral Voltage Monitor (PVMx; x=1,3,4)	O	O	O	O	O	O	O	O	-	-	-	-	-
DMA	O	O	O	O	-	-	-	-	-	-	-	-	-
High Speed Internal (HSI16)	O	O	O	O	(5)	-	(5)	-	-	-	-	-	-
Oscillator RC48	O	O	-	-	-	-	-	-	-	-	-	-	-
High Speed External (HSE)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low Speed Internal (LSI)	O	O	O	O	O	-	O	-	O	-	-	-	-
Low Speed External (LSE)	O	O	O	O	O	-	O	-	O	-	O	-	O
Multi-Speed Internal (MSI)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock Security System (CSS)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock Security System on LSE	O	O	O	O	O	O	O	O	O	O	-	-	-
RTC / Auto wakeup	O	O	O	O	O	O	O	O	O	O	O	O	O
Number of RTC Tamper pins	3	3	3	3	3	O	3	O	3	O	3	O	3
LCD	O	O	O	O	O	O	O	O	-	-	-	-	-

Table 3. Functionalities depending on the working mode⁽¹⁾ (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
USB FS	O ⁽⁸⁾	O ⁽⁸⁾	-	-	-	O	-	-	-	-	-	-	-
USARTx (x=1,2,3)	O	O	O	O	O ⁽⁶⁾	O ⁽⁶⁾	-	-	-	-	-	-	-
Low-power UART (LPUART)	O	O	O	O	O ⁽⁶⁾	O ⁽⁶⁾	O ⁽⁶⁾	O ⁽⁶⁾	-	-	-	-	-
I2Cx (x=1,2)	O	O	O	O	O ⁽⁷⁾	O ⁽⁷⁾	-	-	-	-	-	-	-
I2C3	O	O	O	O	O ⁽⁷⁾	O ⁽⁷⁾	O ⁽⁷⁾	O ⁽⁷⁾	-	-	-	-	-
SPIx (x=1,2,3)	O	O	O	O	-	-	-	-	-	-	-	-	-
CAN	O	O	O	O	-	-	-	-	-	-	-	-	-
SDMMC1	O	O	O	O	-	-	-	-	-	-	-	-	-
SWPMI1	O	O	O	O	-	O	-	-	-	-	-	-	-
SAIx (x=1)	O	O	O	O	-	-	-	-	-	-	-	-	-
ADCx (x=1)	O	O	O	O	-	-	-	-	-	-	-	-	-
DACx (x=1,2)	O	O	O	O	O	-	-	-	-	-	-	-	-
VREFBUF	O	O	O	O	O	-	-	-	-	-	-	-	-
OPAMPx (x=1)	O	O	O	O	O	-	-	-	-	-	-	-	-
COMPx (x=1,2)	O	O	O	O	O	O	O	O	-	-	-	-	-
Temperature sensor	O	O	O	O	-	-	-	-	-	-	-	-	-
Timers (TIMx)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low-power timer 1 (LPTIM1)	O	O	O	O	O	O	O	O	-	-	-	-	-
Low-power timer 2 (LPTIM2)	O	O	O	O	O	O	-	-	-	-	-	-	-
Independent watchdog (IWDG)	O	O	O	O	O	O	O	O	O	O	-	-	-
Window watchdog (WWDG)	O	O	O	O	-	-	-	-	-	-	-	-	-
SysTick timer	O	O	O	O	-	-	-	-	-	-	-	-	-
Touch sensing controller (TSC)	O	O	O	O	-	-	-	-	-	-	-	-	-
Random number generator (RNG)	O ⁽⁸⁾	O ⁽⁸⁾	-	-	-	-	-	-	-	-	-	-	-
AES hardware accelerator	O	O	O	O	-	-	-	-	-	-	-	-	-

