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Ultra-low-power Arm® Cortex®-M4 32-bit MCU+FPU, 100DMIPS, up to 512KB Flash, 160KB SRAM, analog, audio

Datasheet - production data

Features

- Ultra-low-power with FlexPowerControl
  - 1.71 V to 3.6 V power supply
  - -40 °C to 85/125 °C temperature range
  - 145 nA in V_{BAT} mode: supply for RTC and 32x32-bit backup registers
  - 22 nA Shutdown mode (5 wakeup pins)
  - 106 nA Standby mode (5 wakeup pins)
  - 375 nA Standby mode with RTC
  - 2.05 µA Stop 2 mode, 2.40 µA with RTC
  - 84 µA/MHz run mode
  - Batch acquisition mode (BAM)
  - 4 µs wakeup from Stop mode
  - Brown out reset (BOR)
  - Interconnect matrix
- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait-state execution from Flash memory, frequency up to 80 MHz, MPU, 100DMIPS and DSP instructions
- Performance benchmark
  - 1.25 DMIPS/MHz (Drystone 2.1)
  - 273.55 CoreMark® (3.42 CoreMark/MHz @ 80 MHz)
- Energy benchmark
  - 174.5 ULPBench® score
- Clock Sources
  - 4 to 48 MHz crystal oscillator
  - 32 kHz crystal oscillator for RTC (LSE)
  - Internal 16 MHz factory-trimmed RC (±1%)
  - Internal low-power 32 kHz RC (±5%)
  - Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than ±0.25 % accuracy)
  - Internal 48 MHz with clock recovery
  - 2 PLLs for system clock, audio, ADC

LQFP100 (14x14) LQFP64 (10x10) | UFBGA100 (7×7) UFBGA64 (5x5) | WLCSP64 | UFQFPN48 (7x7)

- Up to 83 fast I/Os, most 5 V-tolerant
- RTC with HW calendar, alarms and calibration
- Up to 21 capacitive sensing channels: support touchkey, linear and rotary touch sensors
- 12x timers: 1x 16-bit advanced motor-control, 1x 32-bit and 3x 16-bit general purpose, 2x 16-bit basic, 2x low-power 16-bit timers (available in Stop mode), 2x watchdogs, SysTick timer
- Memories
  - Up to 512 KB single bank Flash, proprietary code readout protection
  - 160 KB of SRAM including 32 KB with hardware parity check
  - Quad SPI memory interface
- Rich analog peripherals (independent supply)
  - 1x 12-bit ADC 5 Msps, up to 16-bit with hardware oversampling, 200 µA/Msps
  - 1x 12-bit DAC output channels, low-power sample and hold
  - 1x operational amplifier with built-in PGA
  - 2x ultra-low-power comparators
  - Accurate 2.5 V or 2.048 V reference voltage buffered output
- 16x communication interfaces
  - 1x SAI (serial audio interface)
  - 4x I2C FM+(1 Mbit/s), SMBus/PMBus
  - 3x USARTs (ISO 7816, LIN, IrDA, modem)
  - 1x UART (LIN, IrDA, modem)
  - 1x LPUART (Stop 2 wake-up)
  - 3x SPIs (and 1x Quad SPI)
  - CAN (2.0B Active) and SDMMC interface
  - IRTIM (Infrared interface)
- 14-channel DMA controller

- True random number generator
- CRC calculation unit, 96-bit unique ID
- Development support: serial wire debug (SWD), JTAG, Embedded Trace Macrocell™
- All packages are ECOPACK2® compliant

Table 1. Device summary

Reference	Part numbers
STM32L451xx	STM32L451CC, STM32L451RC, STM32L451VC, STM32L451CE, STM32L451RE, STM32L451VE

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L451xx microcontrollers.

This document should be read in conjunction with the STM32L43xxx/44xxx/45xxx/46xxx reference manual (RM0394). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the Arm®[a] Cortex®-M4 core, please refer to the Cortex®-M4 Technical Reference Manual, available from the www.arm.com website.

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Description

The STM32L451xx devices are the ultra-low-power microcontrollers based on the high-performance Arm® Cortex®-M4 32-bit RISC core operating at a frequency of up to 80 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all Arm® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32L451xx devices embed high-speed memories (Flash memory up to 512 Kbyte, 160 Kbyte of SRAM), a Quad SPI flash memories interface (available on all packages) and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The STM32L451xx devices embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, proprietary code readout protection and Firewall.

The devices offer a fast 12-bit ADC (5 Msps), two comparators, one operational amplifier, one DAC channel, an internal voltage reference buffer, a low-power RTC, one general-purpose 32-bit timer, one 16-bit PWM timer dedicated to motor control, four general-purpose 16-bit timers, and two 16-bit low-power timers.

In addition, up to 21 capacitive sensing channels are available.

They also feature standard and advanced communication interfaces.

- Four I2Cs
- Three SPIs
- Three USARTs, one UART and one Low-Power UART.
- One SAI (Serial Audio Interfaces)
- One SDMMC
- One CAN

The STM32L451xx operates in the -40 to +85 °C (+105 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported: analog independent supply input for ADC, DAC, OPAMP and comparators. A VBAT input allows to backup the RTC and backup registers.

The STM32L451xx family offers six packages from 48 to 100-pin packages.

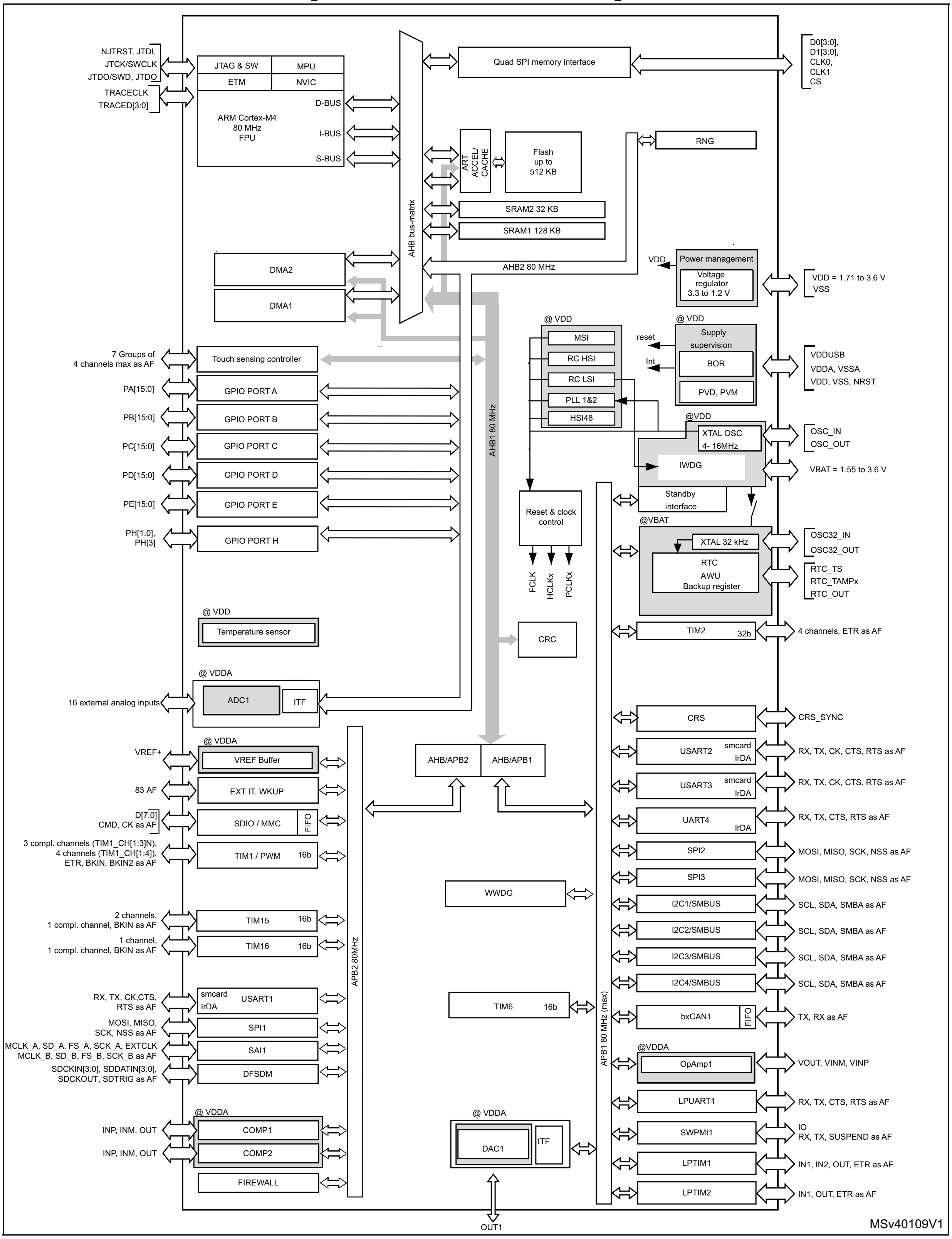
Table 2. STM32L451xx family device features and peripheral counts

Peripheral		STM32L451Vx		STM32L451Rx		STM32L451Cx	
Flash memory		256KB	512KB	256KB	512KB	256KB	512KB
SRAM		160KB					
Quad SPI		Yes					
Timers	Advanced control	1 (16-bit)					
	General purpose	2 (16-bit) 1 (32-bit)					
	Basic	2 (16-bit)					
	Low -power	2 (16-bit)					
	SysTick timer	1					
	Watchdog timers (independent, window)	2					
Comm. interfaces	SPI	3					
	I^2C	4					
	USART UART LPUART	3 1 1					
	SAI	1					
	CAN	1					
	SDMMC	Yes				No	
RTC		Yes					
Tamper pins		3		2		2	
Random generator		Yes					
GPIOs Wakeup pins		83 5		52 4		38 3	
Capacitive sensing Number of channels		21		12		6	
12-bit ADC Number of channels		1 16		1 16		1 10	
12-bit DAC channels		1					
Internal voltage reference buffer		Yes		No			
Analog comparator		2					
Operational amplifiers		1					
Max. CPU frequency		80 MHz					
Operating voltage		1.71 to 3.6 V					

Table 2. STM32L451xx family device features and peripheral counts (continued)

Peripheral	STM32L451Vx	STM32L451Rx	STM32L451Cx
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 125 °C Junction temperature: -40 to 105 °C / -40 to 130 °C		
Packages	LQFP100 UFBGA100	WLCSP64 LQFP64 UFBGA64	UFQFPN48

Figure 1. STM32L451xx block diagram



Note: AF: alternate function on I/O pins.

3 Functional overview

3.1 Arm® Cortex®-M4 core with FPU

The Arm® Cortex®-M4 with FPU processor is the latest generation of Arm® processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an Arm® core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded Arm® core, the STM32L451xx family is compatible with all Arm® tools and software.

Figure 1 shows the general block diagram of the STM32L451xx family devices.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard Arm® Cortex®-M4 processors. It balances the inherent performance advantage of the Arm® Cortex®-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor near 100 DMIPS performance at 80MHz, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 64-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 80 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded Flash memory

STM32L451xx devices feature up to 512 Kbyte of embedded Flash memory available for storing programs and data in single bank architecture. The Flash memory contains 256 pages of 2 Kbyte.

Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection: the Flash memory cannot be read from or written to if either debug features are connected, boot in RAM or bootloader is selected
  - Level 2: chip readout protection: debug features (Cortex-M4 JTAG and serial wire), boot in RAM and bootloader selection are disabled (JTAG fuse). This selection is irreversible.

Table 3. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A(1)	No	No	N/A(1)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	Yes(1)	No	No	No(1)
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. Erased when RDP change from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming. Two areas can be selected, with 2-Kbyte granularity.
- Proprietary code readout protection (PCROP): a part of the flash memory can be protected against read and write from third parties. The protected area is execute-only: it can only be reached by the STM32 CPU, as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited. The PCROP area granularity is 64-bit wide. An additional option bit (PCROP_RDP) allows to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- single error detection and correction
- double error detection.
- The address of the ECC fail can be read in the ECC register

3.5 Embedded SRAM

STM32L451xx devices feature 160 Kbyte of embedded SRAM. This SRAM is split into two blocks:

- 128 Kbyte mapped at address 0x2000 0000 (SRAM1)
- 32 Kbyte located at address 0x1000 0000 with hardware parity check (SRAM2).

  This memory is also mapped at address 0x2002 0000, offering a contiguous address space with the SRAM1 (32 Kbyte aliased by bit band)

  This block is accessed through the ICode/DCode buses for maximum performance. These 32 Kbyte SRAM can also be retained in Standby mode.

  The SRAM2 can be write-protected with 1 Kbyte granularity.

The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.6 Firewall

The device embeds a Firewall which protects code sensitive and secure data from any access performed by a code executed outside of the protected areas.

Each illegal access generates a reset which kills immediately the detected intrusion.

The Firewall main features are the following:

- Three segments can be protected and defined thanks to the Firewall registers:
  - Code segment (located in Flash or SRAM1 if defined as executable protected area)
  - Non-volatile data segment (located in Flash)
  - Volatile data segment (located in SRAM1)
- The start address and the length of each segments are configurable:
  - Code segment: up to 1024 Kbyte with granularity of 256 bytes
  - Non-volatile data segment: up to 1024 Kbyte with granularity of 256 bytes
  - Volatile data segment: up to 128 Kbyte with a granularity of 64 bytes
- Specific mechanism implemented to open the Firewall to get access to the protected areas (call gate entry sequence)
- Volatile data segment can be shared or not with the non-protected code
- Volatile data segment can be executed or not depending on the Firewall configuration

The Flash readout protection must be set to level 2 in order to reach the expected level of protection.

3.7 Boot modes

At startup, BOOT0 pin or nSWBOOT0 option bit, and BOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

BOOT0 value may come from the PH3-BOOT0 pin or from an option bit depending on the value of a user option bit to free the GPIO pad if needed.

A Flash empty check mechanism is implemented to force the boot from system flash if the first flash memory location is not programmed and if the boot selection is configured to boot from main flash.

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART, I2C, SPI or CAN.

3.8 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.9 Power supply management

3.9.1 Power supply schemes

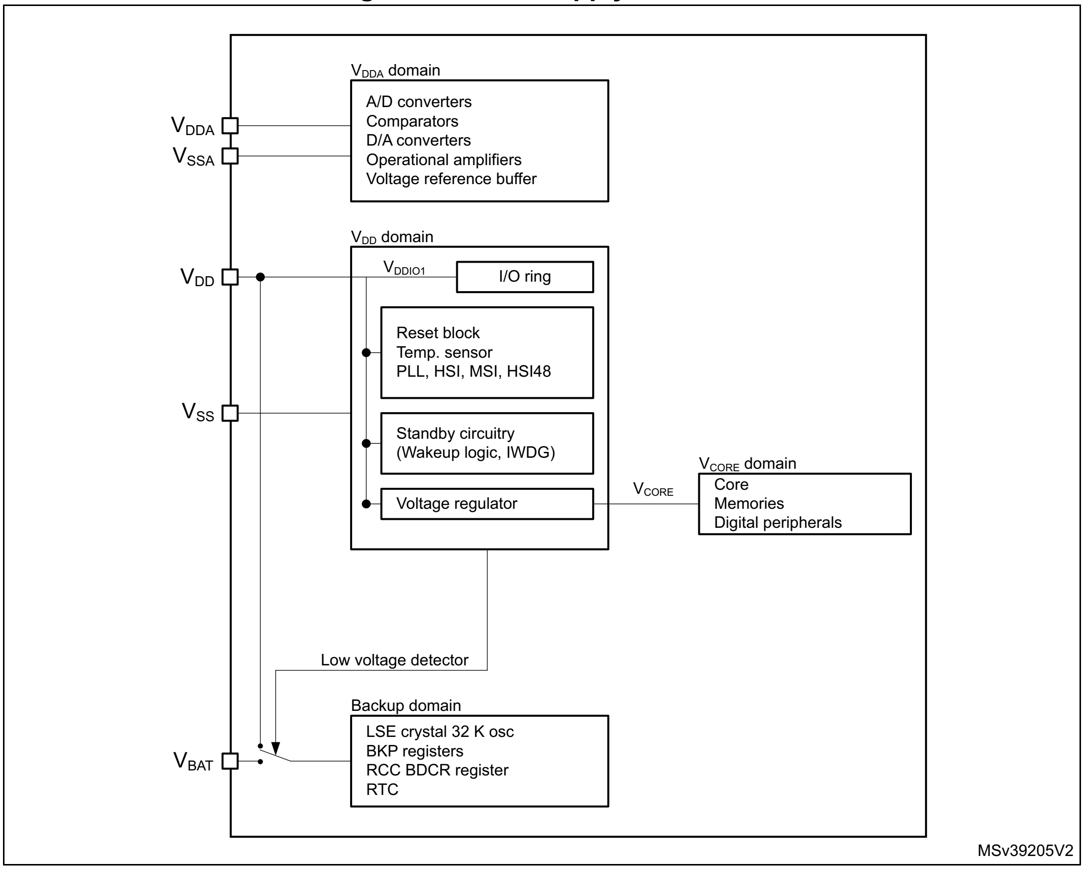
- V_{DD} = 1.71 to 3.6 V: external power supply for I/Os (V_{DDIO1}), the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through VDD pins.
- V_{DDA} = 1.62 V (ADC/COMPs) / 1.8 (DAC/OPAMP) / 2.4 V (VREFBUF) to 3.6 V: external analog power supply for ADC, DAC, OPAMP, Comparators and Voltage reference buffer. The V_{DDA} voltage level is independent from the V_{DD} voltage.
- V_{BAT} = 1.55 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Note: When the functions supplied by V_{DDA} are not used, this supply should preferably be shorted to V_{DD}.

Note: If these supplies are tied to ground, the I/Os supplied by these power supplies are not 5 V tolerant.

Note: V_{DDIOx} is the I/Os general purpose digital functions supply. V_{DDIOx} represents V_{DDIO1}, with $V_{DDIO1} = V_{DD}$.

Figure 2. Power supply overview

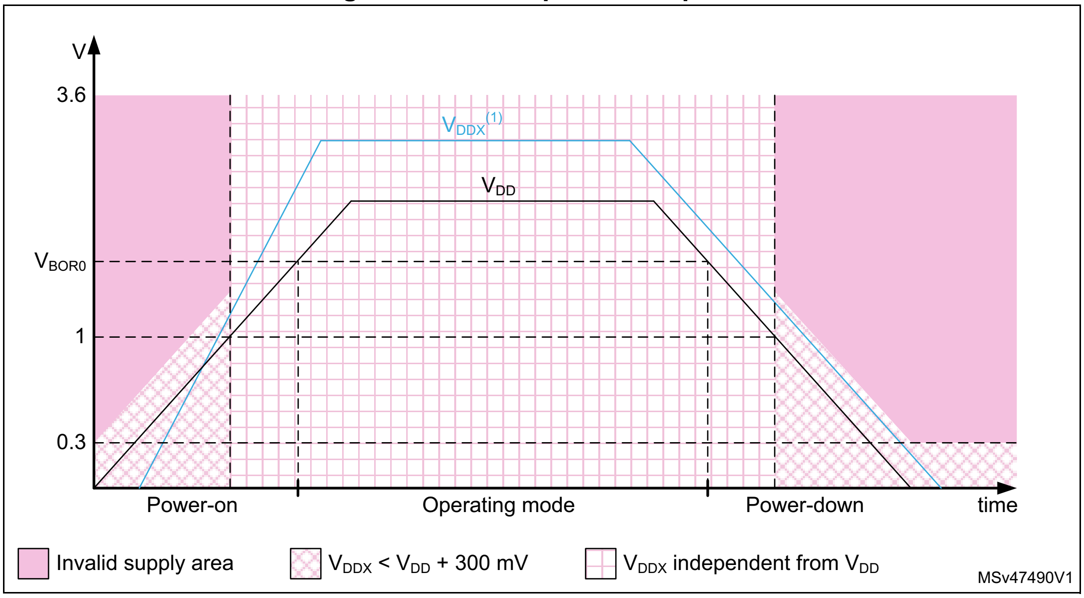


During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA}) must remain below V_{DD} + 300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.

During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ; this allows external decoupling capacitors to be discharged with different time constants during the power- down transient phase.

Figure 3. Power-up/down sequence



1. V_{DDX} refers to V_{DDA}.

3.9.2 Power supply supervisor

The device has an integrated ultra-low-power brown-out reset (BOR) active in all modes except Shutdown and ensuring proper operation after power-on and during power down. The device remains in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71V at power on, and other higher thresholds can be selected through option bytes.The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold. An interrupt can be generated when V_{DD} drops below the VPVD threshold and/or when V_{DD} is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the device embeds a Peripheral Voltage Monitor which compares the independent supply voltage V_{DDA} with a fixed threshold in order to ensure that the peripheral is in its functional supply range.

3.9.3 Voltage regulator

Two embedded linear voltage regulators supply most of the digital circuitries: the main regulator (MR) and the low-power regulator (LPR).

- The MR is used in the Run and Sleep modes and in the Stop 0 mode.
- The LPR is used in Low-Power Run, Low-Power Sleep, Stop 1 and Stop 2 modes. It is also used to supply the 32 Kbyte SRAM2 in Standby with SRAM2 retention.
- Both regulators are in power-down in Standby and Shutdown modes: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The ultralow-power STM32L451xx supports dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the Main Regulator that supplies the logic (V_{CORE}) can be adjusted according to the system's maximum operating frequency.

There are two power consumption ranges:

- Range 1 with the CPU running at up to 80 MHz.
- Range 2 with a maximum CPU frequency of 26 MHz. All peripheral clocks are also limited to 26 MHz.

The V_{CORE} can be supplied by the low-power regulator, the main regulator being switched off. The system is then in Low-power run mode.

- Low-power run mode with the CPU running at up to 2 MHz. Peripherals with independent clock can be clocked by HSI16.

3.9.4 Low-power modes

The ultra-low-power STM32L451xx supports seven low-power modes to achieve the best compromise between low-power consumption, short startup time, available peripherals and available wakeup sources.

Table 4. STM32L451xx modes overview

Mode	Regulator[1]	CPU	Flash	SRAM	Clocks	DMA & Peripherals[2]	Wakeup source	Consumption[3]	Wakeup time
Run	MR range 1	Yes	ON[4]	ON	Any	All	N/A	94 µA/MHz	N/A
	MR range2					All except RNG		85 µA/MHz	
LPRun	LPR	Yes	ON[4]	ON	Any except PLL	All except RNG	N/A	95 µA/MHz	to Range 1: 4 µs to Range 2: 64 µs
Sleep	MR range 1	No	ON[4]	ON[5]	Any	All	Any interrupt or event	27 µA/MHz	6 cycles
	MR range2					All except RNG		27 µA/MHz	
LPSleep	LPR	No	ON[4]	ON[5]	Any except PLL	All except RNG	Any interrupt or event	38 µA/MHz	6 cycles
Stop 0	MR Range 1	No	OFF	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1,2) DAC1 OPAMPx (x=1) USARTx (x=1...3)[6] UART4[6] LPUART1[6] I2Cx (x=1...4)[7] LPTIMx (x=1,2) *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) USARTx (x=1...3)[6] UART4[6] LPUART1[6] I2Cx (x=1...4)[7] LPTIMx (x=1,2)	125 µA	2.47 µs in SRAM 4.1 µs in Flash
	MR Range 2							125 µA	

Table 4. STM32L451xx modes overview (continued)

Mode	Regulator(1)	CPU	Flash	SRAM	Clocks	DMA & Peripherals(2)	Wakeup source	Consumption(3)	Wakeup time
Stop 1	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1,2) DAC1 OPAMPx (x=1) USARTx (x=1...3)(6) UART4(6) LPUART1(6) I2Cx (x=1...4)(7) LPTIMx (x=1,2) *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) USARTx (x=1...3)(6) UART4(6) LPUART1(6) I2Cx (x=1...4)(7) LPTIMx (x=1,2)	9.85 µA w/o RTC 10.5 µA w RTC	5.7 µs in SRAM 7 µs in Flash
Stop 2	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) I2C3(7) LPUART1(6) LPTIM1 *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) I2C3(7) LPUART1(6) LPTIM1	2.05 µA w/o RTC 2.30 µA w/RTC	5.8 µs in SRAM 8.3 µs in Flash