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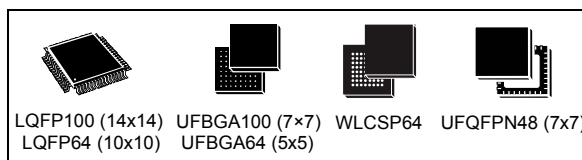


Ultra-low-power Arm[®] Cortex[®]-M4 32-bit MCU+FPU, 100DMIPS,
512KB Flash, 160KB SRAM, analog, audio, AES

Datasheet - production data

Features

- Ultra-low-power with FlexPowerControl
 - 1.71 V to 3.6 V power supply
 - -40 °C to 85/125 °C temperature range
 - 145 nA in V_{BAT} mode: supply for RTC and 32x32-bit backup registers
 - 22 nA Shutdown mode (5 wakeup pins)
 - 106 nA Standby mode (5 wakeup pins)
 - 375 nA Standby mode with RTC
 - 2.05 µA Stop 2 mode, 2.40 µA with RTC
 - 84 µA/MHz run mode
 - Batch acquisition mode (BAM)
 - 4 µs wakeup from Stop mode
 - Brown out reset (BOR)
 - Interconnect matrix
- Core: Arm[®] 32-bit Cortex[®]-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait-state execution from Flash memory, frequency up to 80 MHz, MPU, 100DMIPS and DSP instructions
- Performance benchmark
 - 1.25 DMIPS/MHz (Drystone 2.1)
 - 273.55 CoreMark[®] (3.42 CoreMark/MHz @ 80 MHz)
- Energy benchmark
 - 174.5 ULPBench[®] score
- Clock Sources
 - 4 to 48 MHz crystal oscillator
 - 32 kHz crystal oscillator for RTC (LSE)
 - Internal 16 MHz factory-trimmed RC (±1%)
 - Internal low-power 32 kHz RC (±5%)
 - Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than ±0.25 % accuracy)
 - Internal 48 MHz with clock recovery
 - 2 PLLs for system clock, audio, ADC



- Up to 83 fast I/Os, most 5 V-tolerant
- RTC with HW calendar, alarms and calibration
- Up to 21 capacitive sensing channels: support touchkey, linear and rotary touch sensors
- 12x timers: 1x 16-bit advanced motor-control, 1x 32-bit and 3x 16-bit general purpose, 2x 16-bit basic, 2x low-power 16-bit timers (available in Stop mode), 2x watchdogs, SysTick timer
- Memories
 - 512 KB single bank Flash, proprietary code readout protection
 - 160 KB of SRAM including 32 KB with hardware parity check
 - Quad SPI memory interface
- Rich analog peripherals (independent supply)
 - 1x 12-bit ADC 5 Msps, up to 16-bit with hardware oversampling, 200 µA/Msps
 - 1x 12-bit DAC output channels, low-power sample and hold
 - 1x operational amplifier with built-in PGA
 - 2x ultra-low-power comparators
 - Accurate 2.5 V or 2.048 V reference voltage buffered output
- AES: 128/256-bit key encryption hardware accelerator
- 17x communication interfaces
 - USB 2.0 full-speed crystal less solution with LPM and BCD
 - 1x SAI (serial audio interface)
 - 4x I2C FM+(1 Mbit/s), SMBus/PMBus
 - 3x USARTs (ISO 7816, LIN, IrDA, modem)
 - 1x UART (LIN, IrDA, modem)
 - 1x LPUART (Stop 2 wake-up)
 - 3x SPIs (and 1x Quad SPI)

- CAN (2.0B Active) and SDMMC interface
- IRTIM (Infrared interface)
- 14-channel DMA controller
- True random number generator
- CRC calculation unit, 96-bit unique ID
- Development support: serial wire debug (SWD), JTAG, Embedded Trace Macrocell™
- All packages are ECOPACK2® compliant

Contents

1	Introduction	12
2	Description	13
3	Functional overview	17
3.1	Arm® Cortex®-M4 core with FPU	17
3.2	Adaptive real-time memory accelerator (ART Accelerator™)	17
3.3	Memory protection unit	17
3.4	Embedded Flash memory	18
3.5	Embedded SRAM	19
3.6	Firewall	19
3.7	Boot modes	20
3.8	Cyclic redundancy check calculation unit (CRC)	20
3.9	Power supply management	20
3.9.1	Power supply schemes	20
3.9.2	Power supply supervisor	22
3.9.3	Voltage regulator	23
3.9.4	Low-power modes	23
3.9.5	Reset mode	31
3.9.6	VBAT operation	31
3.10	Interconnect matrix	32
3.11	Clocks and startup	34
3.12	General-purpose inputs/outputs (GPIOs)	37
3.13	Direct memory access controller (DMA)	37
3.14	Interrupts and events	38
3.14.1	Nested vectored interrupt controller (NVIC)	38
3.14.2	Extended interrupt/event controller (EXTI)	38
3.15	Analog to digital converter (ADC)	39
3.15.1	Temperature sensor	39
3.15.2	Internal voltage reference (VREFINT)	40
3.15.3	VBAT battery voltage monitoring	40
3.16	Digital to analog converter (DAC)	40

3.17	Voltage reference buffer (VREFBUF)	41
3.18	Comparators (COMP)	42
3.19	Operational amplifier (OPAMP)	42
3.20	Touch sensing controller (TSC)	42
3.21	Digital filter for Sigma-Delta Modulators (DFSDM)	43
3.22	Random number generator (RNG)	45
3.23	Advanced encryption standard hardware accelerator (AES)	45
3.24	Timers and watchdogs	46
3.24.1	Advanced-control timer (TIM1)	46
3.24.2	General-purpose timers (TIM2, TIM3, TIM15, TIM16)	47
3.24.3	Basic timer (TIM6)	47
3.24.4	Low-power timer (LPTIM1 and LPTIM2)	47
3.24.5	Infrared interface (IRTIM)	48
3.24.6	Independent watchdog (IWDG)	48
3.24.7	System window watchdog (WWDG)	48
3.24.8	SysTick timer	48
3.25	Real-time clock (RTC) and backup registers	49
3.26	Inter-integrated circuit interface (I ² C)	50
3.27	Universal synchronous/asynchronous receiver transmitter (USART)	51
3.28	Low-power universal asynchronous receiver transmitter (LPUART)	52
3.29	Serial peripheral interface (SPI)	53
3.30	Serial audio interfaces (SAI)	53
3.31	Controller area network (CAN)	54
3.32	Secure digital input/output and MultiMediaCards Interface (SDMMC)	54
3.33	Universal serial bus (USB)	55
3.34	Clock recovery system (CRS)	55
3.35	Quad SPI memory interface (QUADSPI)	55
3.36	Development support	57
3.36.1	Serial wire JTAG debug port (SWJ-DP)	57
3.36.2	Embedded Trace Macrocell™	57
4	Pinouts and pin description	58
5	Memory mapping	83

6	Electrical characteristics	87
6.1	Parameter conditions	87
6.1.1	Minimum and maximum values	87
6.1.2	Typical values	87
6.1.3	Typical curves	87
6.1.4	Loading capacitor	87
6.1.5	Pin input voltage	87
6.1.6	Power supply scheme	88
6.1.7	Current consumption measurement	89
6.2	Absolute maximum ratings	89
6.3	Operating conditions	92
6.3.1	General operating conditions	92
6.3.2	Operating conditions at power-up / power-down	93
6.3.3	Embedded reset and power control block characteristics	93
6.3.4	Embedded voltage reference	96
6.3.5	Supply current characteristics	98
6.3.6	Wakeup time from low-power modes and voltage scaling transition times	115
6.3.7	External clock source characteristics	118
6.3.8	Internal clock source characteristics	123
6.3.9	PLL characteristics	130
6.3.10	Flash memory characteristics	131
6.3.11	EMC characteristics	132
6.3.12	Electrical sensitivity characteristics	133
6.3.13	I/O current injection characteristics	134
6.3.14	I/O port characteristics	135
6.3.15	NRST pin characteristics	140
6.3.16	Extended interrupt and event controller input (EXTI) characteristics	141
6.3.17	Analog switches booster	141
6.3.18	Analog-to-Digital converter characteristics	142
6.3.19	Digital-to-Analog converter characteristics	155
6.3.20	Voltage reference buffer characteristics	160
6.3.21	Comparator characteristics	162
6.3.22	Operational amplifiers characteristics	163
6.3.23	Temperature sensor characteristics	166
6.3.24	V _{BAT} monitoring characteristics	167
6.3.25	Timer characteristics	167

	6.3.26	Communication interfaces characteristics	168
7		Package information	181
	7.1	LQFP100 package information	181
	7.2	UFBGA100 package information	184
	7.3	LQFP64 package information	187
	7.4	UFBGA64 package information	189
	7.5	WLCSP64 package information	192
	7.6	UFQFPN48 package information	195
	7.7	Thermal characteristics	198
		7.7.1 Reference document	198
		7.7.2 Selecting the product temperature range	198
8		Ordering information	201
9		Revision history	202

List of tables

Table 1.	STM32L462xx family device features and peripheral counts	14
Table 2.	Access status versus readout protection level and execution modes.	18
Table 3.	STM32L462xx modes overview	24
Table 4.	Functionalities depending on the working mode.	29
Table 5.	STM32L462xx peripherals interconnect matrix	32
Table 6.	DMA implementation	37
Table 7.	Temperature sensor calibration values.	40
Table 8.	Internal voltage reference calibration values	40
Table 9.	DFSDM1 implementation	45
Table 10.	Timer feature comparison.	46
Table 11.	I2C implementation.	50
Table 12.	STM32L462xx USART/UART/LPUART features	51
Table 13.	SAI implementation.	54
Table 14.	Legend/abbreviations used in the pinout table	61
Table 15.	STM32L462xx pin definitions	62
Table 16.	Alternate function AF0 to AF7.	71
Table 17.	Alternate function AF8 to AF15.	77
Table 18.	STM32L462xx memory map and peripheral register boundary addresses	84
Table 19.	Voltage characteristics	89
Table 20.	Current characteristics	90
Table 21.	Thermal characteristics.	91
Table 22.	General operating conditions	92
Table 23.	Operating conditions at power-up / power-down	93
Table 24.	Embedded reset and power control block characteristics.	93
Table 25.	Embedded internal voltage reference.	96
Table 26.	Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF)	99
Table 27.	Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART disable	100
Table 28.	Current consumption in Run and Low-power run modes, code with data processing running from SRAM1	101
Table 29.	Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF)	102
Table 30.	Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART disable	103
Table 31.	Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1	103
Table 32.	Current consumption in Sleep and Low-power sleep modes, Flash ON	104
Table 33.	Current consumption in Low-power sleep modes, Flash in power-down	105
Table 34.	Current consumption in Stop 2 mode	105
Table 35.	Current consumption in Stop 1 mode	107
Table 36.	Current consumption in Stop 0	108
Table 37.	Current consumption in Standby mode	109
Table 38.	Current consumption in Shutdown mode	110
Table 39.	Current consumption in VBAT mode	111
Table 40.	Peripheral current consumption	113
Table 41.	Low-power mode wakeup timings	115
Table 42.	Regulator modes transition times	117

Table 43.	Wakeup time using USART/LPUART	117
Table 44.	High-speed external user clock characteristics	118
Table 45.	Low-speed external user clock characteristics	119
Table 46.	HSE oscillator characteristics	120
Table 47.	LSE oscillator characteristics ($f_{LSE} = 32.768$ kHz)	121
Table 48.	HSI16 oscillator characteristics	123
Table 49.	MSI oscillator characteristics	125
Table 50.	HSI48 oscillator characteristics	128
Table 51.	LSI oscillator characteristics	129
Table 52.	PLL, PLLSAI1 characteristics	130
Table 53.	Flash memory characteristics	131
Table 54.	Flash memory endurance and data retention	131
Table 55.	EMS characteristics	132
Table 56.	EMI characteristics	133
Table 57.	ESD absolute maximum ratings	133
Table 58.	Electrical sensitivities	134
Table 59.	I/O current injection susceptibility	134
Table 60.	I/O static characteristics	135
Table 61.	Output voltage characteristics	137
Table 62.	I/O AC characteristics	138
Table 63.	NRST pin characteristics	140
Table 64.	EXTI Input Characteristics	141
Table 65.	Analog switches booster characteristics	141
Table 66.	ADC characteristics	142
Table 67.	Maximum ADC RAIN	144
Table 68.	ADC accuracy - limited test conditions 1	146
Table 69.	ADC accuracy - limited test conditions 2	148
Table 70.	ADC accuracy - limited test conditions 3	150
Table 71.	ADC accuracy - limited test conditions 4	152
Table 72.	DAC characteristics	155
Table 73.	DAC accuracy	158
Table 74.	VREFBUF characteristics	160
Table 75.	COMP characteristics	162
Table 76.	OPAMP characteristics	163
Table 77.	TS characteristics	166
Table 78.	V_{BAT} monitoring characteristics	167
Table 79.	V_{BAT} charging characteristics	167
Table 80.	TIMx characteristics	167
Table 81.	IWDG min/max timeout period at 32 kHz (LSI)	168
Table 82.	WWDG min/max timeout value at 80 MHz (PCLK)	168
Table 83.	I2C analog filter characteristics	169
Table 84.	SPI characteristics	170
Table 85.	Quad SPI characteristics in SDR mode	173
Table 86.	QUADSPI characteristics in DDR mode	174
Table 87.	SAI characteristics	176
Table 88.	SD / MMC dynamic characteristics, $V_{DD} = 2.7$ V to 3.6 V	178
Table 89.	eMMC dynamic characteristics, $V_{DD} = 1.71$ V to 1.9 V	179
Table 90.	USB electrical characteristics	180
Table 91.	LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data	181
Table 92.	UFPGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data	184

Table 93.	UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)	185
Table 94.	LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data	187
Table 95.	UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package mechanical data	190
Table 96.	UFBGA64 recommended PCB design rules (0.5 mm pitch BGA)	190
Table 97.	WLCSP64 - 64-ball, 3.357x3.657 mm 0.4 mm pitch wafer level chip scale mechanical data	193
Table 98.	WLCSP64 recommended PCB design rules (0.4 mm pitch)	194
Table 99.	UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data	196
Table 100.	Package thermal characteristics	198
Table 101.	STM32L462xx ordering information scheme	201
Table 102.	Document revision history	202

List of figures

Figure 1.	STM32L462xx block diagram	16
Figure 2.	Power supply overview	21
Figure 3.	Power-up/down sequence	22
Figure 4.	Clock tree	36
Figure 5.	Voltage reference buffer	41
Figure 6.	STM32L462Vx LQFP100 pinout ⁽¹⁾	58
Figure 7.	STM32L462Vx UFBGA100 ballout ⁽¹⁾	59
Figure 8.	STM32L462Rx LQFP64 pinout ⁽¹⁾	59
Figure 9.	STM32L462Rx UFBGA64 ballout ⁽¹⁾	60
Figure 10.	STM32L462Rx WLCSP64 pinout ⁽¹⁾	60
Figure 11.	STM32L462Cx UFQFPN48 pinout ⁽¹⁾	61
Figure 12.	STM32L462xx memory map	83
Figure 13.	Pin loading conditions	87
Figure 14.	Pin input voltage	87
Figure 15.	Power supply scheme	88
Figure 16.	Current consumption measurement scheme	89
Figure 17.	VREFINT versus temperature	97
Figure 18.	High-speed external clock source AC timing diagram	118
Figure 19.	Low-speed external clock source AC timing diagram	119
Figure 20.	Typical application with an 8 MHz crystal	121
Figure 21.	Typical application with a 32.768 kHz crystal	122
Figure 22.	HSI16 frequency versus temperature	124
Figure 23.	Typical current consumption versus MSI frequency	128
Figure 24.	HSI48 frequency versus temperature	129
Figure 25.	I/O input characteristics	136
Figure 26.	I/O AC characteristics definition ⁽¹⁾	140
Figure 27.	Recommended NRST pin protection	141
Figure 28.	ADC accuracy characteristics	153
Figure 29.	Typical connection diagram using the ADC	154
Figure 30.	12-bit buffered / non-buffered DAC	157
Figure 31.	SPI timing diagram - slave mode and CPHA = 0	171
Figure 32.	SPI timing diagram - slave mode and CPHA = 1	172
Figure 33.	SPI timing diagram - master mode	172
Figure 34.	Quad SPI timing diagram - SDR mode	175
Figure 35.	Quad SPI timing diagram - DDR mode	175
Figure 36.	SAI master timing waveforms	177
Figure 37.	SAI slave timing waveforms	178
Figure 38.	SDIO high-speed mode	179
Figure 39.	SD default mode	180
Figure 40.	LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline	181
Figure 41.	LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint	182
Figure 42.	LQFP100 marking (package top view)	183
Figure 43.	UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline	184
Figure 44.	UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint	185
Figure 45.	UFBGA100 marking (package top view)	186

Figure 46.	LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline	187
Figure 47.	LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint.	188
Figure 48.	LQFP64 marking (package top view)	189
Figure 49.	UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package outline	189
Figure 50.	UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package recommended footprint	190
Figure 51.	UFBGA64 marking (package top view)	191
Figure 52.	WLCSP64 - 64-ball, 3.357x3.657 mm 0.4 mm pitch wafer level chip scale package outline.	192
Figure 53.	WLCSP64 - 64-pin, 3.357x3.657 mm 0.4 mm pitch wafer level chip scale recommended footprint.	193
Figure 54.	WLCSP64 marking (package top view)	194
Figure 55.	UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline.	195
Figure 56.	UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint	196
Figure 57.	UFQFPN48 marking (package top view)	197
Figure 58.	LQFP64 P_D max vs. T_A	200

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L462xx microcontrollers.

This document should be read in conjunction with the STM32L43xxx/44xxx/45xxx/46xxx reference manual (RM0394). The reference manual is available from the STMicroelectronics website www.st.com.

For information on the Arm^{®(a)} Cortex[®]-M4 core, please refer to the Cortex[®]-M4 Technical Reference Manual, available from the www.arm.com website.



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2 Description

The STM32L462xx devices are the ultra-low-power microcontrollers based on the high-performance Arm[®] Cortex[®]-M4 32-bit RISC core operating at a frequency of up to 80 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all Arm[®] single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32L462xx devices embed high-speed memories (Flash memory up to 512 Kbyte, 160 Kbyte of SRAM), a Quad SPI flash memories interface (available on all packages) and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The STM32L462xx devices embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, proprietary code readout protection and Firewall.

The devices offer a fast 12-bit ADC (5 Msps), two comparators, one operational amplifier, one DAC channel, an internal voltage reference buffer, a low-power RTC, one general-purpose 32-bit timer, one 16-bit PWM timer dedicated to motor control, four general-purpose 16-bit timers, and two 16-bit low-power timers.

In addition, up to 21 capacitive sensing channels are available.

They also feature standard and advanced communication interfaces.

- Four I2Cs
- Three SPIs
- Three USARTs, one UART and one Low-Power UART.
- One SAI (Serial Audio Interfaces)
- One SDMMC
- One CAN
- One USB full-speed device crystal less

The STM32L462xx devices embed AES hardware accelerator.

The STM32L462xx operates in the -40 to +85 °C (+105 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported: analog independent supply input for ADC, DAC, OPAMP and comparators. A VBAT input allows to backup the RTC and backup registers.

The STM32L462xx family offers six packages from 48 to 100-pin packages.

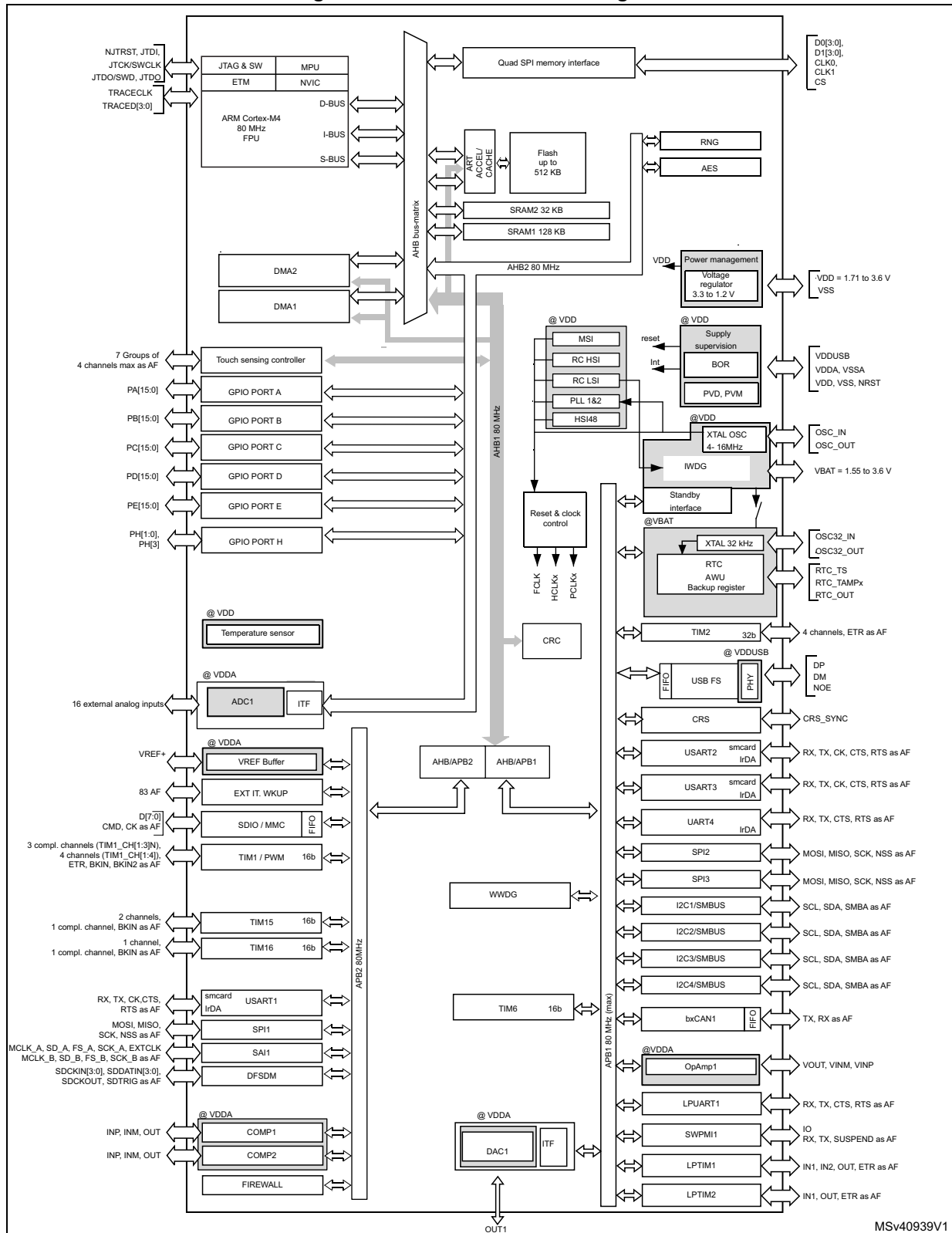
Table 1. STM32L462xx family device features and peripheral counts

Peripheral		STM32L462Vx	STM32L462Rx	STM32L462Cx
Flash memory		512KB		
SRAM		160KB		
Quad SPI		Yes		
Timers	Advanced control	1 (16-bit)		
	General purpose	2 (16-bit) 1 (32-bit)		
	Basic	2 (16-bit)		
	Low -power	2 (16-bit)		
	SysTick timer	1		
	Watchdog timers (independent, window)	2		
Comm. interfaces	SPI	3		
	I ² C	4		
	USART	3		
	UART	1		
	LPUART	1		
	SAI	1		
	CAN	1		
	USB FS	Yes		
SDMMC	Yes		No	
RTC		Yes		
Tamper pins		3	2	2
Random generator		Yes		
AES		Yes		
GPIOs		83	52	38
Wakeup pins		5	4	3
Capacitive sensing Number of channels		21	12	6
12-bit ADC Number of channels		1 16	1 16	1 10
12-bit DAC channels		1		
Internal voltage reference buffer		Yes	No	No
Analog comparator		2		
Operational amplifiers		1		

Table 1. STM32L462xx family device features and peripheral counts (continued)

Peripheral	STM32L462Vx	STM32L462Rx	STM32L462Cx
Max. CPU frequency	80 MHz		
Operating voltage	1.71 to 3.6 V		
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 125 °C Junction temperature: -40 to 105 °C / -40 to 130 °C		
Packages	LQFP100 UFBGA100	WLCSP64 LQFP64 UFBGA64	UFQFPN48

Figure 1. STM32L462xx block diagram



Note: AF: alternate function on I/O pins.



3 Functional overview

3.1 Arm[®] Cortex[®]-M4 core with FPU

The Arm[®] Cortex[®]-M4 with FPU processor is the latest generation of Arm[®] processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm[®] Cortex[®]-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an Arm[®] core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded Arm[®] core, the STM32L462xx family is compatible with all Arm[®] tools and software.

Figure 1 shows the general block diagram of the STM32L462xx family devices.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard Arm[®] Cortex[®]-M4 processors. It balances the inherent performance advantage of the Arm[®] Cortex[®]-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor near 100 DMIPS performance at 80MHz, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 64-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 80 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded Flash memory

STM32L462xx devices feature up to 512 Kbyte of embedded Flash memory available for storing programs and data in single bank architecture. The Flash memory contains 256 pages of 2 Kbyte.

Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
 - Level 0: no readout protection
 - Level 1: memory readout protection: the Flash memory cannot be read from or written to if either debug features are connected, boot in RAM or bootloader is selected
 - Level 2: chip readout protection: debug features (Cortex-M4 JTAG and serial wire), boot in RAM and bootloader selection are disabled (JTAG fuse). This selection is irreversible.

Table 2. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A ⁽¹⁾	No	No	N/A ⁽¹⁾
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	Yes ⁽¹⁾	No	No	No ⁽¹⁾
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. Erased when RDP change from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming. Two areas can be selected, with 2-Kbyte granularity.
- Proprietary code readout protection (PCROP): a part of the flash memory can be protected against read and write from third parties. The protected area is execute-only: it can only be reached by the STM32 CPU, as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited. The PCROP area granularity is 64-bit wide. An additional option bit (PCROP_RDP) allows to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- single error detection and correction
- double error detection.
- The address of the ECC fail can be read in the ECC register

3.5 Embedded SRAM

STM32L462xx devices feature 160 Kbyte of embedded SRAM. This SRAM is split into two blocks:

- 128 Kbyte mapped at address 0x2000 0000 (SRAM1)
- 32 Kbyte located at address 0x1000 0000 with hardware parity check (SRAM2).

This memory is also mapped at address 0x2002 0000, offering a contiguous address space with the SRAM1 (32 Kbyte aliased by bit band)

This block is accessed through the ICode/DCode buses for maximum performance. These 32 Kbyte SRAM can also be retained in Standby mode.

The SRAM2 can be write-protected with 1 Kbyte granularity.

The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.6 Firewall

The device embeds a Firewall which protects code sensitive and secure data from any access performed by a code executed outside of the protected areas.

Each illegal access generates a reset which kills immediately the detected intrusion.

The Firewall main features are the following:

- Three segments can be protected and defined thanks to the Firewall registers:
 - Code segment (located in Flash or SRAM1 if defined as executable protected area)
 - Non-volatile data segment (located in Flash)
 - Volatile data segment (located in SRAM1)
- The start address and the length of each segments are configurable:
 - Code segment: up to 1024 Kbyte with granularity of 256 bytes
 - Non-volatile data segment: up to 1024 Kbyte with granularity of 256 bytes
 - Volatile data segment: up to 128 Kbyte with a granularity of 64 bytes
- Specific mechanism implemented to open the Firewall to get access to the protected areas (call gate entry sequence)
- Volatile data segment can be shared or not with the non-protected code
- Volatile data segment can be executed or not depending on the Firewall configuration

The Flash readout protection must be set to level 2 in order to reach the expected level of protection.

3.7 Boot modes

At startup, BOOT0 pin or nSWBOOT0 option bit, and BOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

BOOT0 value may come from the PH3-BOOT0 pin or from an option bit depending on the value of a user option bit to free the GPIO pad if needed.

A Flash empty check mechanism is implemented to force the boot from system flash if the first flash memory location is not programmed and if the boot selection is configured to boot from main flash.

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART, I2C, SPI, CAN or USB FS in Device mode through DFU (device firmware upgrade).

3.8 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.9 Power supply management

3.9.1 Power supply schemes

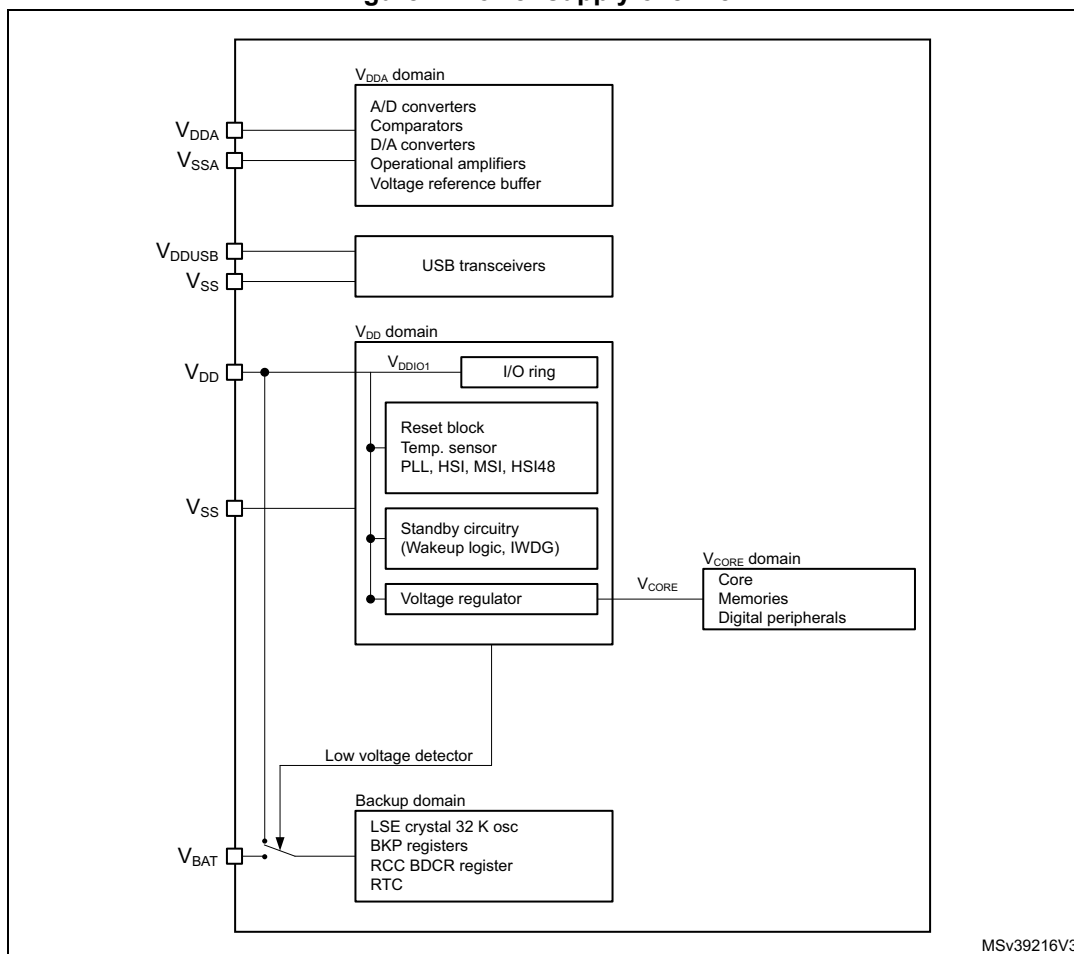
- $V_{DD} = 1.71$ to 3.6 V: external power supply for I/Os (V_{DDIO1}), the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through VDD pins.
- $V_{DDA} = 1.62$ V (ADC/COMP) / 1.8 (DAC/OPAMP) / 2.4 V (VREFBUF) to 3.6 V: external analog power supply for ADC, DAC, OPAMP, Comparators and Voltage reference buffer. The V_{DDA} voltage level is independent from the V_{DD} voltage.
- $V_{DDUSB} = 3.0$ to 3.6 V: external independent power supply for USB transceivers. The V_{DDUSB} voltage level is independent from the V_{DD} voltage.
- $V_{BAT} = 1.55$ to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Note: When the functions supplied by V_{DDA} are not used, this supply should preferably be shorted to V_{DD} .

Note: If these supplies are tied to ground, the I/Os supplied by these power supplies are not 5 V tolerant.

Note: V_{DDIOx} is the I/Os general purpose digital functions supply. V_{DDIOx} represents V_{DDIO1} , with $V_{DDIO1} = V_{DD}$.

Figure 2. Power supply overview



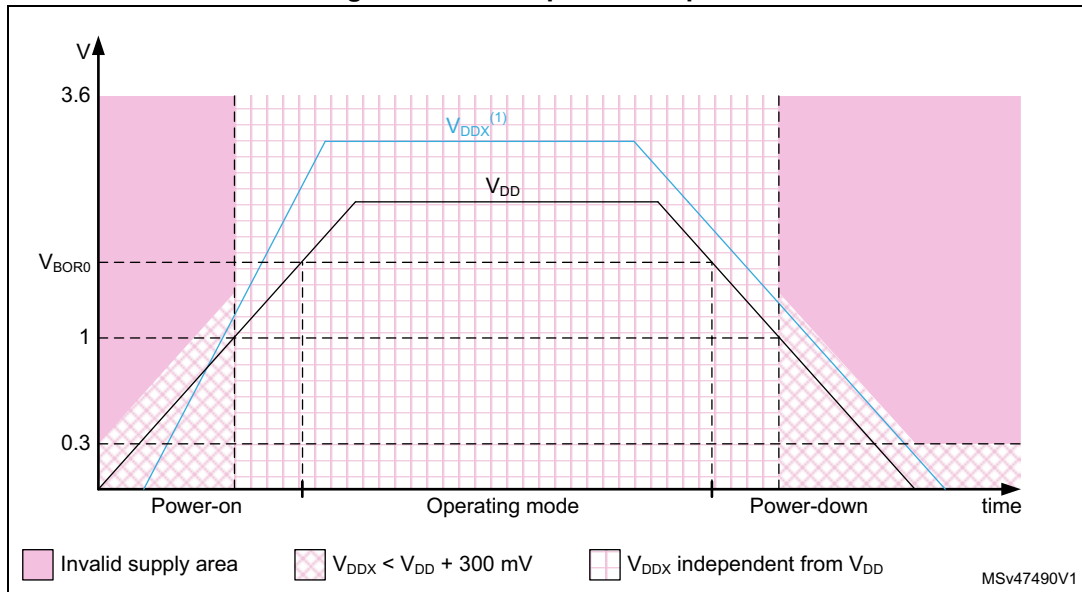
MSv39216V3

During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA}) must remain below $V_{DD} + 300$ mV.
- When V_{DD} is above 1 V, all power supplies are independent.

During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ; this allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

Figure 3. Power-up/down sequence



1. V_{DDX} refers to V_{DDA} .

3.9.2 Power supply supervisor

The device has an integrated ultra-low-power brown-out reset (BOR) active in all modes except Shutdown and ensuring proper operation after power-on and during power down. The device remains in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71V at power on, and other higher thresholds can be selected through option bytes. The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold. An interrupt can be generated when V_{DD} drops below the VPVD threshold and/or when V_{DD} is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the device embeds a Peripheral Voltage Monitor which compares the independent supply voltage V_{DDA} with a fixed threshold in order to ensure that the peripheral is in its functional supply range.

3.9.3 Voltage regulator

Two embedded linear voltage regulators supply most of the digital circuitries: the main regulator (MR) and the low-power regulator (LPR).

- The MR is used in the Run and Sleep modes and in the Stop 0 mode.
- The LPR is used in Low-Power Run, Low-Power Sleep, Stop 1 and Stop 2 modes. It is also used to supply the 32 Kbyte SRAM2 in Standby with SRAM2 retention.
- Both regulators are in power-down in Standby and Shutdown modes: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The ultralow-power STM32L462xx supports dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the Main Regulator that supplies the logic (V_{CORE}) can be adjusted according to the system's maximum operating frequency.

There are two power consumption ranges:

- Range 1 with the CPU running at up to 80 MHz.
- Range 2 with a maximum CPU frequency of 26 MHz. All peripheral clocks are also limited to 26 MHz.

The V_{CORE} can be supplied by the low-power regulator, the main regulator being switched off. The system is then in Low-power run mode.

- Low-power run mode with the CPU running at up to 2 MHz. Peripherals with independent clock can be clocked by HSI16.

3.9.4 Low-power modes

The ultra-low-power STM32L462xx supports seven low-power modes to achieve the best compromise between low-power consumption, short startup time, available peripherals and available wakeup sources.



Table 3. STM32L462xx modes overview

Mode	Regulator ⁽¹⁾	CPU	Flash	SRAM	Clocks	DMA & Peripherals ⁽²⁾	Wakeup source	Consumption ⁽³⁾	Wakeup time
Run	MR range 1	Yes	ON ⁽⁴⁾	ON	Any	All	N/A	94 µA/MHz	N/A
	MR range2					All except USB_FS, RNG		85 µA/MHz	
LPRun	LPR	Yes	ON ⁽⁴⁾	ON	Any except PLL	All except USB_FS, RNG	N/A	95 µA/MHz	to Range 1: 4 µs to Range 2: 64 µs
Sleep	MR range 1	No	ON ⁽⁴⁾	ON ⁽⁵⁾	Any	All	Any interrupt or event	27 µA/MHz	6 cycles
	MR range2					All except USB_FS, RNG		27 µA/MHz	
LPSleep	LPR	No	ON ⁽⁴⁾	ON ⁽⁵⁾	Any except PLL	All except USB_FS, RNG	Any interrupt or event	38 µA/MHz	6 cycles
Stop 0	MR Range 1	No	OFF	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1,2) DAC1 OPAMPx (x=1) USARTx (x=1...3) ⁽⁶⁾ UART4 ⁽⁶⁾ LPUART1 ⁽⁶⁾ I2Cx (x=1...4) ⁽⁷⁾ LPTIMx (x=1,2) *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) USARTx (x=1...3) ⁽⁶⁾ UART4 ⁽⁶⁾ LPUART1 ⁽⁶⁾ I2Cx (x=1...4) ⁽⁷⁾ LPTIMx (x=1,2) USB_FS ⁽⁸⁾	125 µA	2.47 µs in SRAM 4.1 µs in Flash
	MR Range 2					125 µA			



Table 3. STM32L462xx modes overview (continued)

Mode	Regulator ⁽¹⁾	CPU	Flash	SRAM	Clocks	DMA & Peripherals ⁽²⁾	Wakeup source	Consumption ⁽³⁾	Wakeup time
Stop 1	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1,2) DAC1 OPAMPx (x=1) USARTx (x=1...3) ⁽⁶⁾ UART4 ⁽⁶⁾ LPUART1 ⁽⁶⁾ I2Cx (x=1...4) ⁽⁷⁾ LPTIMx (x=1,2) *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) USARTx (x=1...3) ⁽⁶⁾ UART4 ⁽⁶⁾ LPUART1 ⁽⁶⁾ I2Cx (x=1...4) ⁽⁷⁾ LPTIMx (x=1,2) USB_FS ⁽⁸⁾	9.85 μ A w/o RTC 10.5 μ A w RTC	5.7 μ s in SRAM 7 μ s in Flash
Stop 2	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) I2C3 ⁽⁷⁾ LPUART1 ⁽⁶⁾ LPTIM1 *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) I2C3 ⁽⁷⁾ LPUART1 ⁽⁶⁾ LPTIM1	2.05 μ A w/o RTC 2.30 μ A w/RTC	5.8 μ s in SRAM 8.3 μ s in Flash