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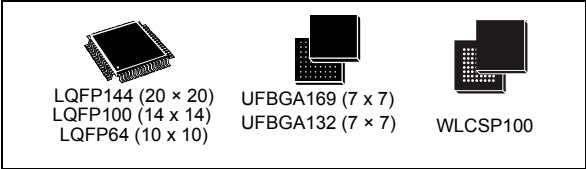
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## Ultra-low-power ARM<sup>®</sup> Cortex<sup>®</sup>-M4 32-bit MCU+FPU, 100DMIPS, up to 1MB Flash, 320KB SRAM, USB OTG FS, audio, ext. SMPS

Datasheet - preliminary data

### Features

- Ultra-low-power with FlexPowerControl
    - 1.71 V to 3.6 V power supply
    - -40 °C to 85/105/125 °C temperature range
    - 320 nA in V<sub>BAT</sub> mode: supply for RTC and 32x32-bit backup registers
    - 25 nA Shutdown mode (5 wakeup pins)
    - 108 nA Standby mode (5 wakeup pins)
    - 426 nA Standby mode with RTC
    - 2.57 µA Stop 2 mode, 2.86 µA Stop 2 with RTC
    - 91 µA/MHz run mode (LDO Mode)
    - 37 µA/MHz run mode (@3.3 V SMPS Mode)
    - Batch acquisition mode (BAM)
    - 5 µs wakeup from Stop mode
    - Brown out reset (BOR) in all modes except shutdown
    - Interconnect matrix
  - Core: ARM<sup>®</sup> 32-bit Cortex<sup>®</sup>-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait-state execution from Flash memory, frequency up to 80 MHz, MPU, 100DMIPS/1.25DMIPS/MHz (Dhrystone 2.1), and DSP instructions
  - Performance benchmark
    - 1.25 DMIPS/MHz (Dhrystone 2.1)
    - 273.55 Coremark<sup>®</sup> (3.42 Coremark/MHz @ 80 MHz)
  - Energy benchmark
    - 217 ULPBENCH™ score
  - 16 x timers: 2 x 16-bit advanced motor-control, 2 x 32-bit and 5 x 16-bit general purpose, 2 x 16-bit basic, 2 x low-power 16-bit timers (available in Stop mode), 2x watchdogs, SysTick timer
  - RTC with HW calendar, alarms and calibration
- 

LQFP144 (20 × 20)    UFBGA169 (7 × 7)    WLCSP100  
 LQFP100 (14 × 14)    UFBGA132 (7 × 7)  
 LQFP64 (10 × 10)
- Up to 136 fast I/Os, most 5 V-tolerant, up to 14 I/Os with independent supply down to 1.08 V
  - Dedicated Chrom-ART Accelerator™ for enhanced graphic content creation (DMA2D)
  - 8- to 14-bit camera interface up to 32 MHz (black&white) or 10 MHz (color)
  - Memories
    - Up to 1 MB Flash, 2 banks read-while-write, proprietary code readout protection
    - 320 KB of SRAM including 64 KB with hardware parity check
    - External memory interface for static memories supporting SRAM, PSRAM, NOR and NAND memories
    - Dual-flash Quad SPI memory interface
  - Clock Sources
    - 4 to 48 MHz crystal oscillator
    - 32 kHz crystal oscillator for RTC (LSE)
    - Internal 16 MHz factory-trimmed RC (±1%)
    - Internal low-power 32 kHz RC (±5%)
    - Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than ±0.25 % accuracy)
    - Internal 48 MHz with clock recovery
    - 3 PLLs for system clock, USB, audio, ADC
  - LCD 8 × 40 or 4 × 44 with step-up converter
  - Up to 24 capacitive sensing channels: support touchkey, linear and rotary touch sensors
  - 4x digital filters for sigma delta modulator
  - Rich analog peripherals (independent supply)
    - 3 × 12-bit ADC 5 Msps, up to 16-bit with hardware oversampling, 200 µA/Msps
    - 2 x 12-bit DAC, low-power sample and hold

- 2 x operational amplifiers with built-in PGA
- 2 x ultra-low-power comparators
- 20 x communication interfaces
  - USB OTG 2.0 full-speed, LPM and BCD
  - 2 x SAs (serial audio interface)
  - 4 x I2C FM+(1 Mbit/s), SMBus/PMBus
  - 5 x U(S)ARTs (ISO 7816, LIN, IrDA, modem)
  - 1 x LPUART
  - 3 x SPIs (4 x SPIs with the Quad SPI)
- 2x CAN (2.0B Active) and SDMMC
- SWPMI single wire protocol master I/F
- IRTIM (Infrared interface)
- 14-channel DMA controller
- True random number generator
- CRC calculation unit, 96-bit unique ID
- Development support: serial wire debug (SWD), JTAG, Embedded Trace Macrocell™

**Table 1. Device summary**

Reference	Part numbers
STM32L496xx	STM32L496AG, STM32L496QG, STM32L496RG, STM32L496VG, STM32L496ZG, STM32L496AE, STM32L496QE, STM32L496RE, STM32L496VE, STM32L496ZE

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# 1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L496xx microcontrollers.

This document should be read in conjunction with the STM32L4x6 reference manual (RM0351). The reference manual is available from the STMicroelectronics website [www.st.com](http://www.st.com).

For information on the ARM® Cortex®-M4 core, please refer to the Cortex®-M4 Technical Reference Manual, available from the [www.arm.com](http://www.arm.com) website.



## 2 Description

The STM32L496xx devices are the ultra-low-power microcontrollers based on the high-performance ARM<sup>®</sup> Cortex<sup>®</sup>-M4 32-bit RISC core operating at a frequency of up to 80 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32L496xx devices embed high-speed memories (up to 1 Mbyte of Flash memory, 320 Kbyte of SRAM), a flexible external memory controller (FSMC) for static memories (for devices with packages of 100 pins and more), a Quad SPI flash memories interface (available on all packages) and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The STM32L496xx devices embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, proprietary code readout protection and Firewall.

The devices offer up to three fast 12-bit ADCs (5 Msps), two comparators, two operational amplifiers, two DAC channels, an internal voltage reference buffer, a low-power RTC, two general-purpose 32-bit timer, two 16-bit PWM timers dedicated to motor control, seven general-purpose 16-bit timers, and two 16-bit low-power timers. The devices support four digital filters for external sigma delta modulators (DFSDM).

In addition, up to 24 capacitive sensing channels are available. The devices also embed an integrated LCD driver 8x40 or 4x44, with internal step-up converter.

They also feature standard and advanced communication interfaces.

- Four I2Cs
- Three SPIs
- Three USARTs, two UARTs and one Low-Power UART.
- Two SAIs (Serial Audio Interfaces)
- One SDMMC
- Two CAN
- One USB OTG full-speed
- One SWPMI (Single Wire Protocol Master Interface)
- Camera interface
- DMA2D controller

The STM32L496xx operates in the -40 to +85 °C (+105 °C junction), -40 to +105 °C (+125 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V VDD power supply when using internal LDO regulator and a 1.05 to 1.32V VDD12 power supply when using external SMPS supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported: analog independent supply input for ADC, DAC, OPAMPs and comparators, 3.3 V dedicated supply input for USB and up to 14 I/Os can be supplied independently down to 1.08V. A VBAT input allows to backup the RTC and backup registers. Dedicated VDD12 power supplies can be used to bypass the internal LDO regulator when connected to an external SMPS.

The STM32L496xx family offers six packages from 64-pin to 169-pin packages.

**Table 2. STM32L496xx family device features and peripheral counts**

Peripheral		STM32L496Ax		STM32L496Zx		STM32L496Qx		STM32L496Vx		STM32L496Rx	
Flash memory		512KB	1MB	512KB	1MB	512KB	1MB	512KB	1MB	512KB	1MB
SRAM		320 KB									
External memory controller for static memories		Yes		Yes		Yes		Yes <sup>(1)</sup>		No	
Quad SPI		Yes									
Timers	Advanced control	2 (16-bit)									
	General purpose	5 (16-bit) 2 (32-bit)									
	Basic	2 (16-bit)									
	Low power	2 (16-bit)									
	SysTick timer	1									
	Watchdog timers (independent, window)	2									
Comm. interfaces	SPI	3									
	I <sup>2</sup> C	4									
	USART	3									
	UART	2									
	LPUART	1									
	SAI	2									
	CAN	2									
	USB OTG FS	Yes									
SDMMC	Yes										
SWPMI	Yes										
Digital filters for sigma-delta modulators		Yes (4 filters)									
Number of channels		8									
RTC		Yes									
Tamper pins		3									
Camera interface		Yes								Yes <sup>(2)</sup>	
Chrom-ART Accelerator™		Yes									

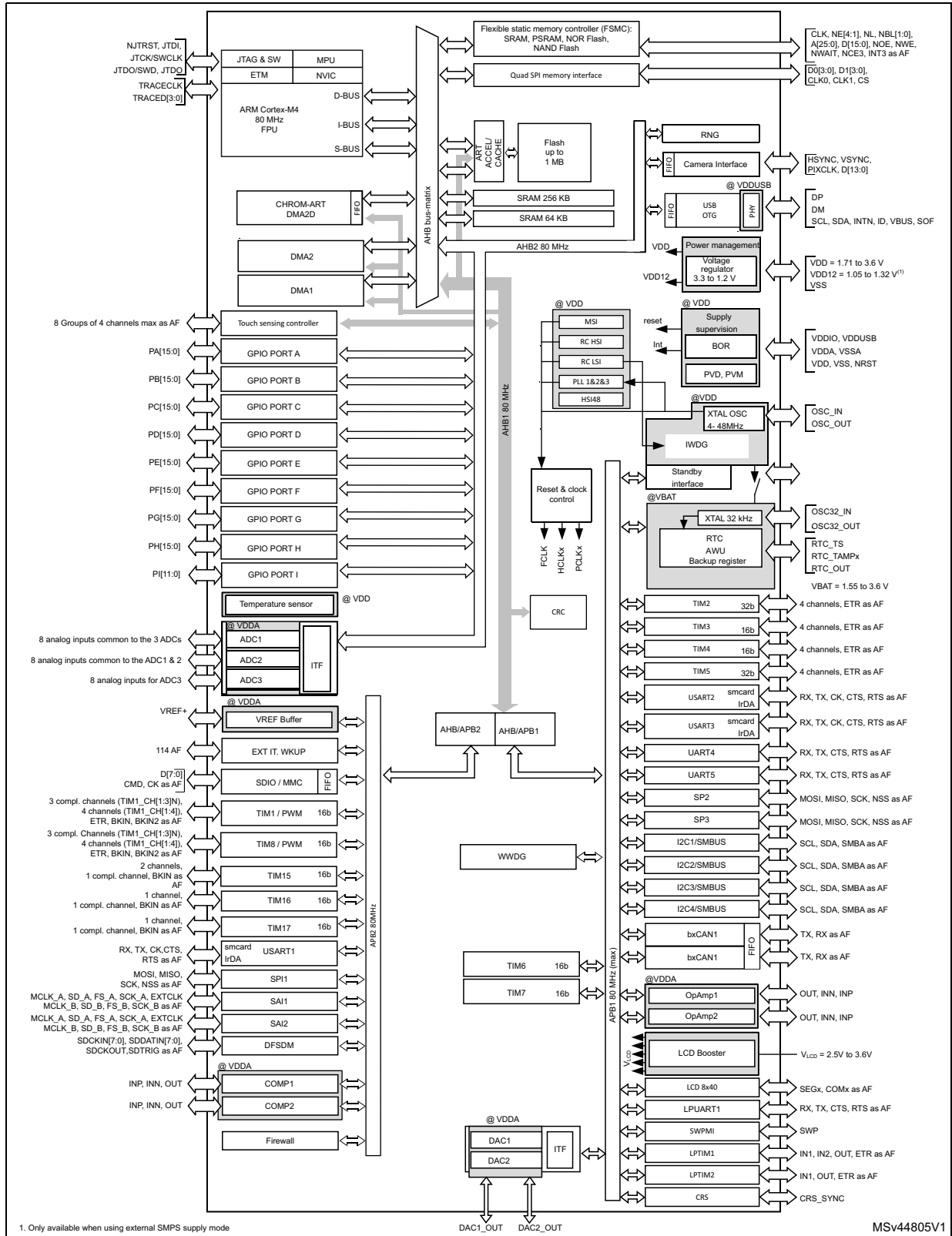


Table 2. STM32L496xx family device features and peripheral counts (continued)

Peripheral	STM32L496Ax	STM32L496Zx	STM32L496Qx	STM32L496Vx	STM32L496Rx
LCD COM x SEG	Yes 8x40 or 4x44				
Random generator	Yes				
GPIOs <sup>(3)</sup>	136	115	110	83	52
Wakeup pins	5	5	5	5	4
Nb of I/Os down to 1.08 V	14	14	14	0	0
Capacitive sensing Number of channels	24	24	24	21	21
12-bit ADCs Number of channels	3 24	3 24	3 19	3 16	3 16
12-bit DAC channels	2				
Internal voltage reference buffer	Yes				
Analog comparator	2				
Operational amplifiers	2				
Max. CPU frequency	80 MHz				
Operating voltage (VDD)	1.71 to 3.6 V				
Operating voltage (VDD12)	1.05 to 1.32 V				
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 105 °C / -40 to 125 °C Junction temperature: -40 to 105 °C / -40 to 125 °C / -40 to 130 °C				
Packages	UFBGA169	LQFP144	UFBGA132	LQFP100 WLCSP100	LQFP64

1. For the LQFP100 and WLCSP100 packages, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select.
2. Only up to 13 data bits.
3. In case external SMPS package type is used, 2 GPIO's are replaced by VDD12 pins to connect the SMPS power supplies hence reducing the number of available GPIO's by 2.

Figure 1. STM32L496xx block diagram



1. Only available when using external SMPS supply mode

MSv44805V1

Note: AF: alternate function on I/O pins.



## 3 Functional overview

### 3.1 ARM<sup>®</sup> Cortex<sup>®</sup>-M4 core with FPU

The ARM<sup>®</sup> Cortex<sup>®</sup>-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM<sup>®</sup> Cortex<sup>®</sup>-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32L496xx family is compatible with all ARM tools and software.

*Figure 1* shows the general block diagram of the STM32L496xx family devices.

### 3.2 Adaptive real-time memory accelerator (ART Accelerator<sup>™</sup>)

The ART Accelerator<sup>™</sup> is a memory accelerator which is optimized for STM32 industry-standard ARM<sup>®</sup> Cortex<sup>®</sup>-M4 processors. It balances the inherent performance advantage of the ARM<sup>®</sup> Cortex<sup>®</sup>-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor near 100 DMIPS performance at 80MHz, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 64-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 80 MHz.

### 3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

### 3.4 Embedded Flash memory

STM32L496xx devices feature up to 1 Mbyte of embedded Flash memory available for storing programs and data. The Flash memory is divided into two banks allowing read-while-write operations. This feature allows to perform a read operation from one bank while an erase or program operation is performed to the other bank. The dual bank boot is also supported. Each bank contains 256 pages of 2 Kbyte.

Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection: the Flash memory cannot be read from or written to if either debug features are connected, boot in RAM or bootloader is selected
  - Level 2: chip readout protection: debug features (Cortex-M4 JTAG and serial wire), boot in RAM and bootloader selection are disabled (JTAG fuse). This selection is irreversible.

**Table 3. Access status versus readout protection level and execution modes**

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A <sup>(1)</sup>	No	No	N/A <sup>(1)</sup>
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	Yes <sup>(1)</sup>	No	No	No <sup>(1)</sup>
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. Erased when RDP change from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming. Two areas per bank can be selected, with 2-Kbyte granularity.
- Proprietary code readout protection (PCROP): a part of the flash memory can be protected against read and write from third parties. The protected area is execute-only: it can only be reached by the STM32 CPU, as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited. One area per bank can be selected, with 64-bit granularity. An additional option bit (PCROP\_RDP) allows to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- single error detection and correction
- double error detection.
- The address of the ECC fail can be read in the ECC register

### 3.5 Embedded SRAM

STM32L496xx devices feature 320 Kbyte of embedded SRAM. This SRAM is split into two blocks:

- 256 Kbyte mapped at address 0x2000 0000 (SRAM1)
- 64 Kbyte located at address 0x1000 0000 with hardware parity check (SRAM2).

This memory is also mapped at address 0x2004 0000, offering a contiguous address space with the SRAM1.

This block is accessed through the ICode/DCode buses for maximum performance. These 64 Kbyte SRAM can also be retained in Standby mode.

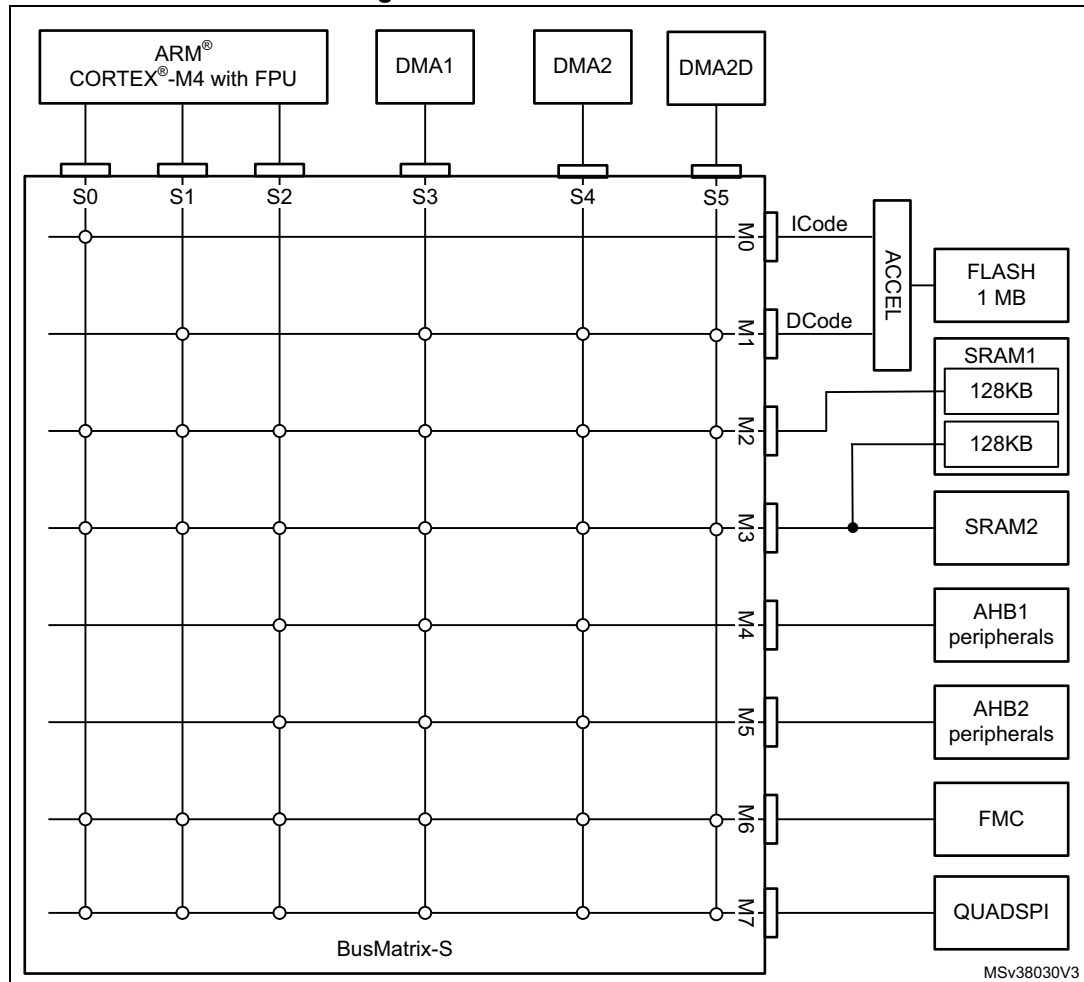
The SRAM2 can be write-protected with 1 Kbyte granularity.

The memory can be accessed in read/write at CPU clock speed with 0 wait states.

### 3.6 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs and the DMA2D) and the slaves (Flash memory, RAM, FMC, QUADSPI, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high speed peripherals work simultaneously.

Figure 2. Multi-AHB bus matrix



### 3.7 Firewall

The device embeds a Firewall which protects code sensitive and secure data from any access performed by a code executed outside of the protected areas.

Each illegal access generates a reset which kills immediately the detected intrusion.

The Firewall main features are the following:

- Three segments can be protected and defined thanks to the Firewall registers:
  - Code segment (located in Flash or SRAM1 if defined as executable protected area)
  - Non-volatile data segment (located in Flash)
  - Volatile data segment (located in SRAM1)
- The start address and the length of each segments are configurable:
  - code segment: up to 1024 Kbyte with granularity of 256 bytes
  - Non-volatile data segment: up to 1024 Kbyte with granularity of 256 bytes
  - Volatile data segment: up to 256 Kbyte of SRAM1 with a granularity of 64 bytes
- Specific mechanism implemented to open the Firewall to get access to the protected areas (call gate entry sequence)
- Volatile data segment can be shared or not with the non-protected code
- Volatile data segment can be executed or not depending on the Firewall configuration

The Flash readout protection must be set to level 2 in order to reach the expected level of protection.

### 3.8 Boot modes

At startup, BOOT0 pin and nBOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

BOOT0 value may come from the PH3-BOOT0 pin or from an option bit depending on the value of a user option bit to free the GPIO pad if needed.

A Flash empty check mechanism is implemented to force the boot from system flash if the first flash memory location is not programmed and if the boot selection is configured to boot from main flash.

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART, I2C, SPI, CAN and USB OTG FS in Device mode through DFU (device firmware upgrade).

### 3.9 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

## 3.10 Power supply management

### 3.10.1 Power supply schemes

- $V_{DD} = 1.71$  to  $3.6$  V: external power supply for I/Os ( $V_{DDIO1}$ ), the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through  $V_{DD}$  pins.
- $V_{DD12} = 1.05$  to  $1.32$  V: external power supply bypassing internal regulator when connected to an external SMPS. It is provided externally through  $V_{DD12}$  pins and only available on packages with the external SMPS supply option.  $V_{DD12}$  does not require any external decoupling capacitance and cannot support any external load.
- $V_{DDA} = 1.62$  V (ADCs/COMP) /  $1.8$  (DACs/OPAMP) to  $3.6$  V: external analog power supply for ADCs, DACs, OPAMPs, Comparators and Voltage reference buffer. The  $V_{DDA}$  voltage level is independent from the  $V_{DD}$  voltage.
- $V_{DDUSB} = 3.0$  to  $3.6$  V: external independent power supply for USB transceivers. The  $V_{DDUSB}$  voltage level is independent from the  $V_{DD}$  voltage.
- $V_{DDIO2} = 1.08$  to  $3.6$  V: external power supply for 14 I/Os (PG[15:2]). The  $V_{DDIO2}$  voltage level is independent from the  $V_{DD}$  voltage.
- $V_{LCD} = 2.5$  to  $3.6$  V: the LCD controller can be powered either externally through VLCD pin, or internally from an internal voltage generated by the embedded step-up converter.
- $V_{BAT} = 1.55$  to  $3.6$  V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when  $V_{DD}$  is not present.

*Note:* When the functions supplied by  $V_{DDA}$ ,  $V_{DDUSB}$  or  $V_{DDIO2}$  are not used, these supplies should preferably be shorted to  $V_{DD}$ .

*Note:* If these supplies are tied to ground, the I/Os supplied by these power supplies are not 5 V tolerant (refer to [Table 19: Voltage characteristics](#)).

*Note:*  $V_{DDIOx}$  is the I/Os general purpose digital functions supply.  $V_{DDIOx}$  represents  $V_{DDIO1}$  or  $V_{DDIO2}$ , with  $V_{DDIO1} = V_{DD}$ .  $V_{DDIO2}$  supply voltage level is independent from  $V_{DDIO1}$ .





### 3.10.3 Voltage regulator

Two embedded linear voltage regulators supply most of the digital circuitries: the main regulator (MR) and the low-power regulator (LPR).

- The MR is used in the Run and Sleep modes and in the Stop 0 mode.
- The LPR is used in Low-Power Run, Low-Power Sleep, Stop 1 and Stop 2 modes. It is also used to supply the 64 Kbyte SRAM2 in Standby with RAM2 retention.
- Both regulators are in power-down in Standby and Shutdown modes: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The ultralow-power STM32L496xx supports dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the Main Regulator that supplies the logic (VCORE) can be adjusted according to the system's maximum operating frequency.

There are two power consumption ranges:

- Range 1 with the CPU running at up to 80 MHz.
- Range 2 with a maximum CPU frequency of 26 MHz. All peripheral clocks are also limited to 26 MHz.

The VCORE can be supplied by the low-power regulator, the main regulator being switched off. The system is then in Low-power run mode.

- Low-power run mode with the CPU running at up to 2 MHz. Peripherals with independent clock can be clocked by HSI16.

When the MR is in use, the STM32L496xx with the external SMPS option allows to force an external VCORE supply on the VDD12 supply pins.

When VDD12 is forced by an external source and is higher than the output of the internal LDO, the current is taken from this external supply and the overall power efficiency is significantly improved if using an external step down DC/DC converter.

### 3.10.4 Low-power modes

The ultra-low-power STM32L496xx supports seven low-power modes to achieve the best compromise between low-power consumption, short startup time, available peripherals and available wakeup sources: