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STM32L4R5xx STM32L4R7xx STM32L4R9xx

Ultra-low-power Arm® Cortex®-M4 32-bit MCU+FPU, 150DMIPS, up to 2MB Flash, 640KB SRAM, LCD-TFT & MIPI DSI, ext. SMPS

Datasheet- production data

Features

- Ultra-low-power with FlexPowerControl
  - 1.71 V to 3.6 V power supply
  - -40 °C to 85/125 °C temperature range
  - Batch acquisition mode (BAM)
  - 305 nA in VBAT mode: supply for RTC and 32x32-bit backup registers
  - 33 nA Shutdown mode (5 wakeup pins)
  - 125 nA Standby mode (5 wakeup pins)
  - 420 nA Standby mode with RTC
  - 2.8 µA Stop 2 with RTC
  - 110 µA/MHz Run mode (LDO mode)
  - 43 µA/MHz Run mode (@ 3.3 V SMPS mode)
  - 5 µs wakeup from Stop mode
  - Brownout reset (BOR) in all modes except shutdown
  - Interconnect matrix
- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, adaptive real-time accelerator (ART Accelerator™) allowing 0-wait-state execution from Flash memory, frequency up to 120 MHz, MPU, 150 DMIPS/1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Performance benckmark
  - 1.25 DMIPS/MHz (Drystone 2.1)
  - 409.20 Coremark® (3.41 Coremark/MHz @120 MHz)
- Energy benckmark
  - 233 ULPMark™CP score
  - 56.5 ULPMark™PP score
- Clock sources
  - 4 to 48 MHz crystal oscillator
  - 32 kHz crystal oscillator for RTC (LSE)
  - Internal 16 MHz factory-trimmed RC (±1%)
  - Internal low-power 32 kHz RC (±5%)

LQFP144 (20 × 20)
LQFP100 (14 x 14)

UFBGA169 (7 x 7)
UFBGA144 (10 x 10)
UFBGA132 (7 × 7)

WLCSP144

  - Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than ±0.25 % accuracy)
  - Internal 48 MHz with clock recovery
  - 3 PLLs for system clock, USB, audio, ADC
- RTC with HW calendar, alarms and calibration
- Up to 24 capacitive sensing channels: support touchkey, linear and rotary touch sensors
- Advanced graphics features
  - Chrom-ART Accelerator™ (DMA2D) for enhanced graphic content creation
  - Chrom-GRC™ (GFXMMU) allowing up to 20% of graphic resources optimization
  - MIPI® DSI Host controller with two DSI lanes running at up to 500 Mbits/s each
  - LCD-TFT controller
- 16x timers: 2 x 16-bit advanced motor-control, 2 x 32-bit and 5 x 16-bit general purpose, 2x 16-bit basic, 2x low-power 16-bit timers (available in Stop mode), 2x watchdogs, SysTick timer
- Up to 136 fast I/Os, most 5 V-tolerant, up to 14 I/Os with independent supply down to 1.08 V
- Memories
  - 2-Mbyte Flash, 2 banks read-while-write, proprietary code readout protection
  - 640 Kbytes of SRAM including 64 Kbytes with hardware parity check
  - External memory interface for static memories supporting SRAM, PSRAM, NOR, NAND and FRAM memories
  - 2 x OctoSPI memory interface
- 4x digital filters for sigma delta modulator
- Rich analog peripherals (independent supply)

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  - 12-bit ADC 5 Msps, up to 16-bit with hardware oversampling, 200 µA/Msps
  - 2x 12-bit DAC, low-power sample and hold
  - 2x operational amplifiers with built-in PGA
  - 2x ultra-low-power comparators
- 20x communication interfaces
  - USB OTG 2.0 full-speed, LPM and BCD
  - 2x SAIs (serial audio interface)
  - 4x I2C FM+(1 Mbit/s), SMBus/PMBus
  - 6x USARTs (ISO 7816, LIN, IrDA, modem)
  - 3x SPIs (5x SPIs with the dual OctoSPI)
  - CAN (2.0B Active) and SDMMC
- 14-channel DMA controller
- True random number generator
- CRC calculation unit, 96-bit unique ID
- 8- to 14-bit camera interface up to 32 MHz (black and white) or 10 MHz (color)
- Development support: serial wire debug (SWD), JTAG, Embedded Trace Macrocell (ETM)

Table 1. Device summary

Reference	Part numbers
STM32L4R5xx	STM32L4R5VI, STM32L4R5QI, STM32L4R5ZI, STM32L4R5AI, STM32L4R5AG, STM32L4R5QG, STM32L4R5VG, STM32L4R5ZG
STM32L4R7xx	STM32L4R7VI, STM32L4R7ZI, STM32L4R7AI
STM32L4R9xx	STM32L4R9VI, STM32L4R9ZI, STM32L4R9AI, STM32L4R9AG, STM32L4R9VG, STM32L4R9ZG

Contents

1 Introduction . . . 13

2 Description . . . 14

3 Functional overview . . . 18

3.1 Arm® Cortex®-M4 core with FPU . . . 18

3.2 Adaptive real-time memory accelerator (ART Accelerator™) . . . 18

3.3 Memory protection unit . . . 18

3.4 Embedded Flash memory . . . 19

3.5 Embedded SRAM . . . 20

3.6 Multi-AHB bus matrix . . . 21

3.7 Firewall . . . 21

3.8 Boot modes . . . 22

3.9 Cyclic redundancy check calculation unit (CRC) . . . 22

3.10 Power supply management . . . 23

3.10.1 Power supply schemes . . . 23

3.10.2 Power supply supervisor . . . 27

3.10.3 Voltage regulator . . . 27

3.10.4 Low-power modes . . . 29

3.10.5 Reset mode . . . 36

3.10.6 VBAT operation . . . 37

3.11 Interconnect matrix . . . 37

3.12 Clocks and startup . . . 39

3.13 General-purpose inputs/outputs (GPIOs) . . . 42

3.14 Direct memory access controller (DMA) . . . 42

3.15 DMA request router (DMAMux) . . . 43

3.16 Chrom-ART Accelerator™ (DMA2D) . . . 43

3.17 Chrom-GRC™ (GFXMMU) . . . 43

3.18 Interrupts and events . . . 44

3.18.1 Nested vectored interrupt controller (NVIC) . . . 44

3.18.2 Extended interrupt/event controller (EXTI) . . . 44

3.19 Analog-to-digital converter (ADC) . . . 45

3.19.1 Temperature sensor . . . 45
3.19.2 Internal voltage reference (VREFINT) . . . 46
3.19.3 VBAT battery voltage monitoring . . . 46
3.20 Digital to analog converter (DAC) . . . 46
3.21 Voltage reference buffer (VREFBUF) . . . 47
3.22 Comparators (COMP) . . . 47
3.23 Operational amplifier (OPAMP) . . . 48
3.24 Touch sensing controller (TSC) . . . 48
3.25 LCD-TFT controller (LTDC) . . . 49
3.26 DSI Host (DSIHOST) . . . 49
3.27 Digital filter for sigma-delta modulators (DFSDM) . . . 51
3.28 Random number generator (RNG) . . . 52
3.29 Digital camera interface (DCMI) . . . 52
3.30 Timers and watchdogs . . . 52
3.30.1 Advanced-control timer (TIM1, TIM8) . . . 53
3.30.2 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM15, TIM16, TIM17) . . . 54
3.30.3 Basic timers (TIM6 and TIM7) . . . 54
3.30.4 Low-power timer (LPTIM1 and LPTIM2) . . . 54
3.30.5 Independent watchdog (IWDG) . . . 55
3.30.6 System window watchdog (WWDG) . . . 55
3.30.7 SysTick timer . . . 55
3.31 Real-time clock (RTC) and backup registers . . . 56
3.32 Inter-integrated circuit interface (I^2C) . . . 56
3.33 Universal synchronous/asynchronous receiver transmitter (USART) . . . 58
3.34 Low-power universal asynchronous receiver transmitter (LPUART) . . . 59
3.35 Serial peripheral interface (SPI) . . . 59
3.36 Serial audio interfaces (SAI) . . . 59
3.37 Controller area network (CAN) . . . 60
3.38 Secure digital input/output and MultiMediaCards Interface (SDMMC) . . . 61
3.39 Universal serial bus on-the-go full-speed (OTG_FS) . . . 62
3.40 Clock recovery system (CRS) . . . 62
3.41 Flexible static memory controller (FSMC) . . . 62
3.42 OctoSPI interface (OctoSPI) . . . 63

3.43 OctoSPI IO manager (OctoSPIIOM) 64
3.44 Development support 64
3.44.1 Serial wire JTAG debug port (SWJ-DP) 64
3.44.2 Embedded Trace Macrocell™ 65

4 Pinouts and pin description 66

5 Memory mapping 135

6 Electrical characteristics 140
6.1 Parameter conditions 140
6.1.1 Minimum and maximum values 140
6.1.2 Typical values 140
6.1.3 Typical curves 140
6.1.4 Loading capacitor 140
6.1.5 Pin input voltage 140
6.1.6 Power supply scheme 141
6.1.7 Current consumption measurement 142
6.2 Absolute maximum ratings 142
6.3 Operating conditions 144
6.3.1 General operating conditions 144
6.3.2 Operating conditions at power-up / power-down 146
6.3.3 Embedded reset and power control block characteristics 146
6.3.4 Embedded voltage reference 148
6.3.5 Supply current characteristics 150
6.3.6 Wakeup time from low-power modes and voltage scaling transition times 186
6.3.7 External clock source characteristics 189
6.3.8 Internal clock source characteristics 194
6.3.9 PLL characteristics 201
6.3.10 MIPI D-PHY characteristics 201
6.3.11 MIPI D-PHY PLL characteristics 204
6.3.12 MIPI D-PHY regulator characteristics 205
6.3.13 Flash memory characteristics 206
6.3.14 EMC characteristics 207
6.3.15 Electrical sensitivity characteristics 208
6.3.16 I/O current injection characteristics 209

6.3.17 I/O port characteristics 210
6.3.18 NRST pin characteristics 216
6.3.19 Extended interrupt and event controller input (EXTI) characteristics . . 217
6.3.20 Analog switches booster 217
6.3.21 Analog-to-digital converter characteristics 218
6.3.22 Digital-to-Analog converter characteristics 231
6.3.23 Voltage reference buffer characteristics 236
6.3.24 Comparator characteristics 238
6.3.25 Operational amplifiers characteristics 239
6.3.26 Temperature sensor characteristics 243
6.3.27 V_{BAT} monitoring characteristics 243
6.3.28 DFSDM characteristics 244
6.3.29 Timer characteristics 245
6.3.30 Communication interfaces characteristics 247
6.3.31 FSMC characteristics 256
6.3.32 OctoSPI characteristics 272
6.3.33 Camera interface (DCMI) timing specifications 280
6.3.34 LCD-TFT controller (LTDC) characteristics 281
6.3.35 SD/SDIO/MMC card host interfaces (SDMMC) 282

7 Package information 285
7.1 UFBGA169 package information 285
7.2 UFBGA144 package information 288
7.3 LQFP144 package information 291
7.4 WLCSP144 package information 295
7.5 UFBGA132 package information 298
7.6 LQFP100 package information 301
7.7 Thermal characteristics 304
7.7.1 Reference document 304
7.7.2 Selecting the product temperature range 304

8 Ordering information 307

9 Revision history 308

List of tables

Table 1. Device summary . . . 2
Table 2. STM32L4R5xx, STM32L4R7xx and STM32L4R9xx features and peripheral counts . . . 15
Table 3. Access status versus readout protection level and execution modes . . . 19
Table 4. STM32L4R5xx modes overview . . . 29
Table 5. Functionalities depending on the working mode . . . 34
Table 6. STM32L4R5xx, STM32L4R7xx and STM32L4R9xx peripherals interconnect matrix . . . 37
Table 7. DMA implementation . . . 42
Table 8. Temperature sensor calibration values . . . 46
Table 9. Internal voltage reference calibration values . . . 46
Table 10. Timer feature comparison . . . 53
Table 11. I2C implementation . . . 57
Table 12. USART/UART/LPUART features . . . 58
Table 13. SAI implementation . . . 60
Table 14. Legend/abbreviations used in the pinout table . . . 76
Table 15. STM32L4Rxxx pin definitions . . . 77
Table 16. Alternate function AF0 to AF7 . . . 117
Table 17. Alternate function AF8 to AF15 . . . 126
Table 18. STM32L4R5xx, STM32L4R7xx and STM32L4R9xx memory map and peripheral register boundary addresses . . . 136
Table 19. Voltage characteristics . . . 143
Table 20. Current characteristics . . . 143
Table 21. Thermal characteristics . . . 144
Table 22. General operating conditions . . . 144
Table 23. Operating conditions at power-up / power-down . . . 146
Table 24. Embedded reset and power control block characteristics . . . 146
Table 25. Embedded internal voltage reference . . . 148
Table 26. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single Bank, ART enable (Cache ON Prefetch OFF) . 151
Table 27. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single Bank, ART enable (Cache ON Prefetch OFF) and power supplied by external SMPS . . . 152
Table 28. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART enable (Cache ON Prefetch OFF) . . . 153
Table 29. Consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART enable (Cache ON Prefetch OFF) and power supplied by external SMPS . . . 154
Table 30. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single bank, ART disable . . . 155
Table 31. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single bank, ART disable and power supplied by external SMPS . 156
Table 32. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART disable . . . 157
Table 33. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART disable and power supplied by external SMPS . . 158
Table 34. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1 . . . 159

Table 35. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1 and power supplied by external SMPS . . . 160
Table 36. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF) . . . 161
Table 37. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF) and power supplied by external SMPS . . . 163
Table 38. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART disable . . . 165
Table 39. Typical current consumption in Run and Low-power run modes with different codes running from Flash, ART disable and power supplied by external SMPS . . . 166
Table 40. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1 . . . 167
Table 41. Typical consumption in Run and Low-power run modes, with different codes running from SRAM1 and power supplied by external SMPS . . . 168
Table 42. Current consumption in Sleep and Low-power sleep mode, Flash ON . . . 169
Table 43. Current consumption in Sleep and Low-power sleep modes, Flash ON and power supplied by external SMPS . . . 170
Table 44. Current consumption in Low-power sleep mode, Flash in power-down . . . 171
Table 45. Current consumption in Stop 2 mode, SRAM3 disabled . . . 172
Table 46. Current consumption in Stop 2 mode, SRAM3 enabled . . . 173
Table 47. Current consumption in Stop 1 mode . . . 174
Table 48. Current consumption in Stop 0 mode . . . 175
Table 49. Current consumption in Standby mode . . . 175
Table 50. Current consumption in Shutdown mode . . . 177
Table 51. Current consumption in VBAT mode . . . 179
Table 52. Peripheral current consumption . . . 181
Table 53. Low-power mode wakeup timings . . . 186
Table 54. Regulator modes transition times . . . 188
Table 55. Wakeup time using USART/LPUART . . . 188
Table 56. High-speed external user clock characteristics . . . 189
Table 57. Low-speed external user clock characteristics . . . 190
Table 58. HSE oscillator characteristics . . . 191
Table 59. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) . . . 193
Table 60. HSI16 oscillator characteristics . . . 194
Table 61. MSI oscillator characteristics . . . 196
Table 62. HSI48 oscillator characteristics . . . 199
Table 63. LSI oscillator characteristics . . . 200
Table 64. PLL, PLLSAI1, PLLSAI2 characteristics . . . 201
Table 65. MIPI D-PHY characteristics . . . 202
Table 66. MIPI D-PHY AC characteristics LP mode and HS/LP transitions . . . 203
Table 67. DSI-PLL characteristics . . . 204
Table 68. DSI regulator characteristics . . . 205
Table 69. Flash memory characteristics . . . 206
Table 70. Flash memory endurance and data retention . . . 206
Table 71. EMS characteristics . . . 207
Table 72. EMI characteristics . . . 208
Table 73. ESD absolute maximum ratings . . . 208
Table 74. Electrical sensitivities . . . 209
Table 75. I/O current injection susceptibility . . . 210
Table 76. I/O static characteristics . . . 210
Table 77. Output voltage characteristics . . . 213

Table 78. I/O AC characteristics . . . 214
Table 79. NRST pin characteristics . . . 216
Table 80. EXTI input characteristics . . . 217
Table 81. Analog switches booster characteristics . . . 217
Table 82. ADC characteristics . . . 218
Table 83. Maximum ADC RAIN . . . 220
Table 84. ADC accuracy - limited test conditions 1 . . . 222
Table 85. ADC accuracy - limited test conditions 2 . . . 224
Table 86. ADC accuracy - limited test conditions 3 . . . 226
Table 87. ADC accuracy - limited test conditions 4 . . . 228
Table 88. DAC characteristics . . . 231
Table 89. DAC accuracy . . . 234
Table 90. VREFBUF characteristics . . . 236
Table 91. COMP characteristics . . . 238
Table 92. OPAMP characteristics . . . 239
Table 93. TS characteristics . . . 243
Table 94. V_{BAT} monitoring characteristics . . . 243
Table 95. V_{BAT} charging characteristics . . . 243
Table 96. DFSDM characteristics . . . 244
Table 97. TIMx characteristics . . . 246
Table 98. IWDG min/max timeout period at 32 kHz (LSI) . . . 246
Table 99. WWDG min/max timeout value at 120 MHz (PCLK) . . . 246
Table 100. I2C analog filter characteristics . . . 247
Table 101. SPI characteristics . . . 248
Table 102. SAI characteristics . . . 252
Table 103. USB electrical characteristics . . . 254
Table 104. USB OTG electrical characteristics . . . 255
Table 105. USB BCD DC electrical characteristics . . . 255
Table 106. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings . . . 258
Table 107. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings . . . 258
Table 108. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings . . . 259
Table 109. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings . . . 260
Table 110. Asynchronous multiplexed PSRAM/NOR read timings . . . 261
Table 111. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings . . . 261
Table 112. Asynchronous multiplexed PSRAM/NOR write timings . . . 262
Table 113. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings . . . 263
Table 114. Synchronous multiplexed NOR/PSRAM read timings . . . 265
Table 115. Synchronous multiplexed PSRAM write timings . . . 267
Table 116. Synchronous non-multiplexed NOR/PSRAM read timings . . . 268
Table 117. Synchronous non-multiplexed PSRAM write timings . . . 270
Table 118. Switching characteristics for NAND Flash read cycles . . . 272
Table 119. Switching characteristics for NAND Flash write cycles . . . 272
Table 120. OctoSPI characteristics in SDR mode . . . 273
Table 121. OctoSPI characteristics in DTR mode (no DQS) . . . 274
Table 122. OctoSPI characteristics in DTR mode (with DQS)/Octal and Hyperbus . . . 275
Table 123. DCMI characteristics . . . 280
Table 124. LTDC characteristics . . . 282
Table 125. Dynamics characteristics:
SD / eMMC characteristics at VDD = 2.7 V to 3.6 V . . . 282
Table 126. Dynamics characteristics:
eMMC characteristics at VDD = 1.71 V to 1.9 V . . . 283
Table 127. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid

array package mechanical data . . . 285
Table 128. UFBGA169 recommended PCB design rules (0.5 mm pitch BGA) . . . 286
Table 129. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package mechanical data . . . 288
Table 130. UFBGA144 recommended PCB design rules (0.80 mm pitch BGA) . . . 289
Table 131. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data . . . 292
Table 132. WLCSP - 144 bump, 5.24x 5.24 mm, 0.40 mm pitch, wafer level chip scale, mechanical data . . . 296
Table 133. WLCSP - 144 bump, 5.24x 5.24 mm, 0.40 mm pitch, wafer level chip scale, recommended PCB design rules . . . 297
Table 134. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package mechanical data . . . 298
Table 135. UFBGA132 recommended PCB design rules (0.5 mm pitch BGA) . . . 299
Table 136. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data . . . 301
Table 137. Package thermal characteristics . . . 304
Table 138. STM32L4Rxxx ordering information scheme . . . 307
Table 139. Document revision history . . . 308

List of figures

Figure 1. STM32L4R5xx, STM32L4R7xx and STM32L4R9xx block diagram . . . 17
Figure 2. Multi-AHB bus matrix . . . 21
Figure 3. STM32L4R5xx and STM32L4R7xx power supply overview . . . 24
Figure 4. STM32L4R5xxxP and STM32L4R7xxxP with external SMPS power supply overview . . . 25
Figure 5. STM32L4R9xx power supply overview . . . 26
Figure 6. Power-up/down sequence . . . 27
Figure 7. Clock tree . . . 41
Figure 8. Voltage reference buffer . . . 47
Figure 9. STM32L4R5xx and STM32L4R7xx UFBGA169 ballout(1) . . . 66
Figure 10. STM32L4R9xx UFBGA169 ballout(1) . . . 66
Figure 11. STM32L4R5xxxP UFBGA169 external SMPS ballout(1) . . . 67
Figure 12. STM32L4R5xx and STM32L4R7xx LQFP144 pinout(1) . . . 68
Figure 13. STM32L4R9xx LQFP144 pinout(1) . . . 69
Figure 14. STM32L4R5ZxxxP external SMPS LQFP144 pinout(1) . . . 70
Figure 15. STM32L4R9xx UFBGA144 ballout(1) . . . 71
Figure 16. STM32L4R9xx WLCSP144 ballout(1) . . . 71
Figure 17. STM32L4R9ZxxxP WLCSP144 external SMPS ballout(1) . . . 72
Figure 18. STM32L4R5xx WLCSP144 ballout(1) . . . 72
Figure 19. STM32L4R5xx UFBGA132 ballout(1) . . . 73
Figure 20. STM32L4R5xxxP UFBGA132 external SMPS ballout(1) . . . 73
Figure 21. STM32L4R5xx and STM32L4R7xx LQFP100 pinout(1) . . . 74
Figure 22. STM32L4R9xx LQFP100 pinout(1) . . . 75
Figure 23. STM32L4R5xx, STM32L4R7xx and STM32L4R9xx memory map . . . 135
Figure 24. Pin loading conditions . . . 140
Figure 25. Pin input voltage . . . 140
Figure 26. Power supply scheme . . . 141
Figure 27. Current consumption measurement . . . 142
Figure 28. VREFINT versus temperature . . . 149
Figure 29. High-speed external clock source AC timing diagram . . . 189
Figure 30. Low-speed external clock source AC timing diagram . . . 190
Figure 31. Typical application with an 8 MHz crystal . . . 192
Figure 32. Typical application with a 32.768 kHz crystal . . . 193
Figure 33. HSI16 frequency versus temperature . . . 195
Figure 34. Typical current consumption versus MSI frequency . . . 198
Figure 35. HSI48 frequency versus temperature . . . 200
Figure 36. MIPI D-PHY HS/LP clock lane transition timing diagram . . . 204
Figure 37. MIPI D-PHY HS/LP data lane transition timing diagram . . . 204
Figure 38. I/O input characteristics . . . 212
Figure 39. I/O AC characteristics definition(1) . . . 216
Figure 40. Recommended NRST pin protection . . . 217
Figure 41. ADC accuracy characteristics . . . 230
Figure 42. Typical connection diagram using the ADC . . . 230
Figure 43. 12-bit buffered / non-buffered DAC . . . 233
Figure 44. SPI timing diagram - slave mode and CPHA = 0 . . . 249
Figure 45. SPI timing diagram - slave mode and CPHA = 1 . . . 250
Figure 46. SPI timing diagram - master mode . . . 250
Figure 47. SAI master timing waveforms . . . 253
Figure 48. SAI slave timing waveforms . . . 253

Figure 49. USB OTG timings – definition of data signal rise and fall time . . . 255
Figure 50. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms . . . 257
Figure 51. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms . . . 259
Figure 52. Asynchronous multiplexed PSRAM/NOR read waveforms. . . . 260
Figure 53. Asynchronous multiplexed PSRAM/NOR write waveforms . . . 262
Figure 54. Synchronous multiplexed NOR/PSRAM read timings . . . 264
Figure 55. Synchronous multiplexed PSRAM write timings . . . 266
Figure 56. Synchronous non-multiplexed NOR/PSRAM read timings . . . 268
Figure 57. Synchronous non-multiplexed PSRAM write timings . . . 269
Figure 58. NAND controller waveforms for read access . . . 271
Figure 59. NAND controller waveforms for write access . . . 271
Figure 60. NAND controller waveforms for common memory read access . . . 271
Figure 61. NAND controller waveforms for common memory write access . . . 272
Figure 62. OctoSPI timing diagram - SDR mode . . . 277
Figure 63. OctoSPI timing diagram - DDR mode . . . 277
Figure 64. OctoSPI Hyperbus clock . . . 277
Figure 65. OctoSPI Hyperbus read . . . 278
Figure 66. OctoSPI Hyperbus read with double latency . . . 278
Figure 67. OctoSPI Hyperbus write . . . 279
Figure 68. DCMI timing diagram . . . 280
Figure 69. SDIO high-speed mode . . . 284
Figure 70. SD default mode . . . 284
Figure 71. DDR mode . . . 284
Figure 72. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline . . . 285
Figure 73. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array recommended footprint . . . 286
Figure 74. UFBGA169 marking (package top view) . . . 287
Figure 75. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package outline . . . 288
Figure 76. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package recommended footprint . . . 289
Figure 77. UFBGA144 marking (package top view) . . . 290
Figure 78. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline . . . 291
Figure 79. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint . . . 293
Figure 80. LQFP144 marking (package top view) . . . 294
Figure 81. LQFP144 external SMPS device marking (package top view)(2) . . . 294
Figure 82. WLCSP - 144 bump, 5.24x 5.24 mm, 0.40 mm pitch, wafer level chip scale, package outline. . . . 295
Figure 83. WLCSP - 144 bump, 5.24x 5.24 mm, 0.40 mm pitch, wafer level chip scale, recommended footprint . . . 296
Figure 84. WLCSP144 marking (package top view) . . . 297
Figure 85. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package outline. . . . 298
Figure 86. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package recommended footprint . . . 299
Figure 87. UFBGA132 marking (package top view) . . . 300
Figure 88. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline . . . 301
Figure 89. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint . . . 302
Figure 90. LQFP100 marking (package top view) . . . 303

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L4Rxxx microcontrollers.

This document should be read in conjunction with the STM32L4Rxxx reference manual (RM0432). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the Arm®(a) Cortex®-M4 core, please refer to the Cortex®-M4 Technical Reference Manual, available from the www.arm.com website.

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Description

The STM32L4R5xx, STM32L4R7xx and STM32L4R9xx devices are an ultra-low-power microcontrollers family (STM32L4+ Series) based on the high-performance Arm® Cortex®-M4 32-bit RISC core. They operate at a frequency of up to 120 MHz.

The Cortex-M4 core features a single-precision floating-point unit (FPU), which supports all the Arm® single-precision data-processing instructions and all the data types. The Cortex-M4 core also implements a full set of DSP (digital signal processing) instructions and a memory protection unit (MPU) which enhances the application's security.

These devices embed high-speed memories (2 Mbytes of Flash memory and 640 Kbytes of SRAM), a flexible external memory controller (FSMC) for static memories (for devices with packages of 100 pins and more), two OctoSPI Flash memories interface (available on all packages) and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The STM32L4Rxxx devices embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, proprietary code readout protection and a firewall.

These devices offer a fast 12-bit ADC (5 Msps), two comparators, two operational amplifiers, two DAC channels, an internal voltage reference buffer, a low-power RTC, two general-purpose 32-bit timer, two 16-bit PWM timers dedicated to motor control, seven general-purpose 16-bit timers, and two 16-bit low-power timers. The devices support four digital filters for external sigma delta modulators (DFSDM). In addition, up to 24 capacitive sensing channels are available.

They also feature standard and advanced communication interfaces such as:

- Four I2Cs
- Three SPIs
- Three USARTs, two UARTs and one low-power UART
- Two SAIs
- One SDMMC
- One CAN
- One USB OTG full-speed
- Camera interface
- DMA2D controller

The devices operate in the -40 to +85 °C (+105 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V for V_{DD} power supply when using internal LDO regulator and a 1.05 to 1.32 V V_{DD12} power supply when using external SMPS supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported like an analog independent supply input for ADC, DAC, OPAMPs and comparators, a 3.3 V dedicated supply input for USB and up to 14 I/Os, which can be supplied independently down to 1.08 V. A VBAT input allows to backup the RTC and backup the registers. Dedicated V_{DD12} power supplies can be used to bypass the internal LDO regulator when connected to an external SMPS.

The STM32L4Rxxx family offers six packages from 100-pin to 169-pin.

Table 2. STM32L4R5xx, STM32L4R7xx and STM32L4R9xx features and peripheral counts

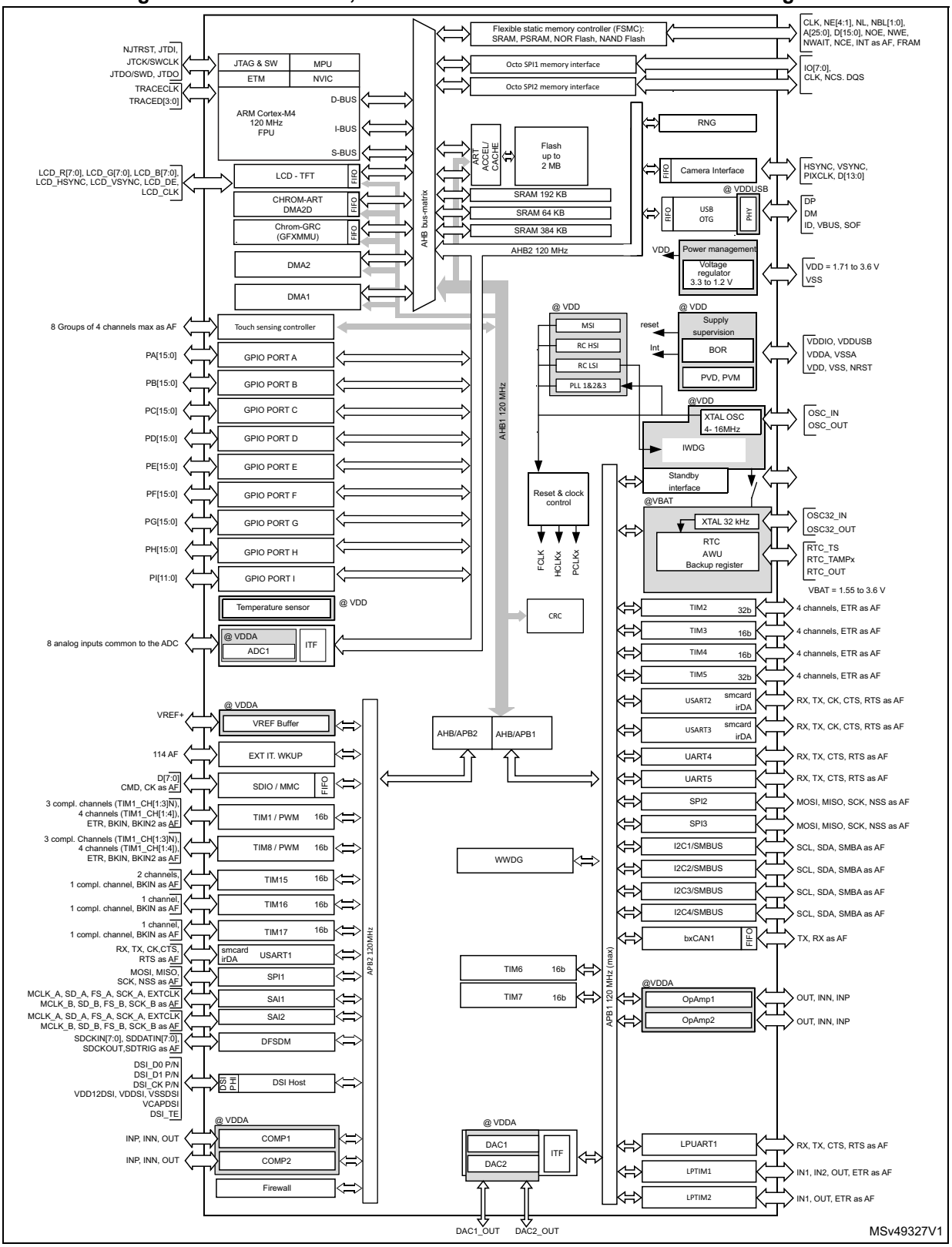
Peripheral		R5VI R5VG	R7VI	R9VI R9VG	R5QI R5QG	R5ZI R5ZG	R7ZI	R9ZI R9ZG	R5AI R5AG	R7AI	R9AI R9AG
Flash memory		1 Mbyte for xxxG devices 2 Mbyte for xxxI devices									
SRAM	System	640 (192 + 64 + 384) Kbyte									
	Backup	128 byte									
External memory controller for static memories (FSMC)		Yes(1)			Yes						
OctoSPI		2									
Timers	Advanced control	2 (16-bit)									
	General purpose	5 (16-bit) 2 (32-bit)									
	Basic	2 (16-bit)									
	Low-power	2 (16-bit)									
	SysTick timer	1									
	Watchdog timers (independent, window)	2									
Comm. interfaces	SPI	3									
	I^2C	4									
	USART/UART UART LPUART	3 2 1									
	SAI	2									
	CAN	1									
	USB OTG FS	Yes									
	SDMMC	Yes									
Digital filters for sigma-delta modulators		Yes (4 filters)									
Number of channels		8									
RTC		Yes									
Tamper pins		3									
Camera interface		Yes									
Chrom-ART Accelerator™		Yes									
Chrom-GRC™		No	Yes		No		Yes		No		Yes

Table 2. STM32L4R5xx, STM32L4R7xx and STM32L4R9xx features and peripheral counts (continued)

Peripheral	R5VI R5VG	R7VI	R9VI R9VG	R5QI R5QG	R5ZI R5ZG	R7ZI	R9ZI R9ZG	R5AI R5AG	R7AI	R9AI R9AG
LCD - TFT	No	Yes		No		Yes		No	Yes	
MIPI DSI Host(2)	No		Yes	No			Yes	No		Yes
Random number generator	Yes									
GPIOs(3) Wakeup pins Nb of I/Os down to 1.08 V	83 5 0		77 4 0	110 5 14	115 5 14		112 5 11	140 5 14		131 4 13
Capacitive sensing Number of channels	21		18	24						
12-bit ADCs Number of channels	1									
	16		14	16						14
12-bit DAC Number of channels	2 2									
Internal voltage reference buffer	Yes									
Analog comparator	2									
Operational amplifiers	2									
Max. CPU frequency	120 MHz									
Operating voltage (V_{DD})	1.71 to 3.6 V									
Operating voltage (V_{DD12})	1.05 to 1.32 V									
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 105 °C / -40 to 125 °C									
Packages	LQFP100			UFBGA132	LQFP144 WLCSP144	LQFP144	LQFP144, UFBGA144 WLCSP144	UFBGA169		

1. For the LQFP100 package, only FMC bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 chip select.
2. The DSI Host interface is only available on the STM32L4R9xx sales types.
3. In the case of an external SMPS package type is used, 2 GPIOs are replaced by V_{DD12} pins to connect the SMPS power supplies hence reducing the number of available GPIOs by 2.

Figure 1. STM32L4R5xx, STM32L4R7xx and STM32L4R9xx block diagram



Note: AF: alternate function on I/O pins.

3 Functional overview

3.1 Arm® Cortex®-M4 core with FPU

The Arm® Cortex®-M4 with FPU processor is the latest generation of Arm® processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of the MCU implementation, with a reduced pin count and with low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU 32-bit RISC processor features an exceptional code-efficiency, delivering the expected high-performance from an Arm® core in a memory size usually associated with 8-bit and 16-bit devices.

The processor supports a set of DSP instructions which allows an efficient signal processing and a complex algorithm execution. Its single precision FPU speeds up the software development by using metalanguage development tools to avoid saturation.

With its embedded Arm® core, the STM32L4Rxxx family is compatible with all Arm® tools and software.

Figure 1 shows the general block diagram of the STM32L4Rxxx family devices.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator that is optimized for the STM32 industry-standard Arm®Cortex®-M4 processors. It balances the inherent performance advantage of the Arm® Cortex®-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor near 150 DMIPS performance at 120 MHz, the accelerator implements an instruction prefetch queue and a branch cache, which increases the program's execution speed from the Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from the Flash memory at a CPU frequency of up to 120 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to the memory and to prevent one task to accidentally corrupt the memory or the resources used by any other active task. This memory area is organized into up to eight protected areas, which can be divided in up into eight subareas each. The protection area sizes range between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded Flash memory

The STM32L4Rxxx devices feature 2 Mbytes of embedded Flash memory which is available for storing programs and data.

The Flash interface features:

- Single or dual bank operating modes
- Read-while-write (RWW) in dual bank mode

This feature allows to perform a read operation from one bank while an erase or program operation is performed to the other bank. The dual bank boot is also supported. Each bank contains 256 pages of 4 or 8 Kbytes (depending on the read access width).

Flexible protections can be configured thanks to the option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels of protection are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection; the Flash memory cannot be read from or written to if either the debug features are connected or the boot in RAM or bootloader are selected
  - Level 2: chip readout protection; the debug features (Cortex-M4 JTAG and serial wire), the boot in RAM and the bootloader selection are disabled (JTAG fuse). This selection is irreversible.

Table 3. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A(1)	No	No	N/A(1)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	Yes(1)	No	No	No(1)
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. Erased when RDP change from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming:
  - In single bank mode, four areas can be selected with 8-Kbyte granularity.
  - In dual bank mode, two areas per bank can be selected with 4-Kbyte granularity.

- Proprietary code readout protection (PCROP): a part of the Flash memory can be protected against read and write from third parties. The protected area is execute-only and it can only be reached by the STM32 CPU as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited:
  – In single bank mode, two areas can be selected with 128-bit granularity.
  – In dual bank mode, one area per bank can be selected with 64-bit granularity.

  An additional option bit (PCROP_RDP) allows to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- Single error detection and correction
- Double error detection
- The address of the ECC fail can be read in the ECC register.

3.5 Embedded SRAM

The STM32L4R5xx, STM32L4R7xx and STM32L4R9xx devices feature 640 Kbytes of embedded SRAM. This SRAM is split into three blocks:

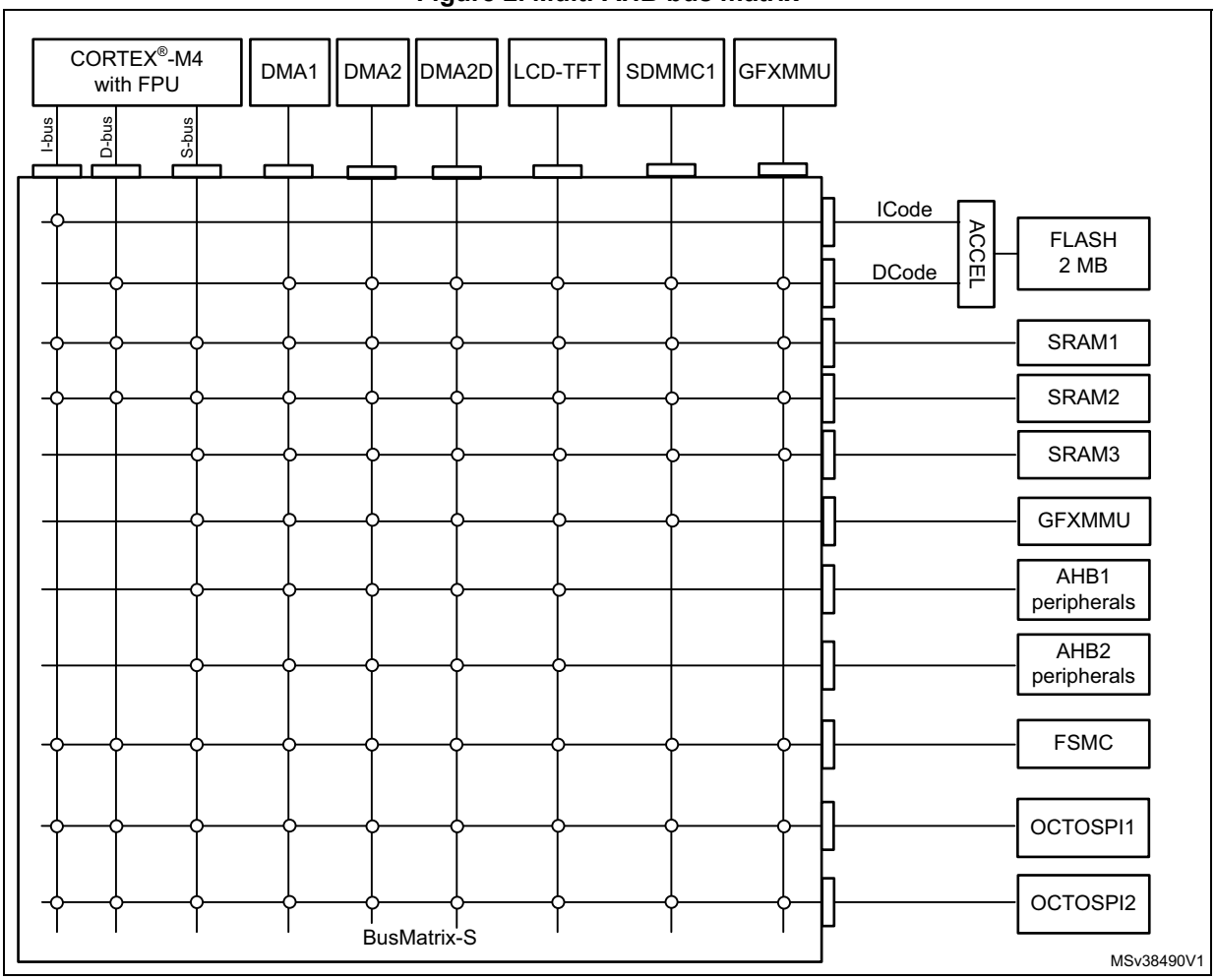
- 192 Kbytes mapped at address 0x2000 0000 (SRAM1).
- 64 Kbytes located at address 0x1000 0000 with hardware parity check (SRAM2). This memory is also mapped at address 0x2003 0000 offering a contiguous address space with the SRAM1.
  This block is accessed through the ICode/DCode buses for maximum performance.
  These 64 Kbytes SRAM can also be retained in Standby mode.
  The SRAM2 can be write-protected with 1 Kbyte granularity.
- 384 Kbytes mapped at address 0x2004 0000 - (SRAM3).

The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.6 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, DMA2D, SDMMC1, LCD-TFT and GFXMMU) and the slaves (Flash memory, RAM, FMC, OctoSPI, AHB and APB peripherals). It also ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 2. Multi-AHB bus matrix



3.7 Firewall

These devices embed a firewall which protects code sensitive and secure data from any access performed by a code executed outside of the protected areas.

Each illegal access generates a reset which kills immediately the detected intrusion.

The main features of the firewall are the following:

- Three segments can be protected and defined thanks to the firewall registers:
  - Code segment (located in Flash or SRAM1 if defined as executable protected area)
  - Non-volatile data segment (located in Flash)
  - Volatile data segment (located in SRAM1)
- The start address and the length of each segment are configurable:
  - Code segment: up to 2048 Kbytes with granularity of 256 bytes
  - Non-volatile data segment: up to 2048 Kbytes with granularity of 256 bytes
  - Volatile data segment: up to 192 Kbytes of SRAM1 with a granularity of 64 bytes
- Specific mechanism implemented to open the firewall to get access to the protected areas (call gate entry sequence)
- Volatile data segment can be shared or not with the non-protected code
- Volatile data segment can be executed or not depending on the firewall configuration

The Flash readout protection must be set to level 2 in order to reach the expected level of protection.

3.8 Boot modes

At startup, a BOOT0 pin and an nBOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The BOOT0 value may come from the PH3-BOOT0 pin or from an option bit depending on the value of a user option bit to free the GPIO pad if needed.

A Flash empty-check mechanism is implemented to force the boot from system Flash if the first Flash memory location is not programmed and if the boot selection is configured to boot from main Flash.

The boot loader is located in the system memory. It is used to reprogram the Flash memory by using USART, I2C, SPI, CAN or USB OTG FS in device mode through the DFU (device firmware upgrade).

3.9 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator with polynomial value and size.

Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean to verify the Flash memory integrity.

The CRC calculation unit helps to compute a signature of the software during runtime, which can be ulteriorly compared with a reference signature generated at link-time and which can be stored at a given memory location.

3.10 Power supply management

3.10.1 Power supply schemes

The STM32L4x devices require a 1.71 V to 3.6 V V_{DD} operating voltage supply. Several independent supplies can be provided for specific peripherals:

- V_{DD} = 1.71 V to 3.6 V
  V_{DD} is the external power supply for the I/Os, the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through the VDD pins.
- V_{DD12} = 1.05 to 1.32 V
  V_{DD12} is the external power supply bypassing the internal regulator when connected to an external SMPS. It is provided externally through VDD12 pins and only available on packages with the external SMPS supply option. VDD12 does not require any external decoupling capacitance and cannot support any external load.
- V_{DDA} = 1.62 V (ADCs/COMPs) / 1.8 V (DACs/OPAMPs) to 2.4 V (VREFBUF) to 3.6 V
  V_{DDA} is the external analog power supply for A/D converters, D/A converters, voltage reference buffer, operational amplifiers and comparators. The V_{DDA} voltage level is independent from the V_{DD} voltage and should preferably be connected to V_{DD} when these peripherals are not used.
- VDDUSB = 3.0 V to 3.6 V
  VDDUSB is the external independent power supply for USB transceivers. The VDDUSB voltage level is independent from the VDD voltage and should preferably be connected to VDD when the USB is not used.
- VDDIO2 = 1.08 V to 3.6 V
- VDDIO2 is the external power supply for 14 I/Os (port G[15:2]). The VDDIO2 voltage level is independent from the VDD voltage and should preferably be connected to VDD when PG[15:2] are not used.
- VDDDSI is used to supply the DSI regulator and MIPI D-PHY. This supply must be connected to the global VDD.
- VCAPDSI pin is the output of DSI regulator (1.2 V) which must be connected externally to VDD12DSI.
- VDD12DSI pin is used to supply the MIPI D-PHY, and to supply clock and data lanes pins. An external capacitor of 2.2 uF must be connected on the VDD12DSI pin.
- V_{BAT} = 1.55 V to 3.6 V
  V_{BAT} is the power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
- V_{REF-}, V_{REF+}
  V_{REF+} is the input reference voltage for ADCs and DACs. It is also the output of the internal voltage reference buffer when enabled.
  When V_{DDA} < 2 V V_{REF+} must be equal to V_{DDA}.
  When V_{DDA} ≥ 2 V V_{REF+} must be between 2 V and V_{DDA}.
  V_{REF+} can be grounded when ADC and DAC are not active.
  The internal voltage reference buffer supports two output voltages, which are configured with VRS bit in the VREFBUF_CSR register:
  - V_{REF+} around 2.048 V. This requires V_{DDA} equal to or higher than 2.4 V.
  - V_{REF+} around 2.5 V. This requires V_{DDA} equal to or higher than 2.8 V.

VREF- and VREF+ pins are not available on all packages. When not available, they are bonded to VSSA and VDDA, respectively.
When the VREF+ is double-bonded with VDDA in a package, the internal voltage reference buffer is not available and must be kept disable (refer to datasheet for packages pinout description).
V_{REF-} must always be equal to V_{SSA}.

An embedded linear voltage-regulator is used to supply the internal digital power V_{CORE}. V_{CORE} is the power supply for digital peripherals, SRAM1, SRAM2 and SRAM3. The Flash is supplied by V_{CORE} and V_{DD}.

Figure 3. STM32L4R5xx and STM32L4R7xx power supply overview

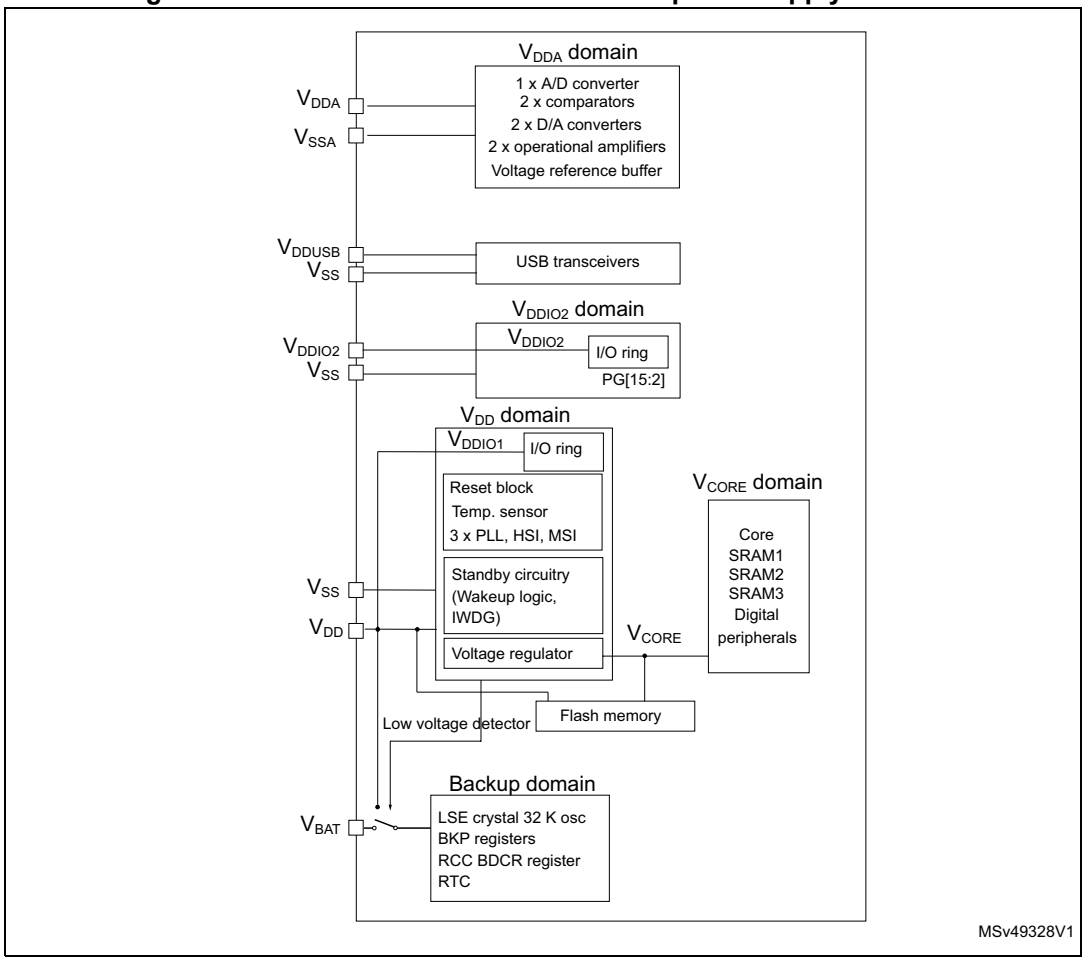
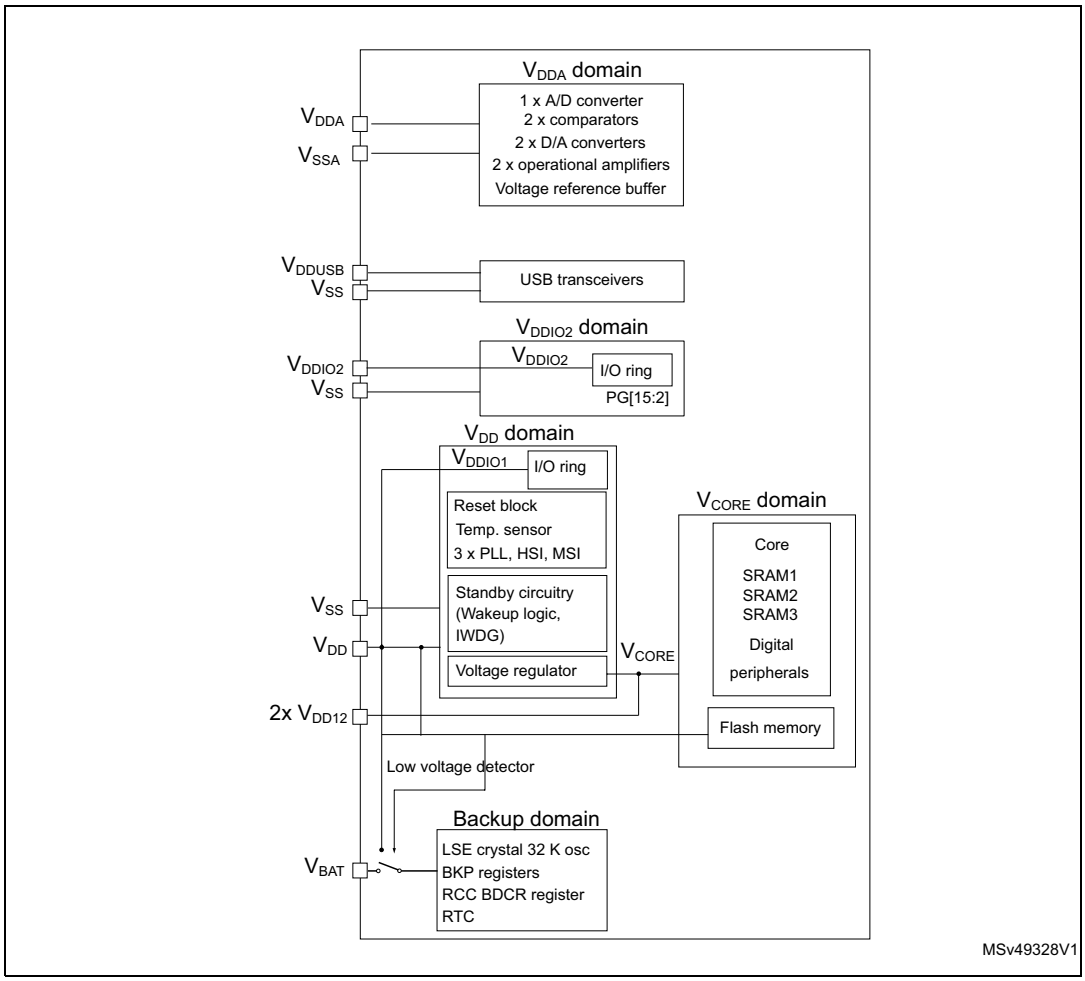



Figure 4. STM32L4R5xxxP and STM32L4R7xxxP with external SMPS power supply overview