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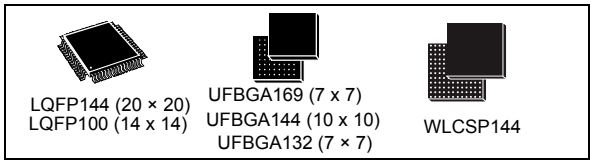
STM32L4S5xx STM32L4S7xx STM32L4S9xx

Ultra-low-power Arm® Cortex®-M4 32-bit MCU+FPU, 150DMIPS, up to 2MB Flash, 640KB SRAM, LCD-TFT & MIPI DSI, AES+HASH

Datasheet- production data

Features

- Ultra-low-power with FlexPowerControl
  - 1.71 V to 3.6 V power supply
  - -40 °C to 85/125 °C temperature range
  - Batch acquisition mode (BAM)
  - 305 nA in VBAT mode: supply for RTC and 32x32-bit backup registers
  - 33 nA Shutdown mode (5 wakeup pins)
  - 125 nA Standby mode (5 wakeup pins)
  - 420 nA Standby mode with RTC
  - 2.8 µA Stop 2 with RTC
  - 110 µA/MHz Run mode
  - 5 µs wakeup from Stop mode
  - Brownout reset (BOR) in all modes except shutdown
  - Interconnect matrix
- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, adaptive real-time accelerator (ART Accelerator™) allowing 0-wait-state execution from Flash memory, frequency up to 120 MHz, MPU, 150 DMIPS/1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Performance benckmark
  - 1.25 DMIPS/MHz (Drystone 2.1)
  - 409.20 Coremark® (3.41 Coremark/MHz @120 MHz)
- Energy benckmark
  - 233 ULPMark™CP score
  - 56.5 ULPMark™PP score
- Clock sources
  - 4 to 48 MHz crystal oscillator
  - 32 kHz crystal oscillator for RTC (LSE)
  - Internal 16 MHz factory-trimmed RC (±1%)
  - Internal low-power 32 kHz RC (±5%)
  - Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than ±0.25 % accuracy)
  - Internal 48 MHz with clock recovery



  - 3 PLLs for system clock, USB, audio, ADC
- RTC with HW calendar, alarms and calibration
- Up to 24 capacitive sensing channels: support touchkey, linear and rotary touch sensors
- Advanced graphics features
  - Chrom-ART Accelerator™ (DMA2D) for enhanced graphic content creation
  - Chrom-GRC™ (GFXMMU) allowing up to 20% of graphic resources optimization
  - MIPI® DSI Host controller with two DSI lanes running at up to 500 Mbits/s each
  - LCD-TFT controller
- 16x timers: 2 x 16-bit advanced motor-control, 2 x 32-bit and 5 x 16-bit general purpose, 2x 16-bit basic, 2x low-power 16-bit timers (available in Stop mode), 2x watchdogs, SysTick timer
- Up to 136 fast I/Os, most 5 V-tolerant, up to 14 I/Os with independent supply down to 1.08 V
- Memories
  - 2-Mbyte Flash, 2 banks read-while-write, proprietary code readout protection
  - 640 Kbytes of SRAM including 64 Kbytes with hardware parity check
  - External memory interface for static memories supporting SRAM, PSRAM, NOR, NAND and FRAM memories
  - 2 x OctoSPI memory interface
- 4x digital filters for sigma delta modulator
- Rich analog peripherals (independent supply)
  - 12-bit ADC 5 Msps, up to 16-bit with hardware oversampling, 200 µA/Msps
  - 2x 12-bit DAC, low-power sample and hold
  - 2x operational amplifiers with built-in PGA

  - 2x ultra-low-power comparators
- 20x communication interfaces
  - USB OTG 2.0 full-speed, LPM and BCD
  - 2x SAIs (serial audio interface)
  - 4x I2C FM+(1 Mbit/s), SMBus/PMBus
  - 6x USARTs (ISO 7816, LIN, IrDA, modem)
  - 3x SPIs (5x SPIs with the dual OctoSPI)
  - CAN (2.0B Active) and SDMMC
- 14-channel DMA controller
- True random number generator
- CRC calculation unit, 96-bit unique ID
- 8- to 14-bit camera interface up to 32 MHz (black and white) or 10 MHz (color)
- Encryption hardware accelerator: AES (128/256-bit key), HASH (SHA-256)
- Development support: serial wire debug (SWD), JTAG, Embedded Trace Macrocell (ETM)

Table 1. Device summary

Reference	Part numbers
STM32L4S5xx	STM32L4S5VI, STM32L4S5QI, STM32L4S5ZI, STM32L4S5AI
STM32L4S7xx	STM32L4S7VI, STM32L4S7ZI, STM32L4S7AI
STM32L4S9xx	STM32L4S9VI, STM32L4S9ZI, STM32L4S9AI

Contents

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List of figures

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L4Sxxx microcontrollers.

This document should be read in conjunction with the STM32L4Sxxx reference manual (RM0432). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the Arm®[a] Cortex®-M4 core, please refer to the Cortex®-M4 Technical Reference Manual, available from the www.arm.com website.

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2 Description

The STM32L4S5xx, STM32L4S7xx and STM32L4S9xx devices are an ultra-low-power microcontrollers family (STM32L4+ Series) based on the high-performance Arm® Cortex®-M4 32-bit RISC core. They operate at a frequency of up to 120 MHz.

The Cortex-M4 core features a single-precision floating-point unit (FPU), which supports all the Arm® single-precision data-processing instructions and all the data types. The Cortex-M4 core also implements a full set of DSP (digital signal processing) instructions and a memory protection unit (MPU) which enhances the application's security.

These devices embed high-speed memories (2 Mbytes of Flash memory and 640 Kbytes of SRAM), a flexible external memory controller (FSMC) for static memories (for devices with packages of 100 pins and more), two OctoSPI Flash memories interface (available on all packages) and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The STM32L4Sxxx devices embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, proprietary code readout protection and a firewall.

These devices offer a fast 12-bit ADC (5 Msps), two comparators, two operational amplifiers, two DAC channels, an internal voltage reference buffer, a low-power RTC, two general-purpose 32-bit timer, two 16-bit PWM timers dedicated to motor control, seven general-purpose 16-bit timers, and two 16-bit low-power timers. The devices support four digital filters for external sigma delta modulators (DFSDM). In addition, up to 24 capacitive sensing channels are available.

They also feature standard and advanced communication interfaces such as:

- Four I2Cs
- Three SPIs
- Three USARTs, two UARTs and one low-power UART
- Two SAIs
- One SDMMC
- One CAN
- One USB OTG full-speed
- Camera interface
- DMA2D controller

The STM32L4S5xx, STM32L4S7xx and STM32L4S9xx devices embed an AES and a HASH hardware accelerator.

The devices operate in the -40 to +85 °C (+105 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported like an analog independent supply input for ADC, DAC, OPAMPs and comparators, a 3.3 V dedicated supply input for USB and up to 14 I/Os, which can be supplied independently down to 1.08 V. A VBAT input allows to backup the RTC and backup the registers.

The STM32L4Sxxx family offers six packages from 100-pin to 169-pin.

Table 2. STM32L4S5xx, STM32L4S7xx and STM32L4S9xx features and peripheral counts

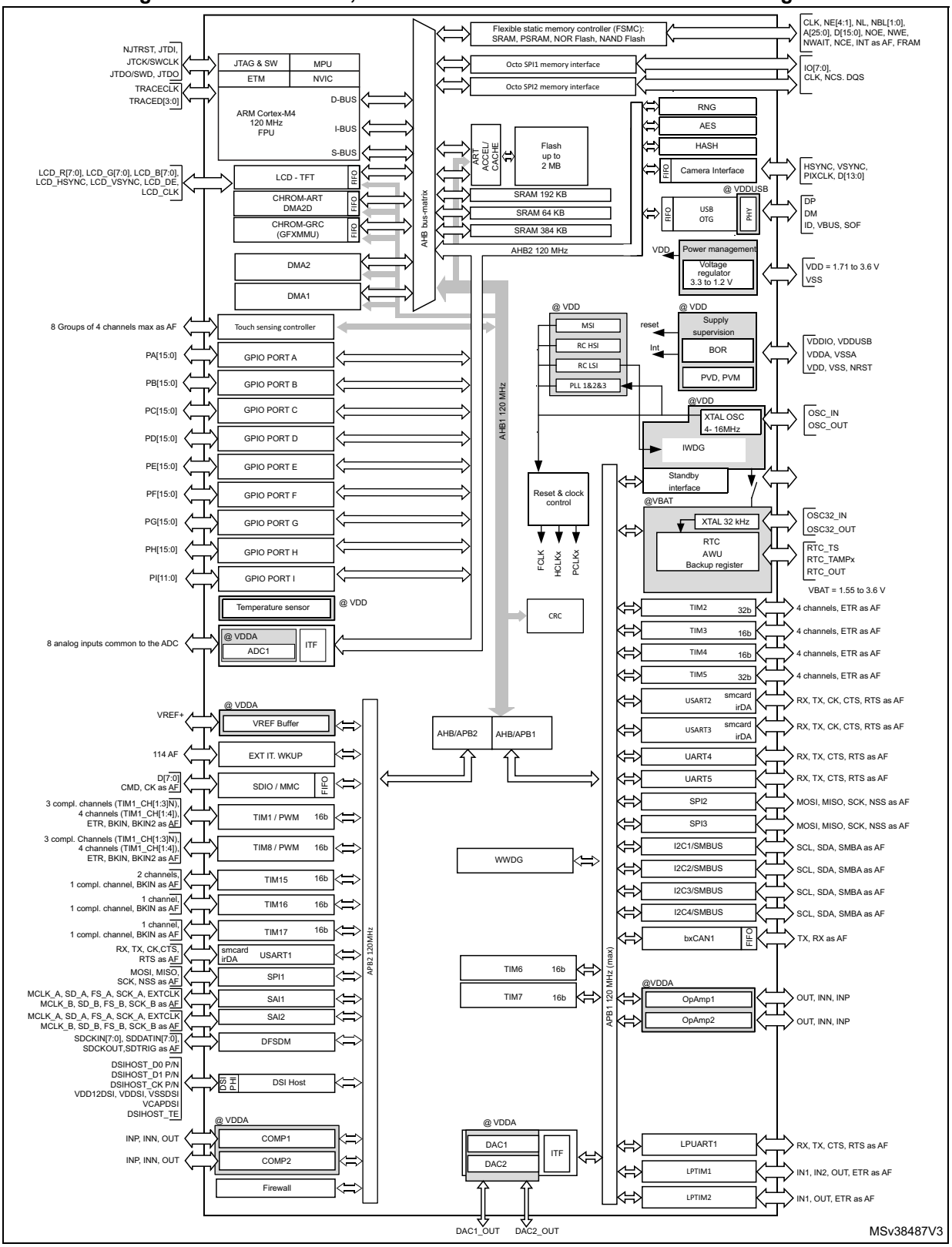
Peripheral		S5VI	S7VI	S9VI	S5QI	S5ZI	S7ZI	S9ZI	S5AI	S7AI	S9AI
Flash memory		2 Mbytes									
SRAM	System	640 (192 + 64 + 384) Kbytes									
	Backup	128 bytes									
External memory controller for static memories (FSMC)		Yes(1)			Yes						
OctoSPI		2									
Timers	Advanced control	2 (16-bit)									
	General purpose	5 (16-bit) 2 (32-bit)									
	Basic	2 (16-bit)									
	Low-power	2 (16-bit)									
	SysTick timer	1									
	Watchdog timers (independent, window)	2									
Comm. interfaces	SPI	3									
	I^2C	4									
	USART/UART UART LPUART	3 2 1									
	SAI	2									
	CAN	1									
	USB OTG FS	Yes									
	SDMMC	Yes									
Digital filters for sigma-delta modulators		Yes (4 filters)									
Number of channels		8									
RTC		Yes									
Tamper pins		3									
Camera interface		Yes									
Chrom-ART Accelerator™		Yes									
Chrom-GRC™		No	Yes		No		Yes		No		Yes

Table 2. STM32L4S5xx, STM32L4S7xx and STM32L4S9xx features and peripheral counts (continued)

Peripheral	S5VI	S7VI	S9VI	S5QI	S5ZI	S7ZI	S9ZI	S5AI	S7AI	S9AI
LCD - TFT	No	Yes		No		Yes		No	Yes	
MIPI DSI Host(2)	No		Yes	No			Yes	No		Yes
Random number generator	Yes									
AES + HASH	Yes									
GPIOs Wakeup pins Nb of I/Os down to 1.08 V	83 5 0		77 4 0	110 5 14	115 5 14		112 5 11	140 5 14		131 4 13
Capacitive sensing Number of channels	21		18	24						
12-bit ADCs Number of channels	1									
	16		14	16						14
12-bit DAC Number of channels	2 2									
Internal voltage reference buffer	Yes									
Analog comparator	2									
Operational amplifiers	2									
Max. CPU frequency	120 MHz									
Operating voltage	1.71 to 3.6 V									
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 125 °C									
Packages	LQFP100			UFBGA 132	LQFP 144 WLCSP144	LQFP 144	LQFP 144, UFBGA 144 WLCSP 144	UFBGA169		
Bootloader	USART 1	USART 2	USART 3	SPI1	SPI2	I2C1	I2C2	I2C3	CAN1	USB through DFU

1. For the LQFP100 package, only FMC bank1 and NAND bank are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 chip select.
2. The DSI Host interface is only available on the STM32L4S9xx sales types.

Figure 1. STM32L4S5xx, STM32L4S7xx and STM32L4S9xx block diagram



Note: AF: alternate function on I/O pins.

3 Functional overview

3.1 Arm® Cortex®-M4 core with FPU

The Arm® Cortex®-M4 with FPU processor is the latest generation of Arm® processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of the MCU implementation, with a reduced pin count and with low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU 32-bit RISC processor features an exceptional code-efficiency, delivering the expected high-performance from an Arm® core in a memory size usually associated with 8-bit and 16-bit devices.

The processor supports a set of DSP instructions which allows an efficient signal processing and a complex algorithm execution. Its single precision FPU speeds up the software development by using metalanguage development tools to avoid saturation.

With its embedded Arm® core, the STM32L4Sxxx family is compatible with all Arm® tools and software.

Figure 1 shows the general block diagram of the STM32L4Sxxx family devices.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator that is optimized for the STM32 industry-standard Arm®Cortex®-M4 processors. It balances the inherent performance advantage of the Arm® Cortex®-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor near 150 DMIPS performance at 120 MHz, the accelerator implements an instruction prefetch queue and a branch cache, which increases the program's execution speed from the Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from the Flash memory at a CPU frequency of up to 120 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to the memory and to prevent one task to accidentally corrupt the memory or the resources used by any other active task. This memory area is organized into up to eight protected areas, which can be divided in up into eight subareas each. The protection area sizes range between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded Flash memory

The STM32L4Sxxx devices feature 2 Mbytes of embedded Flash memory which is available for storing programs and data.

The Flash interface features:

- Single or dual bank operating modes
- Read-while-write (RWW) in dual bank mode

This feature allows to perform a read operation from one bank while an erase or program operation is performed to the other bank. The dual bank boot is also supported. Each bank contains 256 pages of 4 or 8 Kbytes (depending on the read access width).

Flexible protections can be configured thanks to the option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels of protection are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection; the Flash memory cannot be read from or written to if either the debug features are connected or the boot in RAM or bootloader are selected
  - Level 2: chip readout protection; the debug features (Cortex-M4 JTAG and serial wire), the boot in RAM and the bootloader selection are disabled (JTAG fuse). This selection is irreversible.

Table 3. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A(1)	No	No	N/A(1)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	Yes(1)	No	No	No(1)
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. Erased when RDP change from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming:
  - In single bank mode, four areas can be selected with 8-Kbyte granularity.
  - In dual bank mode, two areas per bank can be selected with 4-Kbyte granularity.

- Proprietary code readout protection (PCROP): a part of the Flash memory can be protected against read and write from third parties. The protected area is execute-only and it can only be reached by the STM32 CPU as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited:
  - In single bank mode, two areas can be selected with 128-bit granularity.
  - In dual bank mode, one area per bank can be selected with 64-bit granularity.

  An additional option bit (PCROP_RDP) allows to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- Single error detection and correction
- Double error detection
- The address of the ECC fail can be read in the ECC register.

3.5 Embedded SRAM

The STM32L4S5xx, STM32L4S7xx and STM32L4S9xx devices feature 640 Kbytes of embedded SRAM. This SRAM is split into three blocks:

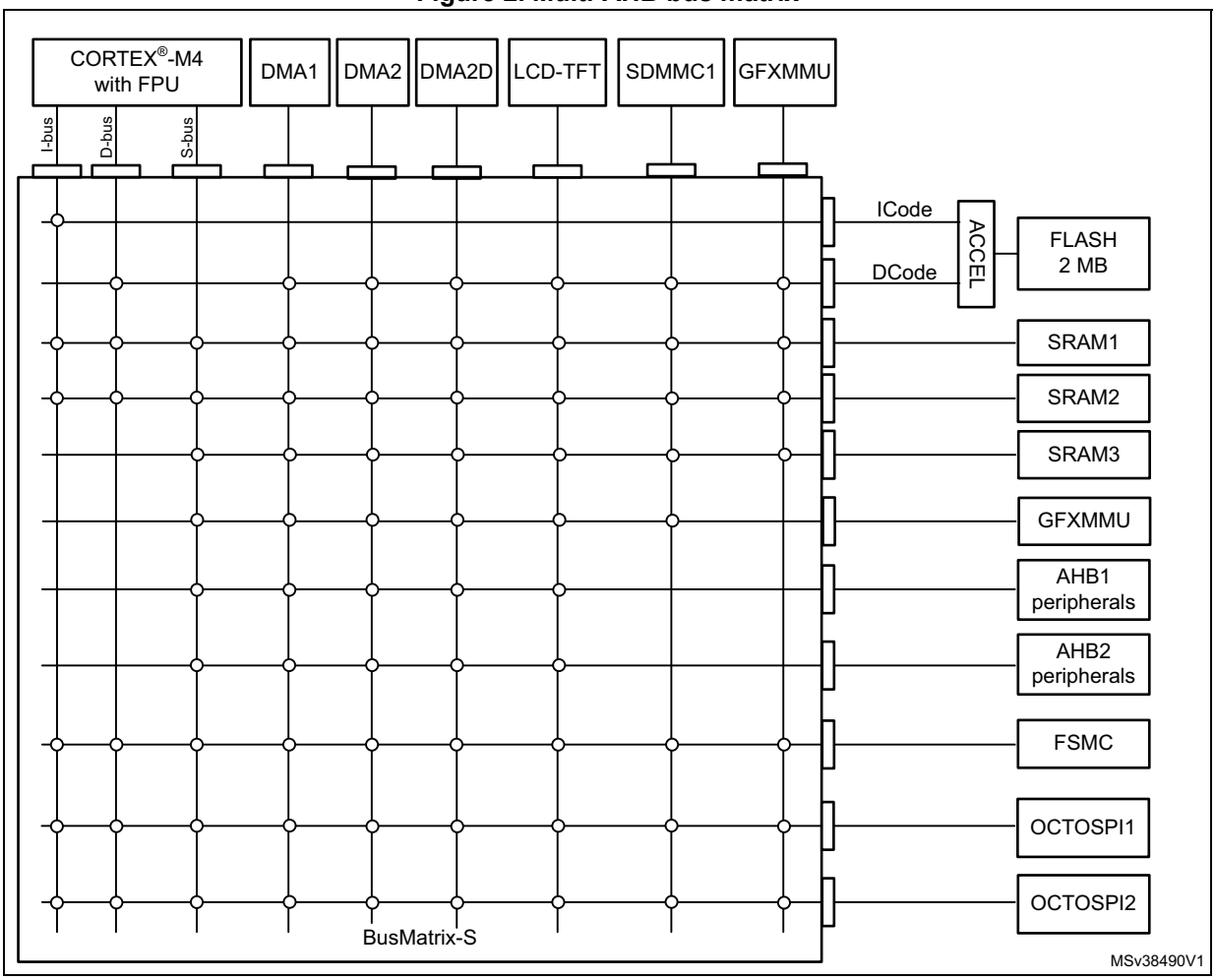
- 192 Kbytes mapped at address 0x2000 0000 (SRAM1).
- 64 Kbytes located at address 0x1000 0000 with hardware parity check (SRAM2). This memory is also mapped at address 0x2003 0000 offering a contiguous address space with the SRAM1.
  This block is accessed through the ICode/DCode buses for maximum performance.
  These 64 Kbytes SRAM can also be retained in Standby mode.
  The SRAM2 can be write-protected with 1 Kbyte granularity.
- 384 Kbytes mapped at address 0x2004 0000 - (SRAM3).

The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.6 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, DMA2D, SDMMC1, LCD-TFT and GFXMMU) and the slaves (Flash memory, RAM, FMC, OctoSPI, AHB and APB peripherals). It also ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 2. Multi-AHB bus matrix



3.7 Firewall

These devices embed a firewall which protects code sensitive and secure data from any access performed by a code executed outside of the protected areas.

Each illegal access generates a reset which kills immediately the detected intrusion.

The main features of the firewall are the following:

- Three segments can be protected and defined thanks to the firewall registers:
  - Code segment (located in Flash or SRAM1 if defined as executable protected area)
  - Non-volatile data segment (located in Flash)
  - Volatile data segment (located in SRAM1)
- The start address and the length of each segment are configurable:
  - Code segment: up to 2048 Kbytes with granularity of 256 bytes
  - Non-volatile data segment: up to 2048 Kbytes with granularity of 256 bytes
  - Volatile data segment: up to 192 Kbytes of SRAM1 with a granularity of 64 bytes
- Specific mechanism implemented to open the firewall to get access to the protected areas (call gate entry sequence)
- Volatile data segment can be shared or not with the non-protected code
- Volatile data segment can be executed or not depending on the firewall configuration

The Flash readout protection must be set to level 2 in order to reach the expected level of protection.

3.8 Boot modes

At startup, a BOOT0 pin and an nBOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The BOOT0 value may come from the PH3-BOOT0 pin or from an option bit depending on the value of a user option bit to free the GPIO pad if needed.

A Flash empty-check mechanism is implemented to force the boot from system Flash if the first Flash memory location is not programmed and if the boot selection is configured to boot from main Flash.

The boot loader is located in the system memory. It is used to reprogram the Flash memory by using USART, I2C, SPI, CAN or USB OTG FS in device mode through the DFU (device firmware upgrade).

3.9 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator with polynomial value and size.

Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean to verify the Flash memory integrity.

The CRC calculation unit helps to compute a signature of the software during runtime, which can be ulteriorly compared with a reference signature generated at link-time and which can be stored at a given memory location.

3.10 Power supply management

3.10.1 Power supply schemes

The STM32L4x devices require a 1.71 V to 3.6 V V_{DD} operating voltage supply. Several independent supplies can be provided for specific peripherals:

- V_{DD} = 1.71 V to 3.6 V

  V_{DD} is the external power supply for the I/Os, the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through the VDD pins.

-

  V_{DDA} = 1.62 V (ADCs/COMPs) / 1.8 V (DACs/OPAMPs) to 2.4 V (VREFBUF) to 3.6 V
  V_{DDA} is the external analog power supply for A/D converters, D/A converters, voltage reference buffer, operational amplifiers and comparators. The V_{DDA} voltage level is independent from the V_{DD} voltage and should preferably be connected to V_{DD} when these peripherals are not used.

- VDDUSB = 3.0 V to 3.6 V
  VDDUSB is the external independent power supply for USB transceivers. The VDDUSB voltage level is independent from the VDD voltage and should preferably be connected to VDD when the USB is not used.
- VDDIO2 = 1.08 V to 3.6 V
- VDDIO2 is the external power supply for 14 I/Os (port G[15:2]). The VDDIO2 voltage level is independent from the VDD voltage and should preferably be connected to VDD when PG[15:2] are not used.
- VDDDSI is an independent DSI power supply dedicated for is used to supply the DSI regulator and MIPI D-PHY. This supply must be connected to the global VDD.
- VCAPDSI pin is the output of DSI regulator (1.2 V) which must be connected externally to VDD12DSI.
- VDD12DSI pin is used to supply the MIPI D-PHY, and to supply clock and data lanes pins. An external capacitor of 2.2 uF must be connected on the VDD12DSI pin.
- V_{BAT} = 1.55 V to 3.6 V

  V_{BAT} is the power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

- VREF-, VREF+

  V_{REF+} is the input reference voltage for ADCs and DACs. It is also the output of the internal voltage reference buffer when enabled.

  When V_{DDA} < 2 V V_{REF+} must be equal to V_{DDA}.

  When V_{DDA} ≥ 2 V V_{REF+} must be between 2 V and V_{DDA}.

  V_{REF+} can be grounded when ADC and DAC are not active.

  The internal voltage reference buffer supports two output voltages, which are configured with VRS bit in the VREFBUF_CSR register:

  – V_{REF+} around 2.048 V. This requires V_{DDA} equal to or higher than 2.4 V.

  – V_{REF+} around 2.5 V. This requires V_{DDA} equal to or higher than 2.8 V.

  VREF- and VREF+ pins are not available on all packages. When not available, they are bonded to VSSA and VDDA, respectively.
  When the VREF+ is double-bonded with VDDA in a package, the internal voltage reference buffer is not available and must be kept disable (refer to datasheet for

packages pinout description).
V_{REF-} must always be equal to V_{SSA}.

An embedded linear voltage-regulator is used to supply the internal digital power V_{CORE}. V_{CORE} is the power supply for digital peripherals, SRAM1, SRAM2 and SRAM3. The Flash is supplied by V_{CORE} and V_{DD}.

Figure 3. STM32L4S5xx and STM32L4S7xx power supply overview

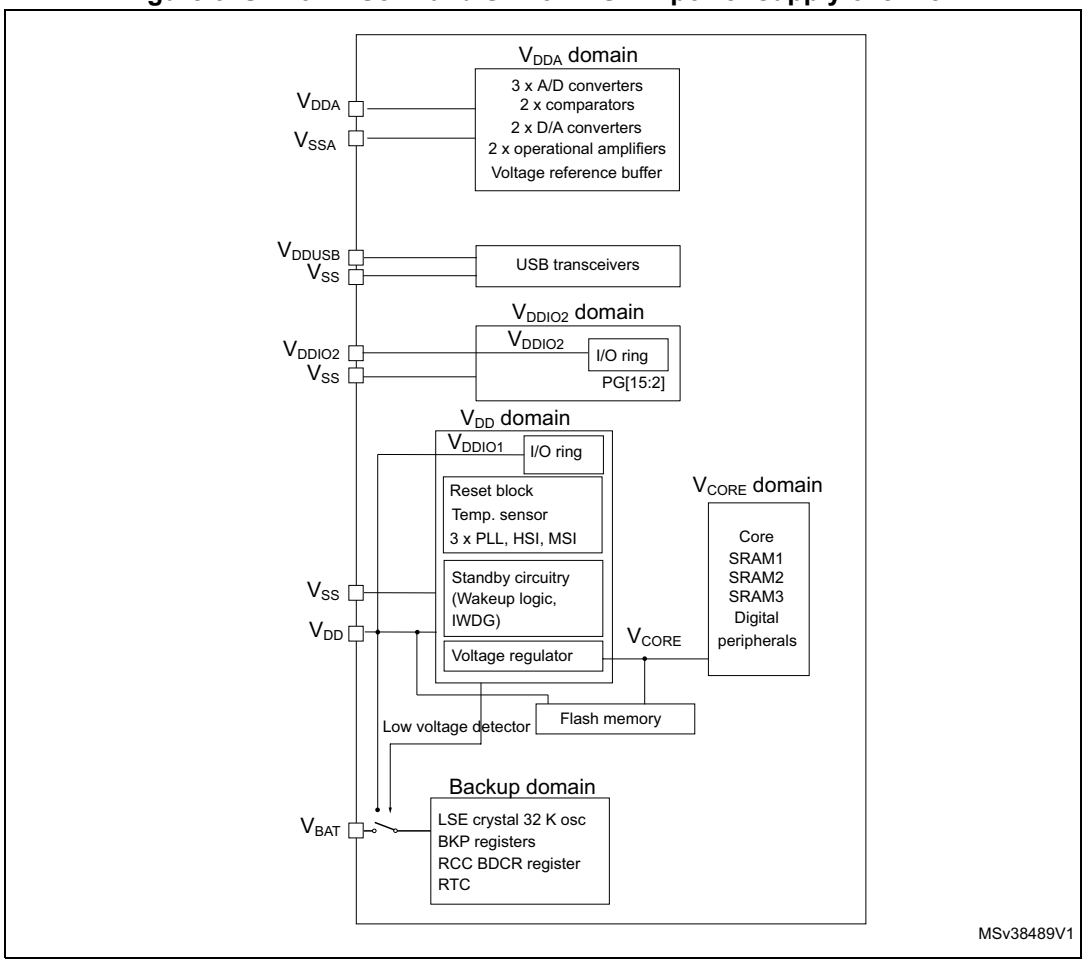
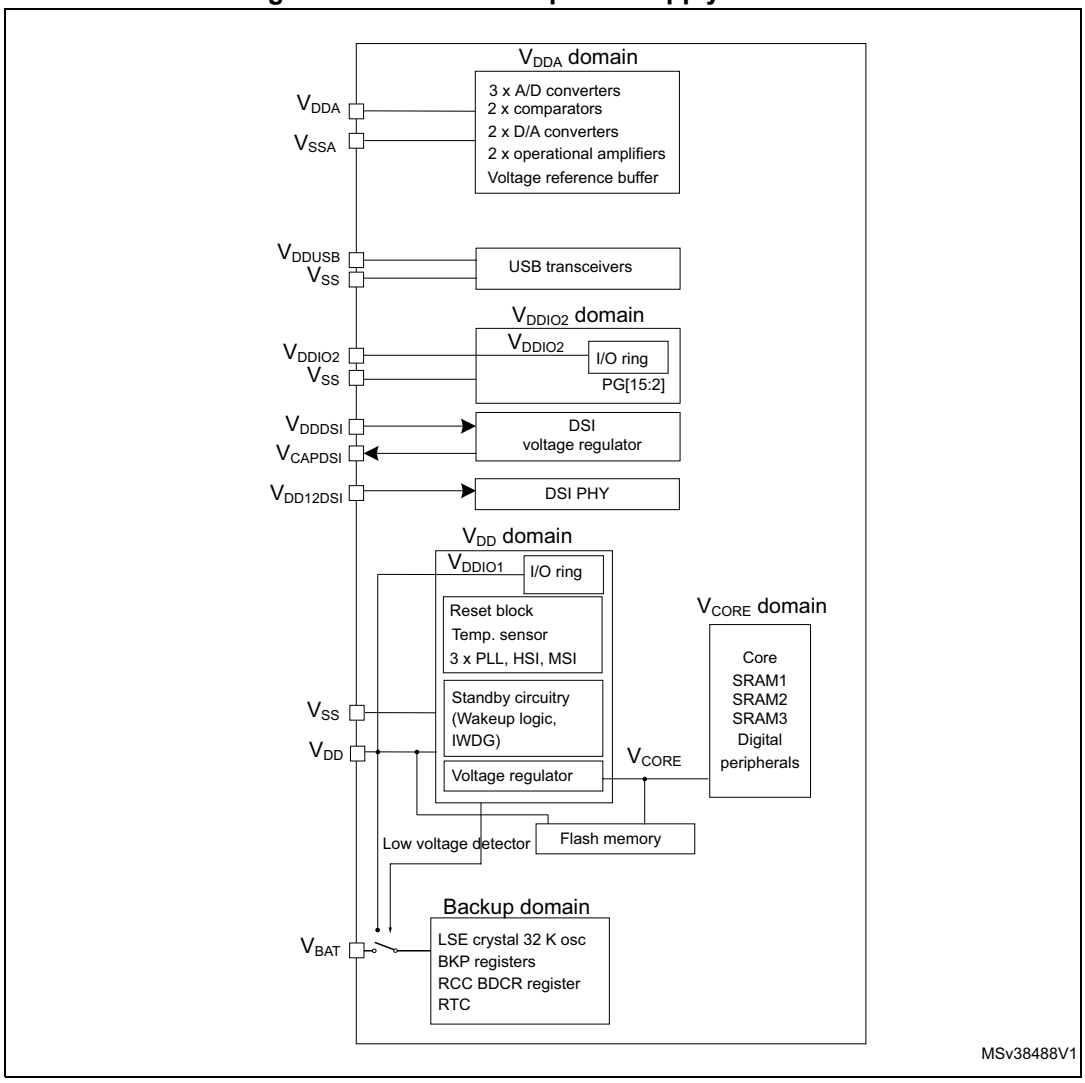


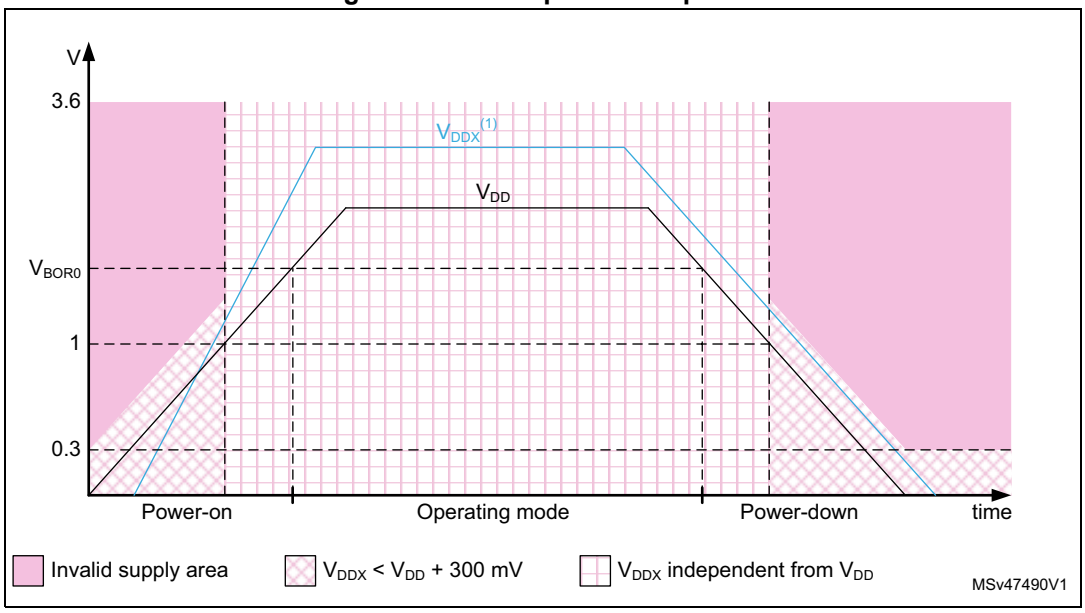
Figure 4. STM32L4S9xx power supply overview



During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA}, V_{DDIO2}, V_{DDUSB} and V_{LCD}) must remain below VDD +300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.
- During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ; this allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

Figure 5. Power-up/down sequence



1. V_{DDX} refers to any power supply among V_{DDA}, V_{DDIO2}, V_{DDUSB} and V_{LCD}.

3.10.2 Power supply supervisor

The STM32L4S5xx, STM32L4S7xx and STM32L4S9xx devices have an integrated ultra-low-power Brownout reset (BOR) active in all modes (except for Shutdown mode). The BOR ensures proper operation of the devices after power-on and during power-down. The devices remain in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71 V at power on, and other higher thresholds can be selected through option bytes.The devices feature an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold.

An interrupt can be generated when V_{DD} drops below the VPVD threshold and/or when V_{DD} is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the devices embed a peripheral voltage monitor which compares the independent supply voltages V_{DDA}, V_{DDUSB}, V_{DDIO2} with a fixed threshold in order to ensure that the peripheral is in its functional supply range.

3.10.3 Voltage regulator

Two embedded linear voltage regulators supply most of the digital circuitries: the main regulator (MR) and the low-power regulator (LPR).

- The MR is used in the Run and Sleep modes and in the Stop 0 mode.
- The LPR is used in Low-power run, Low-power sleep, Stop 1 and Stop 2 modes. It is also used to supply the 64 Kbytes SRAM2 in standby with RAM2 retention.
- Both regulators are in power-down while they are in standby and Shutdown modes: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.