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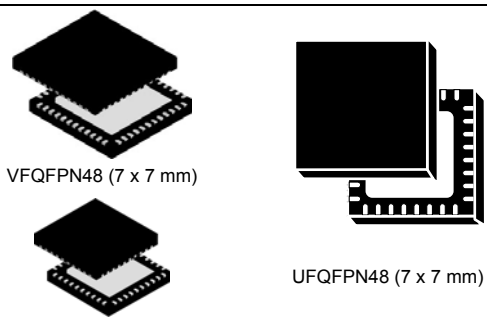
STM32W108HB STM32W108CB STM32W108CC STM32W108CZ

High-performance, IEEE 802.15.4 wireless system-on-chip with up to 256 Kbyte of embedded Flash memory

Datasheet - not recommended for new design

Features

- Complete system-on-chip
  - 32-bit ARM® Cortex®-M3 processor
  - 2.4 GHz IEEE 802.15.4 transceiver and lower MAC
  - 128/192/256-Kbyte Flash, 8/12/16-Kbyte RAM memory
  - AES128 encryption accelerator
  - Flexible ADC, SPI/UART/I^2C serial communications, and general-purpose timers
  - 24 highly configurable GPIOs with Schmitt trigger inputs
- Industry-leading ARM® Cortex®-M3 processor
  - Leading 32-bit processing performance
  - Highly efficient Thumb®-2 instruction set
  - Operation at 6, 12 or 24 MHz
  - Flexible nested vectored interrupt controller
- Low power consumption, advanced management
  - Receive current (w/ CPU): 27 mA
  - Transmit current (w/ CPU, +3 dBm TX): 31 mA
  - Low deep sleep current, with retained RAM and GPIO: 400 nA/800 nA with/without sleep timer
  - Low-frequency internal RC oscillator for low-power sleep timing
  - High-frequency internal RC oscillator for fast (100 µs) processor start-up from sleep
- Exceptional RF performance
  - Normal mode link budget up to 102 dB; configurable up to 107 dB
  - -99 dBm normal RX sensitivity; configurable to -100 dBm (1% PER, 20 byte packet)
  - +3 dB normal mode output power; configurable up to +8 dBm



  - Robust WiFi and Bluetooth coexistence
- Innovative network and processor debug
  - Non-intrusive hardware packet trace
  - Serial wire/JTAG interface
  - Standard ARM debug capabilities: Flash patch and breakpoint; data watchpoint and trace; instrumentation trace macrocell
- Application flexibility
  - Single voltage operation: 2.1-3.6 V with internal 1.8 V and 1.25 V regulators
  - Optional 32.768 kHz crystal for higher timer accuracy
  - Low external component count with single 24 MHz crystal
  - Support for external power amplifier
  - Small 7x7 mm 48-pin VFQFPN and UFQFPN packages or 6x6 mm 40-pin VFQFPN package

Applications

- Smart energy
- Building automation and control
- Home automation and control
- Security and monitoring
- ZigBee® Pro wireless sensor networking
- RF4CE products and remote controls

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1 Description

The STM32W108xx is a fully integrated system-on-chip that integrates a 2.4 GHz, IEEE 802.15.4-compliant transceiver, 32-bit ARM® Cortex®-M3 microprocessor, Flash and RAM memory, and peripherals of use to designers of 802.15.4-based systems.

The transceiver utilizes an efficient architecture that exceeds the dynamic range requirements imposed by the IEEE 802.15.4-2003 standard by over 15 dB. The integrated receive channel filtering allows for robust co-existence with other communication standards in the 2.4 GHz spectrum, such as IEEE 802.11 and Bluetooth. The integrated regulator, VCO, loop filter, and power amplifier keep the external component count low. An optional high performance radio mode (boost mode) is software-selectable to boost dynamic range.

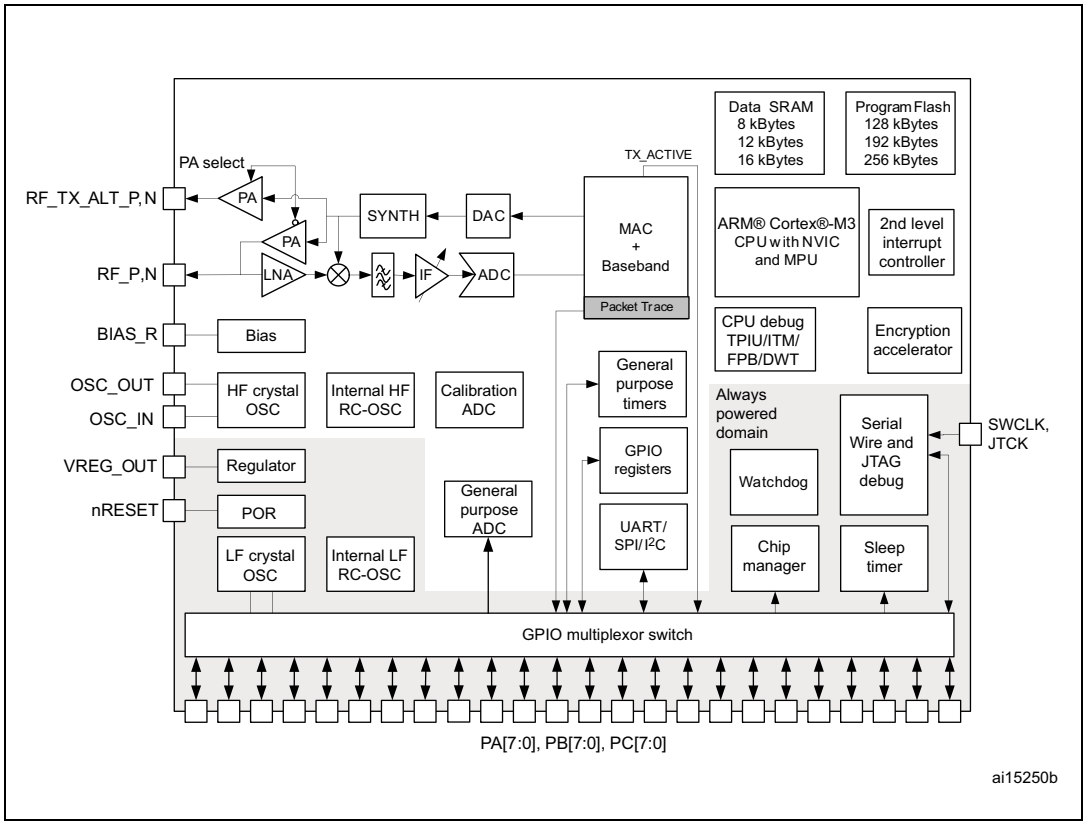
The integrated 32-bit ARM® Cortex®-M3 microprocessor is highly optimized for high performance, low power consumption, and efficient memory utilization. Including an integrated MPU, it supports two different modes of operation: Privileged mode and Unprivileged mode. This architecture could be used to separate the networking stack from the application code and prevent unwanted modification of restricted areas of memory and registers resulting in increased stability and reliability of deployed solutions.

The STM32W108xx has 128/192/256 Kbyte of embedded Flash memory and 8/12/16 Kbyte of integrated RAM for data and program storage. The STM32W108xx HAL software employs an effective wear-leveling algorithm that optimizes the lifetime of the embedded Flash.

To maintain the strict timing requirements imposed by the ZigBee and IEEE 802.15.4-2003 standards, the STM32W108xx integrates a number of MAC functions into the hardware. The MAC hardware handles automatic ACK transmission and reception, automatic backoff delay, and clear channel assessment for transmission, as well as automatic filtering of received packets. A packet trace interface is also integrated with the MAC, allowing complete, non-intrusive capture of all packets to and from the STM32W108xx.

The STM32W108xx offers a number of advanced power management features that enable long battery life. A high-frequency internal RC oscillator allows the processor core to begin code execution quickly upon waking. Various deep sleep modes are available with less than 1 µA power consumption while retaining RAM contents. To support user-defined applications, on-chip peripherals include UART, SPI, I^2C, ADC and general-purpose timers, as well as up to 24 GPIOs. Additionally, an integrated voltage regulator, power-on-reset circuit, and sleep timer are available.

Figure 1. STM32W108xx block diagram



1.1 Development tools

The STM32W108xx implements both the ARM Serial Wire and JTAG debug interfaces. These interfaces provide real time, non-intrusive programming and debugging capabilities. Serial Wire and JTAG provide the same functionality, but are mutually exclusive. The Serial Wire interface uses two pins; the JTAG interface uses five. Serial Wire is preferred, since it uses fewer pins.

The STM32W108xx also integrates the standard ARM system debug components: Flash Patch and Breakpoint (FPB), Data Watchpoint and Trace (DWT), and Instrumentation Trace Macrocell (DWT).

1.2 Overview

1.2.1 Functional description

The STM32W108xx radio receiver is a low-IF, super-heterodyne receiver. The architecture has been chosen to optimize co-existence with other devices in the 2.4 GHz band (namely, WIFI and Bluetooth), and to minimize power consumption. The receiver uses differential signal paths to reduce sensitivity to noise interference. Following RF amplification, the signal is downconverted by an image-rejecting mixer, filtered, and then digitized by an ADC.

The radio transmitter uses an efficient architecture in which the data stream directly modulates the VCO frequency. An integrated power amplifier (PA) provides the output power. Digital logic controls Tx path and output power calibration. If the STM32W108xx is to be used with an external PA, use the TX_ACTIVE or nTX_ACTIVE signal to control the timing of the external switching logic.

The integrated 4.8 GHz VCO and loop filter minimize off-chip circuitry. Only a 24 MHz crystal with its loading capacitors is required to establish the PLL local oscillator signal.

The MAC interfaces the on-chip RAM to the Rx and Tx baseband modules. The MAC provides hardware-based IEEE 802.15.4 packet-level filtering. It supplies an accurate symbol time base that minimizes the synchronization effort of the software stack and meets the protocol timing requirements. In addition, it provides timer and synchronization assistance for the IEEE 802.15.4 CSMA-CA algorithm.

The STM32W108xx integrates an ARM® Cortex®-M3 microprocessor, revision r1p1. This industry-leading core provides 32 bit performance and is very power efficient. It has excellent code density using the ARM® Thumb 2 instruction set. The processor can be operated at 12 MHz or 24 MHz when using the crystal oscillator, or at 6 MHz or 12 MHz when using the integrated high frequency RC oscillator.

The STM32W108xx has 128/192/256 Kbyte of Flash memory, 8/12/16 Kbyte of SRAM on-chip, and the ARM configurable memory protection unit (MPU).

The STM32W108xx contains 24 GPIO pins shared with other peripheral or alternate functions. Because of flexible routing within the STM32W108xx, external devices can use the alternate functions on a variety of different GPIOs. The integrated Serial Controller SC1 can be configured for SPI (master or slave), I^2C (master-only), or UART operation, and the Serial Controller SC2 can be configured for SPI (master or slave) or I^2C (master-only) operation.

The STM32W108xx has a general purpose ADC which can sample analog signals from six GPIO pins in single-ended or differential modes. It can also sample the regulated supply VDD_PADSA, the voltage reference VREF, and GND. The ADC has two selectable voltage ranges: 0 V to 1.2 V for the low voltage (input buffer disabled) and 0.1 V to VDD_PADS minus 0.1 V for the high voltage supply (input buffer enabled). The ADC has a DMA mode to capture samples and automatically transfer them into RAM. The integrated voltage reference for the ADC, VREF, can be made available to external circuitry. An external voltage reference can also be driven into the ADC.

The STM32W108xx contains four oscillators: a high frequency 24 MHz external crystal oscillator (24 MHz HSE OSC), a high frequency 12 MHz internal RC oscillator (12 MHz HSI RC), an optional low frequency 32.768 kHz external crystal oscillator (32 kHz HSE OSC), and a 10 kHz internal RC oscillator (10 kHz LSI RC).

The STM32W108xx has an ultra low power, deep sleep state with a choice of clocking modes. The sleep timer can be clocked with either the external 32.768 kHz crystal oscillator or with a 1 kHz clock derived from the internal 10 kHz LSI RC oscillator. Alternatively, all clocks can be disabled for the lowest power mode. In the lowest power mode, only external events on GPIO pins will wake up the chip. The STM32W108xx has a fast startup time (typically 100 µs) from deep sleep to the execution of the first ARM® Cortex®-M3 instruction.

The STM32W108xx contains three power domains. The always-on high voltage supply powers the GPIO pads and critical chip functions. Regulated low voltage supplies power the rest of the chip. The low voltage supplies are be disabled during deep sleep to reduce power consumption. Integrated voltage regulators generate regulated 1.25 V and 1.8 V voltages from an unregulated supply voltage. The 1.8 V regulator output is decoupled and routed externally to supply analog blocks, RAM, and Flash memories. The 1.25 V regulator output is decoupled externally and supplies the core logic.

The digital section of the receiver uses a coherent demodulator to generate symbols for the hardware-based MAC. The digital receiver also contains the analog radio calibration routines and controls the gain within the receiver path.

In addition to 2 general-purpose timers, the STM32W108xx also contains a watchdog timer to ensure protection against software crashes and CPU lockup, a 32-bit sleep timer dedicated to system timing and waking from sleep at specific times and an ARM® standard system event timer in the NVIC.

The STM32W108xx integrates hardware support for a Packet Trace module, which allows robust packet-based debug.

Note: The STM32W108xx is not pin-compatible with the previous generation chip, the SN250, except for the RF section of the chip. Pins 1-11 and 45-48 are compatible, to ease migration to the STM32W108xx.

1.2.2 ARM® Cortex®-M3 core

The STM32W108xx integrates the ARM® Cortex®-M3 microprocessor, revision r1p1, developed by ARM Ltd, making the STM32W108xx a true system-on-a-chip solution. The ARM® Cortex®-M3 is an advanced 32-bit modified Harvard architecture processor that has separate internal program and data buses, but presents a unified program and data address space to software. The word width is 32 bits for both the program and data sides. The ARM® Cortex®-M3 allows unaligned word and half-word data accesses to support efficiently-packed data structures.

The ARM® Cortex®-M3 clock speed is configurable to 6 MHz, 12 MHz, or 24 MHz. For normal operation 12 MHz is preferred over 24 MHz due to its lower power consumption. The 6 MHz operation can only be used when radio operations are not required since the radio requires an accurate 12 MHz clock.

The ARM® Cortex®-M3 in the STM32W108xx has also been enhanced to support two separate memory protection levels. Basic protection is available without using the MPU, but the usual operation uses the MPU. The MPU protects unimplemented areas of the memory map to prevent common software bugs from interfering with software operation. The architecture could also separate the networking stack from the application code using a fine granularity RAM protection module. Errant writes are captured and details are reported to the developer to assist in tracking down and fixing issues.

2 Documentation conventions

Table 1. Description of abbreviations used for bit field access

Abbreviation	Description(1)
Read/Write (rw)	Software can read and write to these bits.
Read-only (r)	Software can only read these bits.
Write only (w)	Software can only write to this bit. Reading returns the reset value.
Read/Write in (MPU) Privileged mode only (rws)	Software can read and write to these bits only in Privileged mode. For more information, please refer to *RAM memory protection on page 37* and *Memory protection unit on page 42*.

1. The conditions under which the hardware (core) sets or clears this field are explained in details in the bit field description, as well as the events that may be generated by writing to the bit.

3 Pinout and pin description

Figure 2. 48-pin VFQFPN pinout

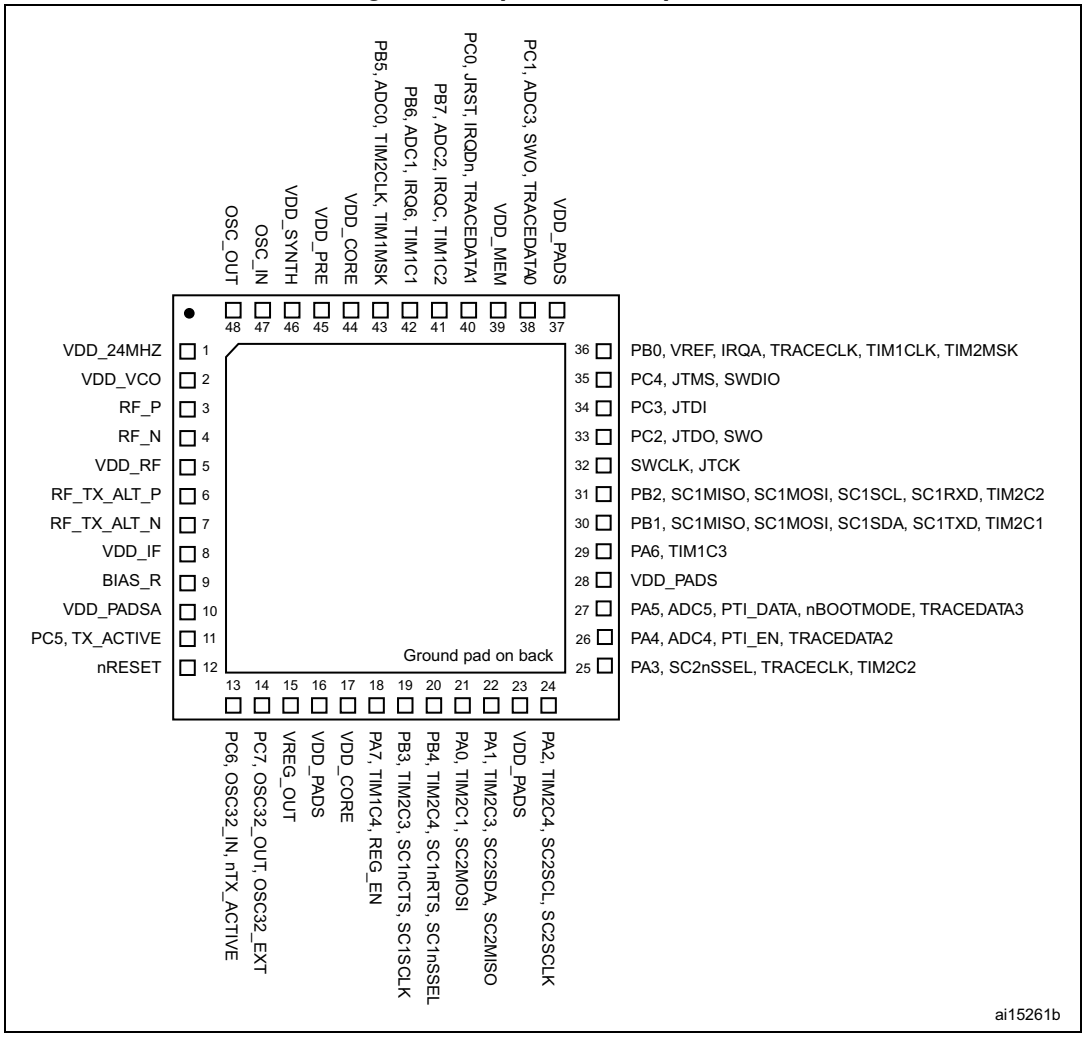


Figure 3. 40-pin VFQFPN pinout

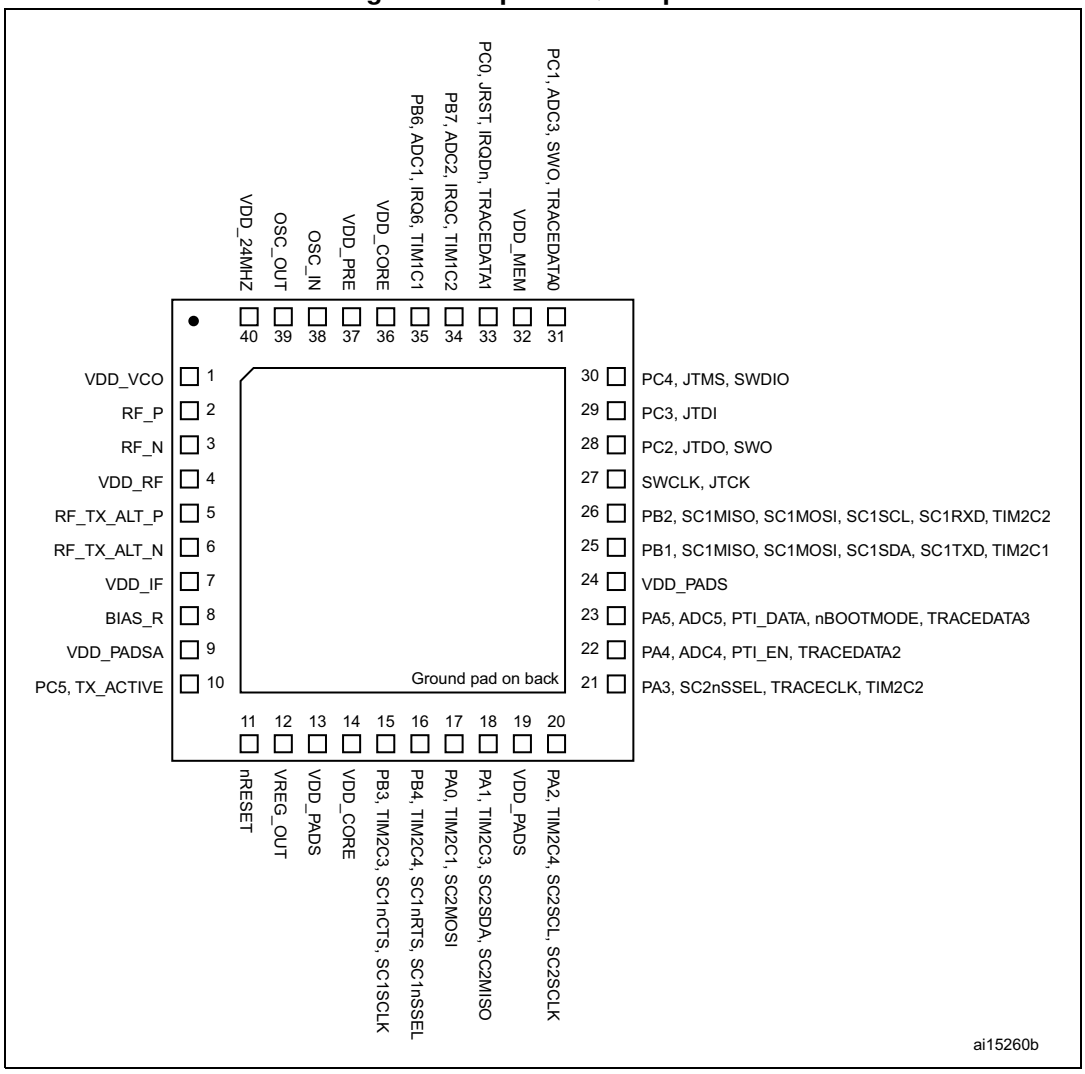


Table 2. Pin descriptions

48-Pin Package Pin no.	40-Pin Package Pin no.	Signal	Direction	Description
1	40	VDD_24MHZ	Power	1.8V high-frequency oscillator supply
2	1	VDD_VCO	Power	1.8V VCO supply
3	2	RF_P	I/O	Differential (with RF_N) receiver input/transmitter output
4	3	RF_N	I/O	Differential (with RF_P) receiver input/transmitter output
5	4	VDD_RF	Power	1.8V RF supply (LNA and PA)
6	5	RF_TX_ALT_P	O	Differential (with RF_TX_ALT_N) transmitter output (optional)
7	6	RF_TX_ALT_N	O	Differential (with RF_TX_ALT_P) transmitter output (optional)
8	7	VDD_IF	Power	1.8V IF supply (mixers and filters)
9	8	BIAS_R	I	Bias setting resistor

Table 2. Pin descriptions (continued)

48-Pin Package Pin no.	40-Pin Package Pin no.	Signal	Direction	Description
10	9	VDD_PADSA	Power	Analog pad supply (1.8V)
11	10	PC5	I/O	Digital I/O
		TX_ACTIVE	O	Logic-level control for external Rx/Tx switch. The STM32W108xx baseband controls TX_ACTIVE and drives it high (VDD_PADS) when in Tx mode. Select alternate output function with GPIOC_CRH[7:4]
12	11	nRESET	I	Active low chip reset (internal pull-up)
13		PC6	I/O	Digital I/O
		OSC32_IN	I/O	32.768 kHz crystal oscillator Select analog function with GPIOC_CRH[11:8]
		nTX_ACTIVE	O	Inverted TX_ACTIVE signal (see PC5) Select alternate output function with GPIOC_CRH[11:8]
14		PC7	I/O	Digital I/O
		OSC32_OUT	I/O	32.768 kHz crystal oscillator. Select analog function with GPIOC_CRH[15:12]
		OSC32_EXT	I	Digital 32 kHz clock input source
15	12	VREG_OUT	Power	Regulator output (1.8 V while awake, 0 V during deep sleep)
16	13	VDD_PADS	Power	Pads supply (2.1-3.6 V)
17	14	VDD_CORE	Power	1.25 V digital core supply decoupling
18		PA7	I/O High current	Digital I/O. Disable REG_EN with GPIO_DBGCR[4]
		TIM1_CH4	O	Timer 1 Channel 4 output Enable timer output with TIM1_CCER Select alternate output function with GPIOA_CRH[15:12] Disable REG_EN with GPIO_DBGCR[4]
			I	Timer 1 Channel 4 input. (Cannot be remapped.)
		REG_EN	O	External regulator open drain output. (Enabled after reset.)

Table 2. Pin descriptions (continued)

48-Pin Package Pin no.	40-Pin Package Pin no.	Signal	Direction	Description
19	15	PB3	I/O	Digital I/O
		TIM2_CH3 (see Pin 22)	O	Timer 2 channel 3 output Enable remap with TIM2_OR[6] Enable timer output in TIM2_CCER Select alternate output function with GPIOB_CRL[15:12]
			I	Timer 2 channel 3 input. Enable remap with TIM2_OR[6].
		UART_CTS	I	UART CTS handshake of Serial Controller 1 Enable with SC1_UARTCR[5] Select UART with SC1_CR
		SC1SCLK	O	SPI master clock of Serial Controller 1 Either disable timer output in TIM2_CCER or disable remap with TIM2_OR[6] Enable master with SC1_SPICR[4] Select SPI with SC1_CR Select alternate output function with GPIOB_CRL[15:12]
			I	SPI slave clock of Serial Controller 1 Enable slave with SC1_SPICR[4] Select SPI with SC1_CR
20	16	PB4	I/O	Digital I/O
		TIM2_CH4 (see also Pin 24)	O	Timer 2 channel 4 output Enable remap with TIM2_OR[7] Enable timer output in TIM2_CCER Select alternate output function with GPIOB_CRH[3:0]
			I	Timer 2 channel 4 input. Enable remap with TIM2_OR[7].
		UART_RTS	O	UART RTS handshake of Serial Controller 1 Either disable timer output in TIM2_CCER or disable remap with TIM2_OR[7] Enable with SC1_UARTCR[5] Select UART with SC1_CR Select alternate output function with GPIOB_CRH[3:0]
		SC1nSSEL	I	SPI slave select of Serial Controller 1 Enable slave with SC1_SPICR[4] Select SPI with SC1_CR

Table 2. Pin descriptions (continued)

48-Pin Package Pin no.	40-Pin Package Pin no.	Signal	Direction	Description
21	17	PA0	I/O	Digital I/O
		TIM2_CH1 (see also Pin 30)	O	Timer 2 channel 1 output Disable remap with TIM2_OR[4] Enable timer output in TIM2_CCER Select alternate output function with GPIOA_CRL[3:0]
			I	Timer 2 channel 1 input. Disable remap with TIM2_OR[4].
		SC2MOSI	O	SPI master data out of Serial Controller 2 Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[4] Enable master with SC2_SPICR[4] Select SPI with SC2_CR Select alternate output function with GPIOA_CRL[3:0]
			I	SPI slave data in of Serial Controller 2 Enable slave with SC2_SPICR[4] Select SPI with SC2_CR
22	18	PA1	I/O	Digital I/O
		TIM2_CH3 (see also Pin 19)	O	Timer 2 channel 3 output Disable remap with TIM2_OR[6] Enable timer output in TIM2_CCER Select alternate output function with GPIOA_CRL[7:4]
			I	Timer 2 channel 3 input. Disable remap with TIM2_OR[6].
		SC2SDA	I/O	I^2C data of Serial Controller 2 Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[6] Select I^2C with SC2_CR Select alternate open-drain output function with GPIOA_CRL[7:4]
		SC2MISO	O	SPI slave data out of Serial Controller 2 Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[6] Enable slave with SC2_SPICR[4] Select SPI with SC2_CR Select alternate output function with GPIOA_CRL[7:4]
			I	SPI master data in of Serial Controller 2 Enable slave with SC2_SPICR[4] Select SPI with SC2_CR
23	19	VDD_PADS	Power	Pads supply (2.1-3.6V)

Table 2. Pin descriptions (continued)

48-Pin Package Pin no.	40-Pin Package Pin no.	Signal	Direction	Description
24	20	PA2	I/O	Digital I/O
		TIM2_CH4 (see also Pin 20)	O	Timer 2 channel 4 output Disable remap with TIM2_OR[7] Enable timer output in TIM2_CCER Select alternate output function with GPIOA_CRL[11:8]
			I	Timer 2 channel 4 input. Disable remap with TIM2_OR[7].
		SC2SCL	I/O	I^2C clock of Serial Controller 2 Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[7] Select I^2C with SC2_CR Select alternate open-drain output function with GPIOA_CRL[11:8]
		SC2SCLK	O	SPI master clock of Serial Controller 2 Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[7] Enable master with SC2_SPICR[4] Select SPI with SC2_CR Select alternate output function with GPIOA_CRL[11:8]
			I	SPI slave clock of Serial Controller 2 Enable slave with SC2_SPICR[4] Select SPI with SC2_CR
25	21	PA3	I/O	Digital I/O
		SC2nSSEL	I	SPI slave select of Serial Controller 2 Enable slave with SC2_SPICR[4] Select SPI with SC2_CR
		TRACECLK (see also Pin 36)	O	Synchronous CPU trace clock Either disable timer output in TIM2_CCER or enable remap with TIM2_OR[5] Enable trace interface in ARM core Select alternate output function with GPIOA_CRL[15:12]
		TIM2_CH2 (see also Pin 31)	O	Timer 2 channel 2 output Disable remap with TIM2_OR[5] Enable timer output in TIM2_CCER Select alternate output function with GPIOA_CRL[15:12]
			I	Timer 2 channel 2 input. Disable remap with TIM2_OR[5].

Table 2. Pin descriptions (continued)

48-Pin Package Pin no.	40-Pin Package Pin no.	Signal	Direction	Description
26	22	PA4	I/O	Digital I/O
		ADC4	Analog	ADC Input 4. Select analog function with GPIOA_CRH[3:0].
		PTI_EN	O	Frame signal of Packet Trace Interface (PTI). Disable trace interface in ARM core. Select alternate output function with GPIOA_CRH[3:0].
		TRACEDATA2	O	Synchronous CPU trace data bit 2. Select 4-wire synchronous trace interface in ARM core. Enable trace interface in ARM core. Select alternate output function with GPIOA_CRH[3:0].
27	23	PA5	I/O	Digital I/O
		ADC5	Analog	ADC Input 5. Select analog function with GPIOA_CRH[7:4].
		PTI_DATA	O	Data signal of Packet Trace Interface (PTI). Disable trace interface in ARM core. Select alternate output function with GPIOA_CRH[7:4].
		nBOOTMODE	I	Embedded serial bootloader activation out of reset. Signal is active during and immediately after a reset on NRST. See *Section 6.2: Resets on page 48* for details.
		TRACEDATA3	O	Synchronous CPU trace data bit 3. Select 4-wire synchronous trace interface in ARM core. Enable trace interface in ARM core. Select alternate output function with GPIOA_CRH[7:4]
28	24	VDD_PADS	Power	Pads supply (2.1-3.6 V)
29		PA6	I/O High current	Digital I/O
		TIM1_CH3	O	Timer 1 channel 3 output Enable timer output in TIM1_CCER Select alternate output function with GPIOA_CRH[11:8]
			I	Timer 1 channel 3 input (Cannot be remapped.)