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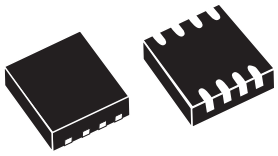
STM6502, STM6503
STM6504, STM6505

Dual push-button Smart Reset™ with user-adjustable setup delays

Features

- Dual Smart Reset push-button inputs with extended reset setup delay
- Adjustable Smart Reset setup delay (t_{SRC}): by external capacitor or three-state logic (product options): t_{SRC} = 2, 6, 10 s (min.)
- Power-on reset
- Single $\overline{RST}$ output, active-low, open-drain
- Factory-programmable thresholds to monitor V_{CC} in the range of 1.575 to 4.625 V typ.
- Operating voltage 1.0 V (active-low output valid) to 5.5 V
- Low supply current
- Operating temperature: industrial grade –40 °C to +85 °C
- TDFN8 package: 2 mm x 2 mm x 0.75 mm
- RoHS compliant



TDFN8 (DG)
2 mm x 2 mm

Applications

- Mobile phones, smartphones
- e-books
- MP3 players
- Games
- Portable navigation devices
- Any application that requires delayed reset push-button(s) response for improved system stability

Table 1. Device summary

Part number	Voltage inputs		Smart Reset inputs			t_{SRC} programming		Reset or Power Good outputs		Package
	V_{CC}	V_{BAT}	$\overline{SR0}$	$\overline{SR1}$	SRE immediate, independent	Ext. SRC pin	Three-state input TSR	$\overline{RST}$	$\overline{BLD}$	
STM6502[1]	✓		✓	✓		✓		✓		TDFN-8L
STM6503	✓		✓	✓			✓	✓		TDFN-8L
STM6504[1]	✓		✓		✓		✓	✓		TDFN-8L
STM6505	✓	✓	✓	✓		✓		✓	✓	TDFN-8L

1. Contact local ST sales office for availability.

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1 Description

STM6502 has two combined Smart Reset inputs ($\overline{SR0}$ and $\overline{SR1}$) with delayed Smart Reset setup time (t_{SRC}) programmed by an external capacitor on the SRC pin.

STM6503 is similar to STM6502, has two combined delayed Smart Reset inputs ($\overline{SR0}$, $\overline{SR1}$) and three user-selectable delayed Smart Reset setup time (t_{SRC}) options of 2 s, 6 s and 10 s through a three-state TSR input pin: when connected to ground, t_{SRC} = 2 s; when left open, t_{SRC} = 6 s; when connected to V_{CC}, t_{SRC} = 10 s (all the times are minimum).

STM6504 has two independent Smart Reset inputs. $\overline{SR0}$ provides the delayed Smart Reset setup time (t_{SRC}) function with three user-selectable t_{SRC} options through a three-state TSR input pin: when connected to ground, t_{SRC} = 2 s; when left open, t_{SRC} = 6 s; when connected to V_{CC}, t_{SRC} = 10 s (all the times are minimum). SRE provides instant reset. SRE is edge-triggered with a special debounce time ($t_{DEBOUNCE}$ = 240 ms min.) at the falling edge after a valid reset period.

STM6505 has two combined delayed Smart Reset inputs ($\overline{SR0}$, $\overline{SR1}$) and provides an adjustable reset delay setup time via an external capacitor connected to the SRC pin. The $\overline{RST}$ output depends also on the V_{CC} monitoring threshold. STM6505 also provides independent low battery detect ($\overline{BLD}$) output controlled by the secondary external input voltage V_{BAT}. V_{BAT} is monitored for low voltage and provides an indication on the battery low detect output pin ($\overline{BLD}$). V_{BAT} threshold is 1.25 V, fixed, and an external resistor divider is to be used to set the actual battery voltage threshold. V_{BAT} threshold hysteresis is 8 mV typ. (16 mV max.). V_{BAT} is voltage monitoring input only, the device is powered only from the V_{CC} pin; V_{CC} must be ≥ 1.575 V for proper operation of the V_{BAT} comparator.

1.1 Smart Reset devices

The Smart Reset device family STM65xx provides a useful feature that ensures inadvertent short reset push-button closures do not cause system resets. This is done by implementing extended Smart Reset input delay (t_{SRC}). Once the valid Smart Reset input levels and setup delay are met, the device generates an output reset pulse with user-programmable timeout period (t_{REC}).

The Smart Reset inputs can be also connected to the applications interrupt to allow the control of both the interrupt pin and the hard reset functions. If the push-buttons are closed for a short time, the processor is only interrupted. If the system still does not respond properly, holding the push-buttons for the extended setup time (t_{SRC}) causes hard reset of the processor through the reset outputs. The Smart Reset feature helps significantly increase system stability.

The STM65xx family of Smart Reset devices consists of low current microprocessor reset circuits targeted at applications such as MP3 players, navigation, smartphones or mobile phones; generally any application that requires delayed reset push-button(s) response for improved system stability. The STM65xx devices feature single or dual Smart Reset inputs (SR). The delayed Smart Reset setup time (t_{SRC}) options of 2 s, 6 s and 10 s (all min.) are adjustable by an external capacitor on the SRC pin or selectable by three-state logic. The delayed setup period ignores switch closures shorter than t_{SRC}, thus preventing unwanted resets.

The STM65xx devices have active-low (optionally active-high) open-drain reset ($\overline{RST}$) output(s) with or without internal pull-up resistor or push-pull as output options, with factory-programmed or capacitor-adjustable or push-buttons defined output reset pulse duration, with or without power-on reset function.

Some devices also have an undervoltage monitoring feature: the reset output is also asserted when the monitored supply voltage V_{CC} drops below the specified threshold. The reset output remains asserted for the reset timeout period (t_{REC}) after the monitored supply voltage goes above the specified threshold.

Figure 1. Logic diagrams

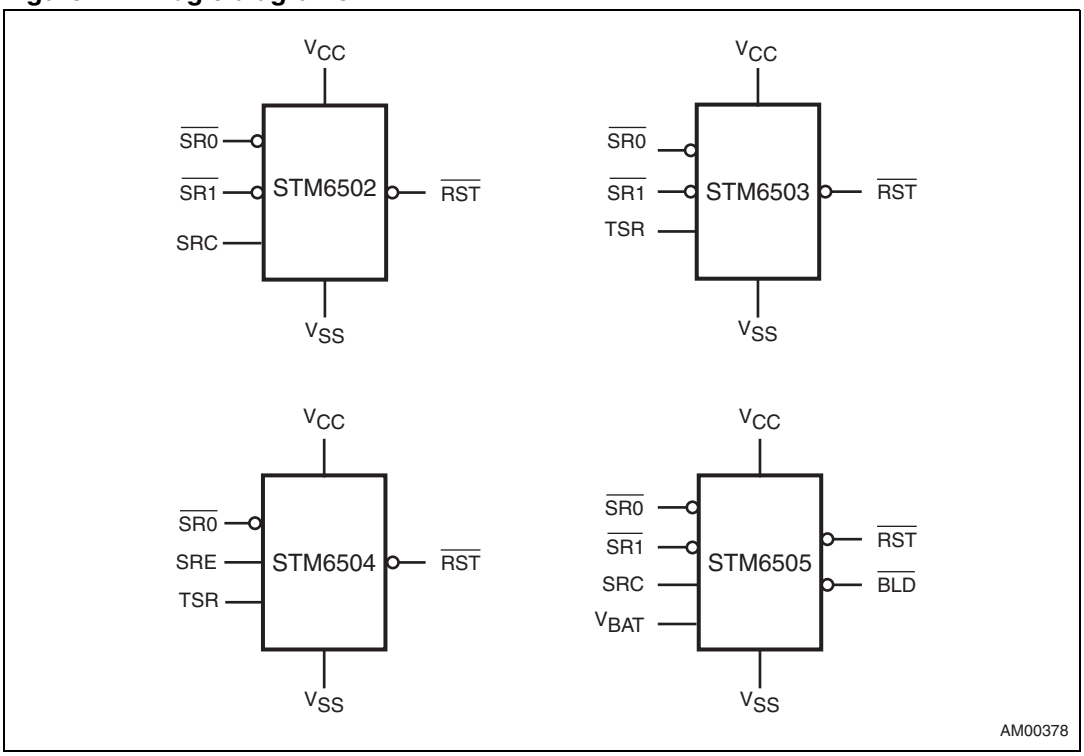


Figure 2. Pin connections

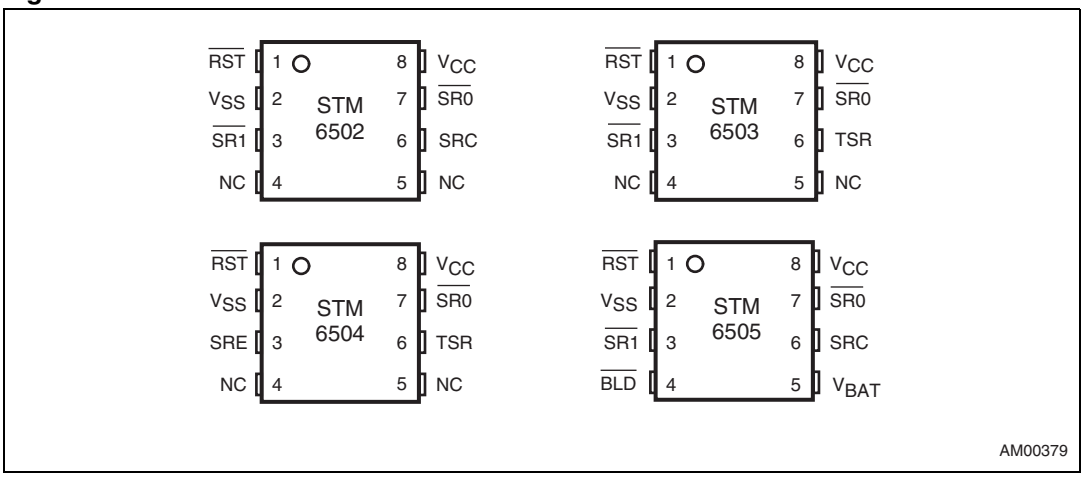
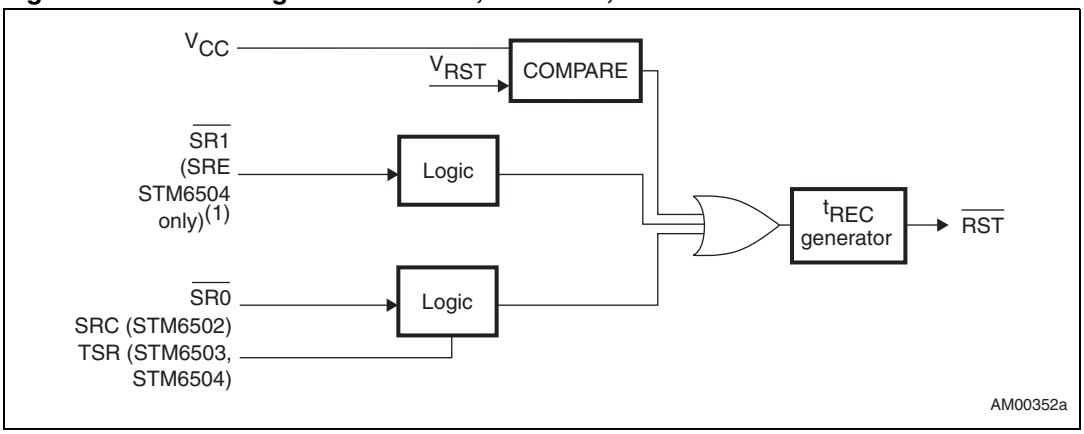


Table 2. Signal names

Symbol	Input/ output	Description
$\overline{RST}$	Output	Open-drain reset output, active-low.
$\overline{BLD}$	Output	Battery low detect output, active-low, open-drain. STM6505 only.
$\overline{SR0}$	Input	Primary push-button Smart Reset input. Active-low, with or without internal 65 kΩ pull-up to V_{CC} (product options).
$\overline{SR1}$	Input	Secondary push-button Smart Reset input - combines with the primary push-button reset to provide setup delay time before reset. Active-low, with or without internal 65 kΩ pull-up to V_{CC} (product options).
SRE	Input	Secondary push-button Smart Reset input - provides instant Smart Reset. SRE is edge-triggered with a special debounce time ($t_{DEBOUNCE}$ = 240 ms min.) at the falling edge after a valid reset period. Active-high, no internal pull-up to V_{CC}. STM6504 only.
SRC	Input	Smart Reset input delay setup control: connect to an external capacitor to adjust the delay setup time (t_{SRC}). STM6502 and STM6505 only.
TSR	Input	A three-state Smart Reset input delay setup control. When connected to ground, t_{SRC} = 2 s; when left open, t_{SRC} = 6 s; when connected to V_{CC}, t_{SRC} = 10 s (all times are minimum). TSR is a DC-type input, intended to be either permanently grounded, permanently connected to V_{CC} or permanently left open. If left open, for improved system glitch immunity it is strongly recommended to connect a 0.1 µF decoupling ceramic capacitor between the TSR and V_{SS} pins. STM6503 and STM6504 only.
V_{CC}	Supply	Supply voltage input. Power supply for the device and an input for the monitored supply voltage. A 0.1 µF decoupling ceramic capacitor is recommended to be connected between the V_{CC} and V_{SS} pins.
V_{BAT}	Input	Battery voltage monitoring input. STM6505 only.
V_{SS}	Supply	Ground
NC		No connect (not bonded); should be connected to V_{SS}.

Figure 3. Block diagram - STM6502, STM6503, STM6504



1. STM6504 only: $\overline{SR0}$ and SRE are working independently. SRE is edge-triggered and has a special debounce time ($t_{DEBOUNCE}$ = 240 ms min.) at the falling edge after a valid reset period.

Figure 4. Block diagram - STM6505

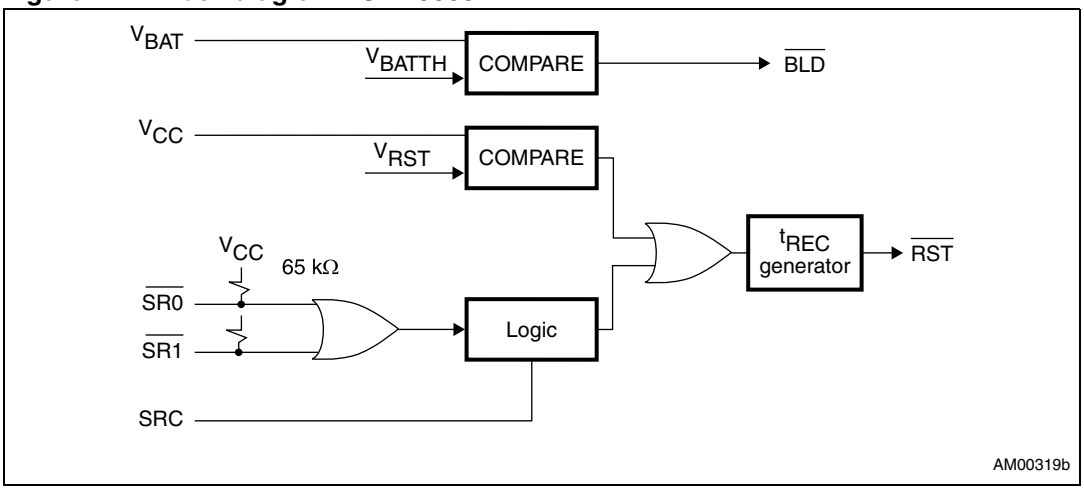


Figure 5. Single-button Smart Reset typical hookup

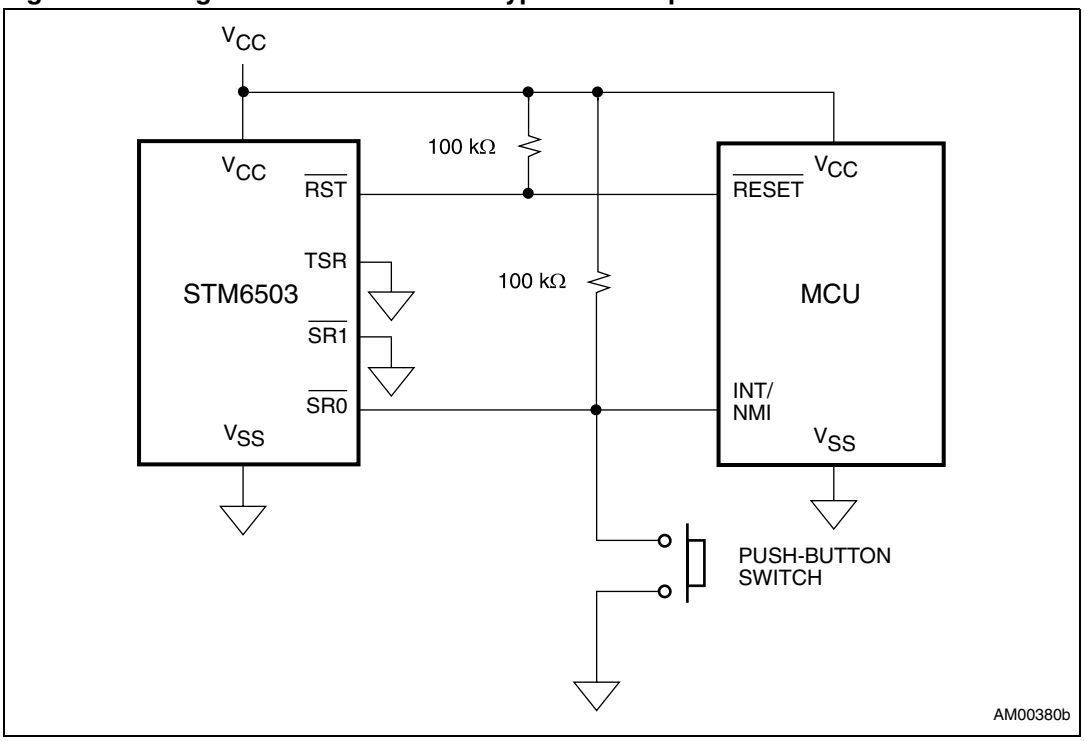
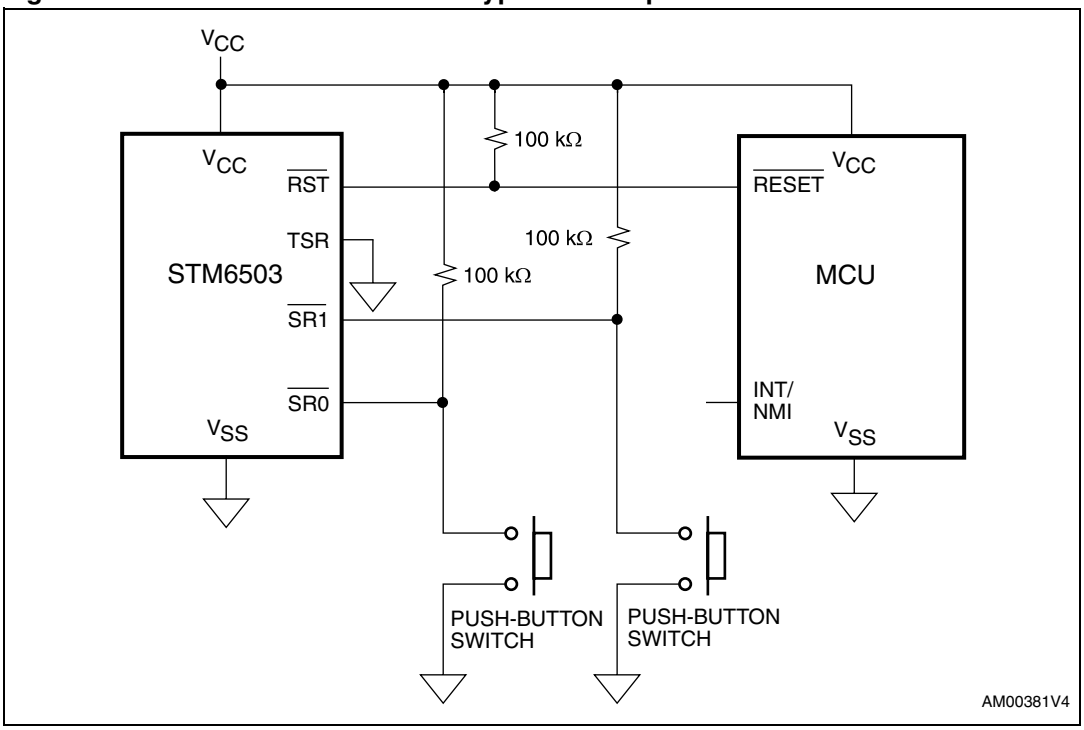


Figure 6. Dual-button Smart Reset typical hookup



1.2 Pin descriptions

1.2.1 Power supply (V_{CC})

This pin is used to provide the power to the device and to monitor the power supply.
A 0.1 µF decoupling ceramic capacitor is recommended to be connected between the V_{CC} and V_{SS} pins.

1.2.2 Ground (V_{SS})

This is the supply ground for the device.

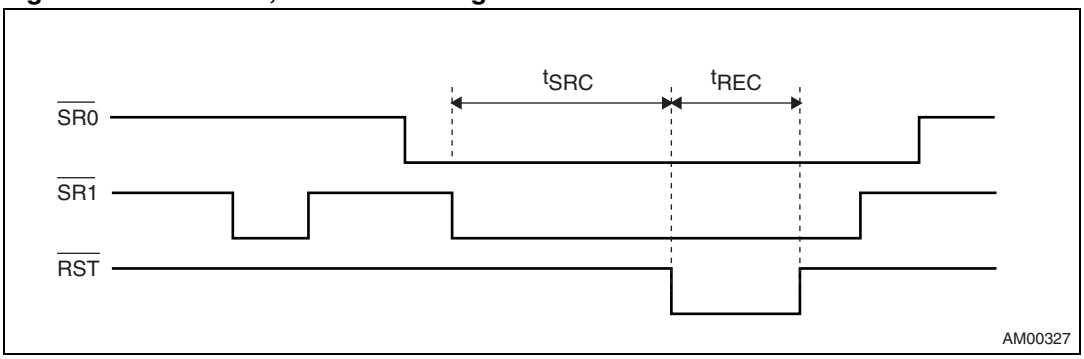
1.2.3 Primary Smart Reset input ($\overline{SR0}$)

The primary push-button Smart Reset input, active-low pin is connected to the first push-button switch.

1.2.4 Secondary Smart Reset input ($\overline{SR1}$)

The secondary push-button Smart Reset input, active-low pin is connected to the second push-button switch. Keeping both Smart Reset inputs $\overline{SR0}$ and $\overline{SR1}$ active for longer than t_{SRC} activates the reset output pulse.

Figure 7. STM6502, STM6503 timing



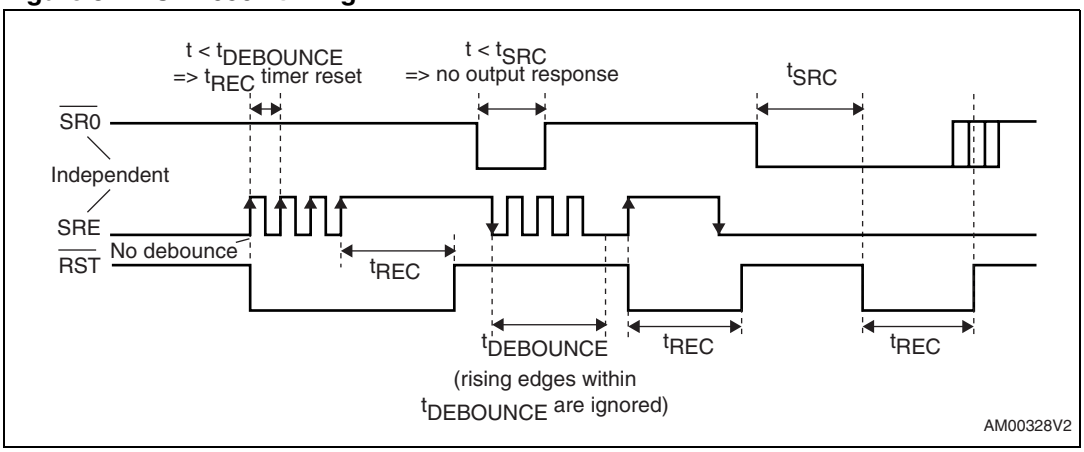
Reset is asserted “low” right after the Smart Reset setup delay (t_{SRC}) has been met and returns to high after the t_{REC} period.

1.2.5 Edge-triggered Smart Reset input (SRE pin) – STM6504 only

The SRE pin is active-high, immediate and independent reset input that includes an edge trigger with debounce delay $t_{DEBOUNCE}$ on the falling edge.

Note: The triggering edge must be a high-to-low or low-to-high transition with a slew-rate faster than 1 V/µs typ.

Figure 8. STM6504 timing



1.2.6 Adjustable delay of Smart Reset input (SRC pin) – STM6502 and STM6505 only

This pin controls the setup time before the push-button action is validated by the reset output. It is connected to an external capacitor (C_{SRC}), which is tied to ground to provide the desired value of the setup time (t_{SRC}).

Calculated t_{SRC} and C_{SRC} examples are given in *Table 3*. Refer also to *Table 6*.

Table 3. t_{SRC} programmed by an ideal external capacitor – STM6502 and STM6505

Calculated C_{SRC} value [µF]	Setup delay t_{SRC} [s](1)(2)			Closest common C_{SRC} value [µF]
	Min.	Typ.	Max.	
0.2	2	2.5	3.0	0.22
0.3	3	3.75	4.5	0.33
0.6	6	7.5	9	0.56
1	10	12.5	15	1

1. At 25 °C. Example calculations based on an ideal capacitor. During application design and component selection it should be considered that the current flowing into the external t_{SRC} programming capacitor (C_{SRC}) is on the order of 100 nA, therefore a low-leakage capacitor (ceramic or film capacitor) should be used and placed as close as possible to the SRC pin. Also an adequate low-leakage PCB environment should be ensured to prevent t_{SRC} accuracy from being affected. A recommended minimum value of C_{SRC} is 0.01 µF.
2. In case of repeated activations of the t_{SRC} timer, an interval of 10 ms min. is needed between the activations to fully discharge C_{SRC}, so that the next t_{SRC} is as specified.

1.2.7 Programmable Smart Reset input delay (TSR pin) – STM6503 and STM6504 only

The TSR pin allows the user to program the setup time before the push-button action is validated by the reset output. It is controlled by different voltage levels on the three-state TSR input pin: when connected to ground, t_{SRC} = 2 s; when left open, t_{SRC} = 6 s; when connected to V_{CC}, t_{SRC} = 10 s (all times are minimum). TSR is a DC-type input, intended to be either permanently grounded, permanently connected to V_{CC} or permanently left open. If it is left open, for improved system glitch immunity it is strongly recommended to connect a 0.1 µF decoupling ceramic capacitor between the TSR and V_{SS} pins.

1.2.8 Reset output ($\overline{RST}$)

$\overline{RST}$ is the active-low, open-drain reset output in the Smart Reset family.

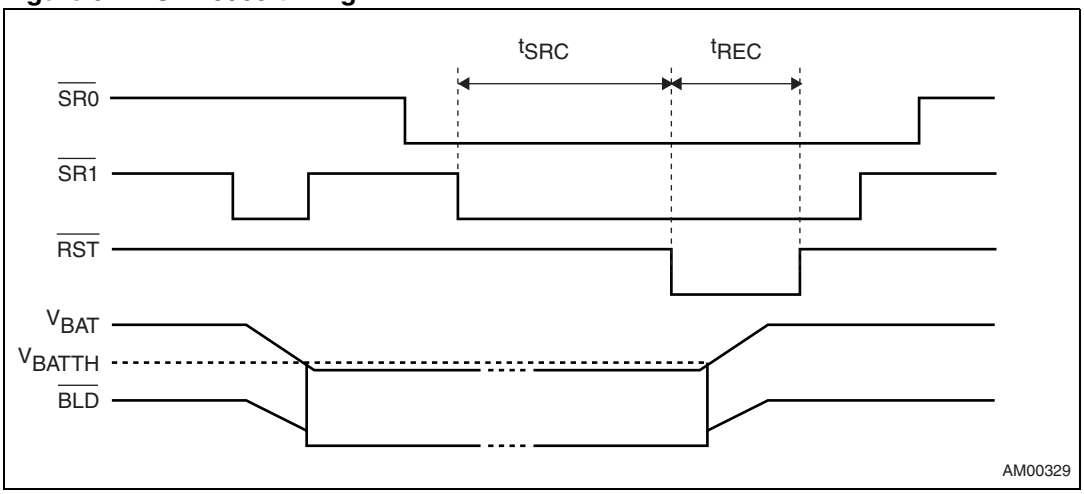
1.2.9 Battery monitoring input (V_{BAT}) – STM6505 only

V_{BAT} is an input for monitoring the battery voltage. V_{BAT} threshold is 1.25 V, fixed, and an external resistor divider is to be used to set the actual battery voltage threshold.

1.2.10 Battery low detect output ($\overline{BLD}$) – STM6505 only

The battery low detect output is controlled by the V_{BAT} voltage monitoring input and is active-low, open-drain, with no pull-up.

Figure 9. STM6505 timing



2 Typical operating characteristics

Figure 10. Supply current (I_{CC}) vs. temperature (STM6505)

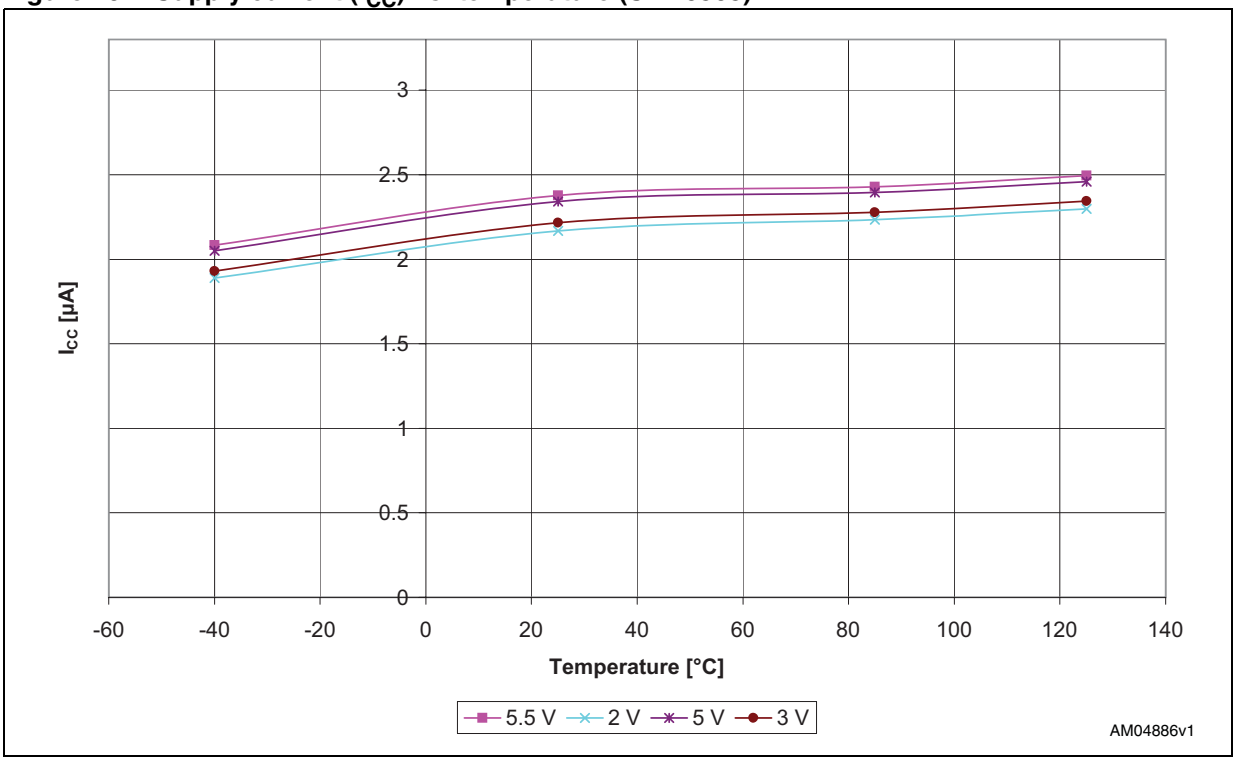


Figure 11. Smart Reset delay (t_{SRC}) vs. temperature, C_{SRC} = 0.62 µF (STM6505)

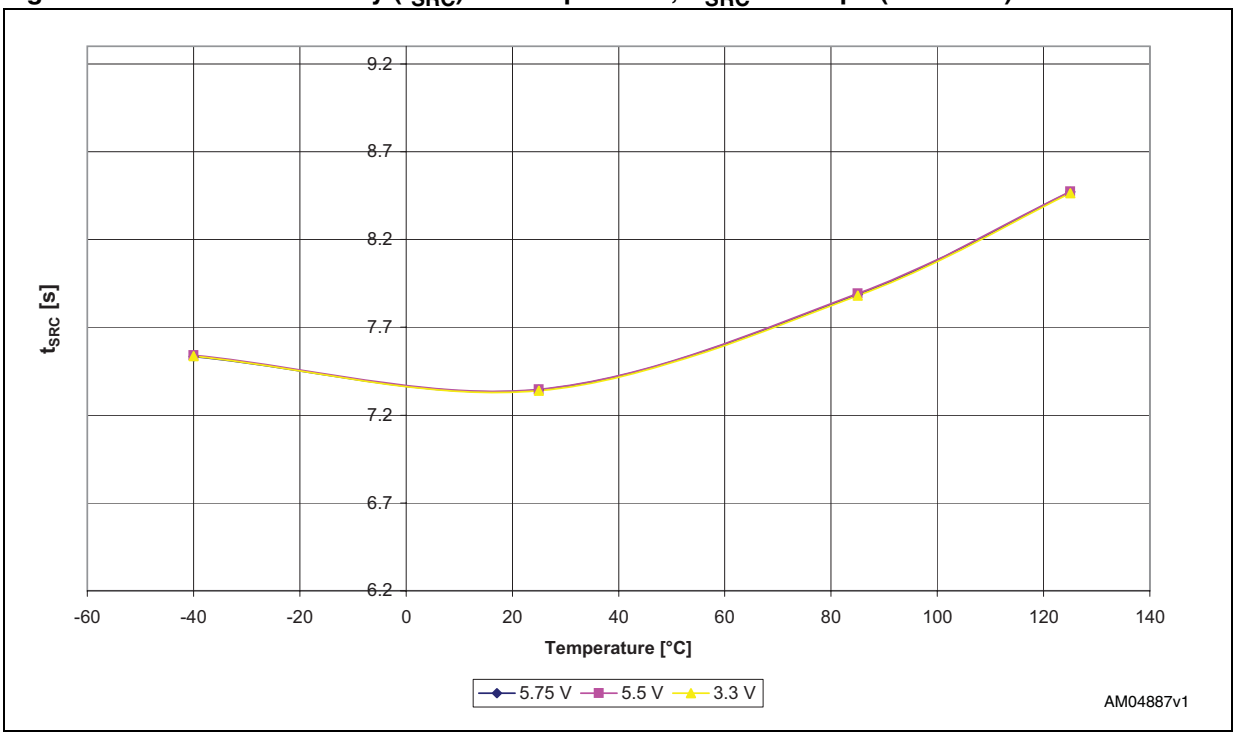


Figure 12. Reset threshold (V_{RST}) vs. temperature, "S" threshold option, V_{CC} falling (STM6505)

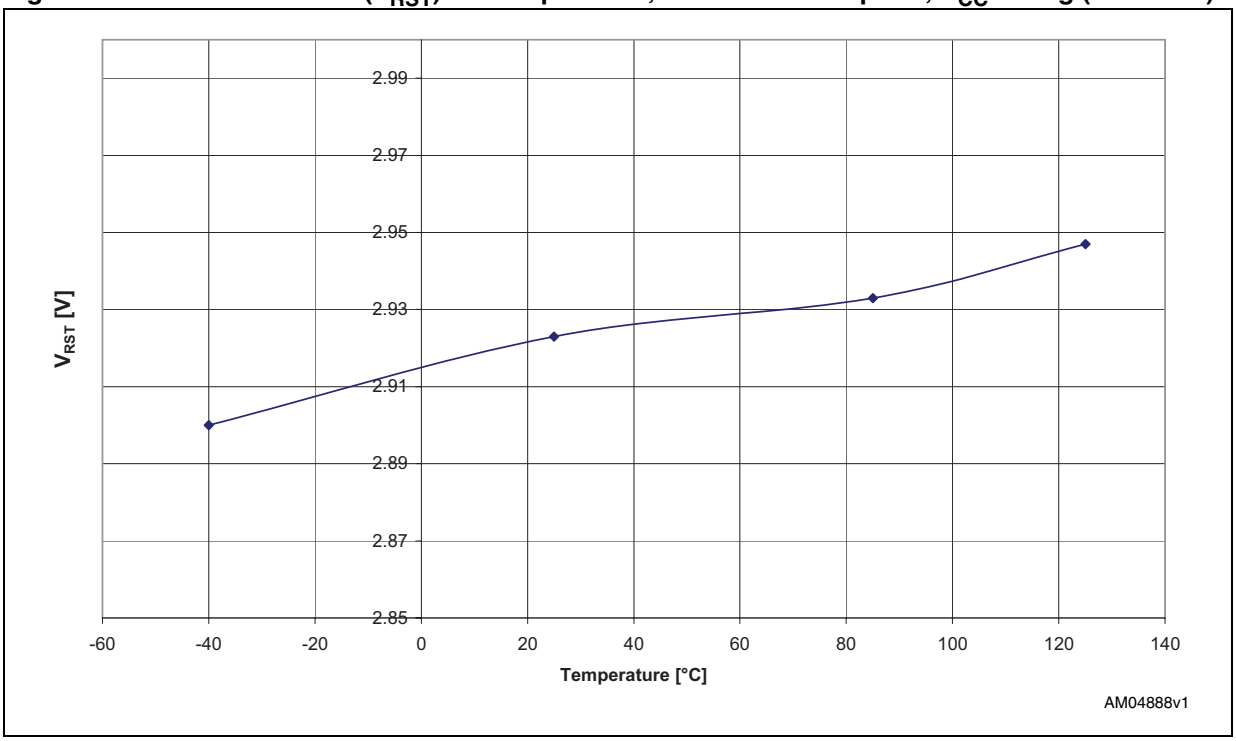
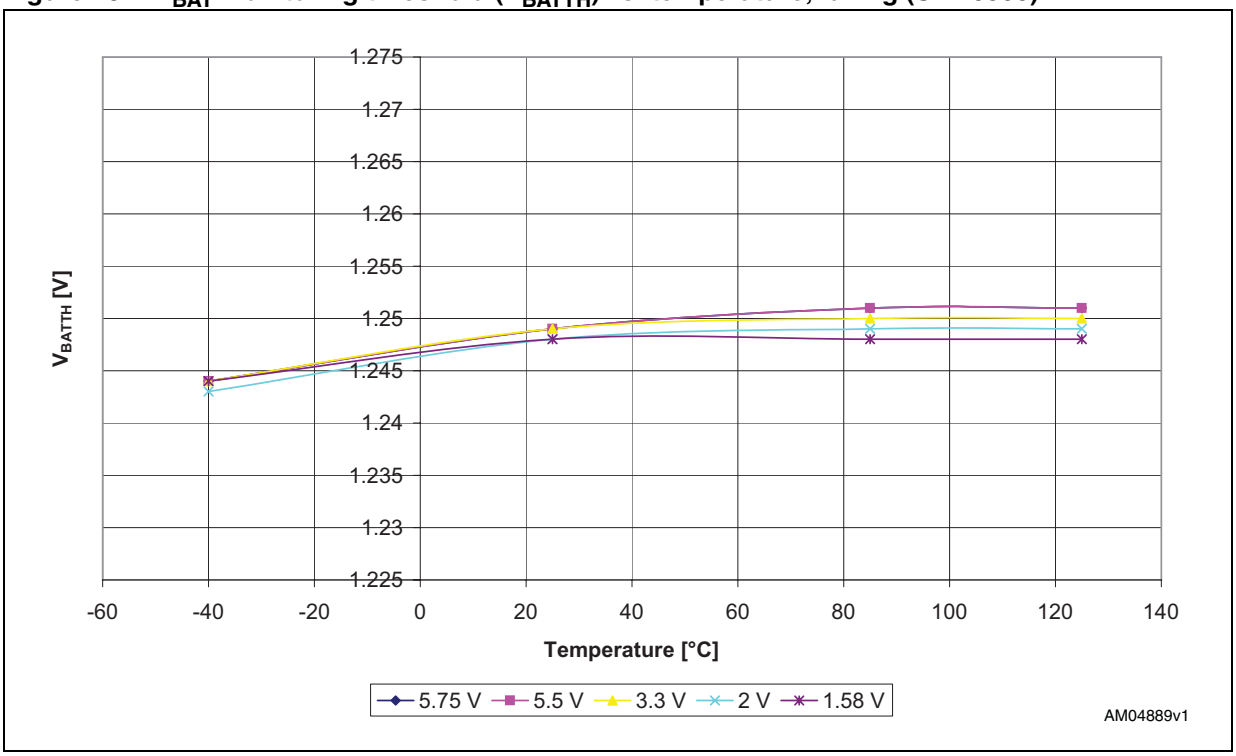


Figure 13. V_{BAT} monitoring threshold (V_{BATTH}) vs. temperature, falling (STM6505)



3 Maximum ratings

Stressing the device above the rating listed in *Table 4: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter		Value	Unit
T_{STG}	Storage temperature (V_{CC} off)		–55 to +150	°C
T_{SLD}(1)	Lead solder temperature for 10 seconds		260	°C
θ_{JA}	Thermal resistance (junction to ambient)	TDFN8	149.0	°C/W
V_{IO}	Input or output voltage		–0.3 to 5.5(2)	V
V_{CC}	Supply voltage		–0.3 to 7	V

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.
2. For inputs or outputs with internal pull-up resistors and push-pull type outputs –0.3 to V_{CC}+0.3 V only.

4 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in *Table 5: Operating and measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 5. Operating and measurement conditions

Parameter	Value	Unit
V_{CC} supply voltage	1.0 to 5.5	V
Ambient operating temperature (T_A)	–40 to +85	°C
Input rise and fall times	≤ 5	ns
Input pulse voltages	0.2 to 0.8 V_{CC}	V
Input and output timing ref. voltages	0.3 to 0.7 V_{CC}	V

Figure 14. AC testing input/output waveforms

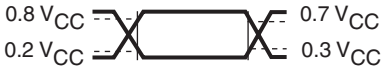


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Table 6. DC and AC characteristics

Symbol	Parameter	Test conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{CC}	Supply voltage range	Reset output valid - active-low		1.0		5.5	V
I_{CC}	Supply current (inputs in their inactive state, t_{REC} and t_{SRC} counter is inactive)	STM6502	V_{CC} = 5.0 V		1.2		µA
			V_{CC} = 3.0 V[3]		1.1		µA
		STM6503	V_{CC} = 5.0 V, TSR left open		4	5.8	µA
			V_{CC} = 3.0 V, TSR left open[3]		3		µA
		STM6504	V_{CC} = 5.0 V, TSR left open		4	5.8	µA
			V_{CC} = 3.0 V, TSR left open[3]		3		µA
		STM6505	V_{CC} = 5.0 V		2.3	3.3	µA
			V_{CC} = 3.0 V[3]		2.2		µA
Output characteristics							
V_{OL}	Reset output voltage low (reset asserted: $\overline{RST}$, $\overline{BLD}$)	$V_{CC} \geq$ 4.5 V, sinking 3.2 mA				0.3	V
		$V_{CC} \geq$ 3.3 V, sinking 2.5 mA				0.3	V
		$V_{CC} \geq$ 1.0 V, sinking 0.1 mA				0.3	V
t_{REC}	Reset timeout delay, factory-programmed	Option A		140	210	280	ms
		Option B		240	360	480	ms
V_{CC} monitoring reset thresholds							
V_{RST}	Fixed voltage trip point for V_{CC} monitoring (refer to *Table 7*)	–40 to +85 °C		V_{RST} –2.5%	V_{RST}	V_{RST} +2.5%	V
		25 °C		V_{RST} –2.0%	V_{RST}	V_{RST} +2.0%	V
V_{HYST}	Hysteresis of V_{RST}	L, M			0.5%		
		T, S, R, Z, Y, W, V			1%		
	V_{CC} to reset delay	V_{CC} falling from (V_{RST} + 100 mV) to (V_{RST} - 100 mV) at 10 mV/µs[4]			20		µs
V_{BAT} monitoring							
V_{BATTH}	Fixed V_{BAT} monitoring threshold	STM6505 only		1.225	1.25	1.275	V
$V_{BATHYST}$	V_{BATTH} hysteresis	STM6505 only			8	16	mV
$I_{LI(VBAT)}$	V_{BAT} input leakage current	STM6505 only		–100	10	100	nA

Table 6. DC and AC characteristics (continued)

Symbol	Parameter	Test conditions(1)	Min.	Typ.(2)	Max.	Unit
Smart Reset inputs						
V_{IL}	$\overline{SR0}$, $\overline{SR1}$, SRE input voltage low		V_{SS} –0.3		0.3 V_{CC}	V
V_{IH}	$\overline{SR0}$, $\overline{SR1}$, SRE input voltage high		0.7 V_{CC}		5.5	V
$I_{LI(SR)}$	Input leakage current, $\overline{SR}$ and SRE inputs	Option without internal pull-up resistor	–1		+1	µA
$I_{LI(TSR)}$	Input leakage current, TSR input	STM6503 and STM6504 only	–5		+7	µA
R_{PUI}	Internal pull-up resistor, input (optional - refer to *Table 12*)			65		kΩ
$t_{DEBOUNCE}$	SRE input falling edge debounce time	STM6504 only	240	360	480	ms
Smart Reset delay						
t_{SRC}(5)	Capacitor-programmable Smart Reset setup time, STM6502 and STM6505. Refer to *Table 3*.	T_A = 25 °C	10 x C_{SRC} (µF)	12.5 x C_{SRC} (µF)	15 x C_{SRC} (µF)	s
t_{SRC}(5)	TSR pin-programmable Smart Reset setup time, STM6503 and STM6504.	TSR = V_{SS}	2	2.5	3	s
		TSR = floating(6)	6	7.5	9	s
		TSR = V_{CC}	10	12.5	15	s

1. Valid for ambient operating temperature: T_A = –40 to +85 °C; V_{CC} = 1.0 to 5.5 V (except where noted).
2. Typical value is at 25 °C and V_{CC} = 3.3 V unless otherwise noted.
3. For devices with V_{RST} < 3.0 V.
4. Guaranteed by design.
5. Input glitch immunity is equal to t_{SRC} (when both $\overline{SR}$ inputs are low, otherwise infinite). STM6502, STM6503, STM6505 only.
6. If left open, for improved system glitch immunity it is strongly recommended to connect a 0.1 µF decoupling ceramic capacitor between the TSR and V_{SS} pins.

Table 7. V_{CC} voltage thresholds

V_{CC} monitoring threshold V_{RST}	Typ.	±2.5% (–40 °C to +85 °C)		±2.0% (25 °C)		Unit
		Min.	Max.	Min.	Max.	
L (falling)	4.625	4.509	4.741	4.533	4.718	V
M (falling)	4.375	4.266	4.484	4.288	4.463	V
T (falling)	3.075	2.998	3.152	3.014	3.137	V
S (falling)	2.925	2.852	2.998	2.867	2.984	V
R (falling)	2.625	2.559	2.691	2.573	2.678	V
Z (falling)	2.313	2.255	2.371	2.267	2.359	V
Y (falling)	2.188	2.133	2.243	2.144	2.232	V
W (falling)	1.665	1.623	1.707	1.632	1.698	V
V (falling)	1.575	1.536	1.614	1.544	1.607	V

5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 15. TDFN – 8-lead 2 x 2 x 0.75 mm, 0.5 mm pitch package outline

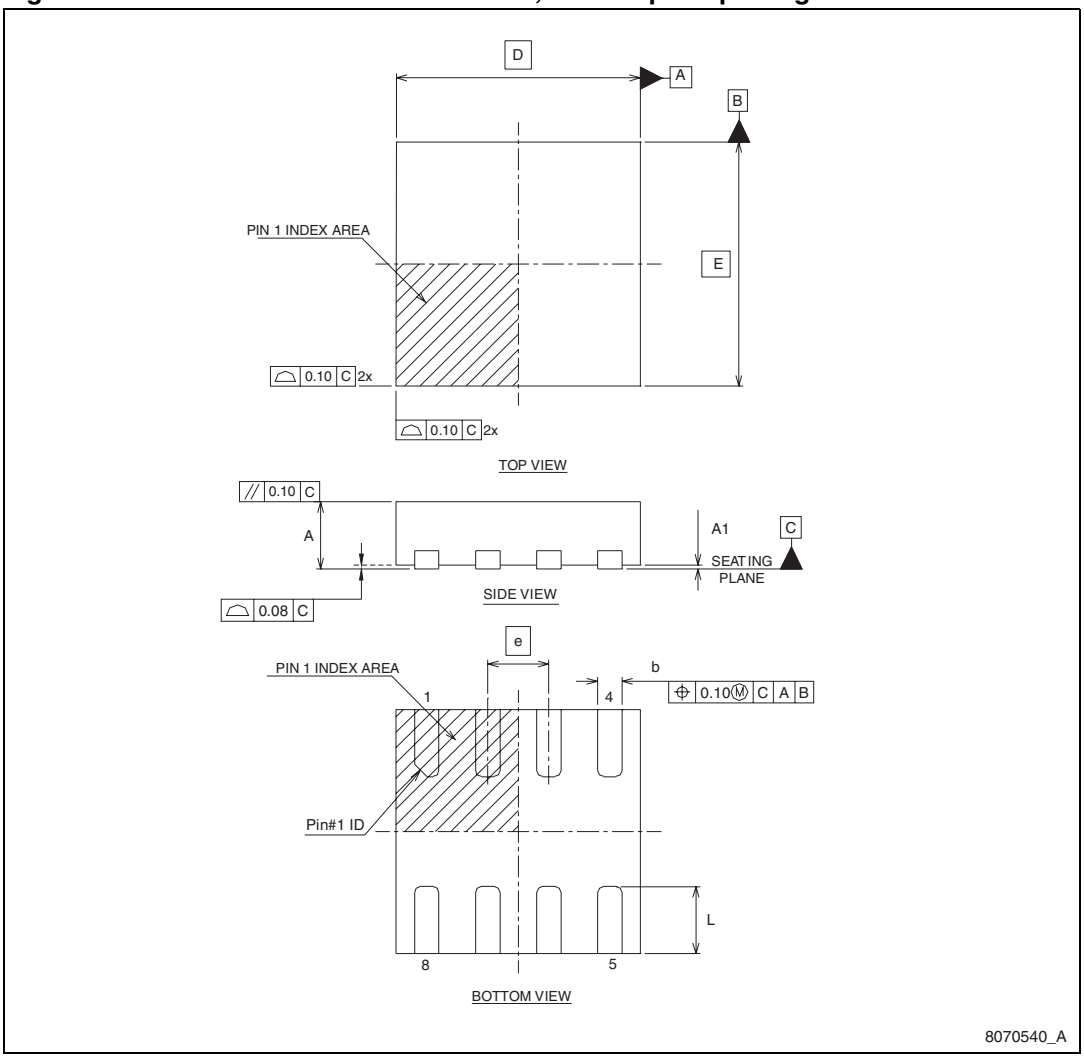


Table 8. TDFN – 8-lead 2 x 2 x 0.75 mm, 0.5 mm pitch package mechanical data

Symbol	Dimension (mm)			Dimension (inches)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D BSC	1.9	2.00	2.1	0.075	0.079	0.083
E BSC	1.9	2.00	2.1	0.075	0.079	0.083
e		0.50			0.020	
L	0.45	0.55	0.65	0.018	0.022	0.026

Figure 16. Landing pattern - TDFN – 8-lead 2 x 2 mm without thermal pad

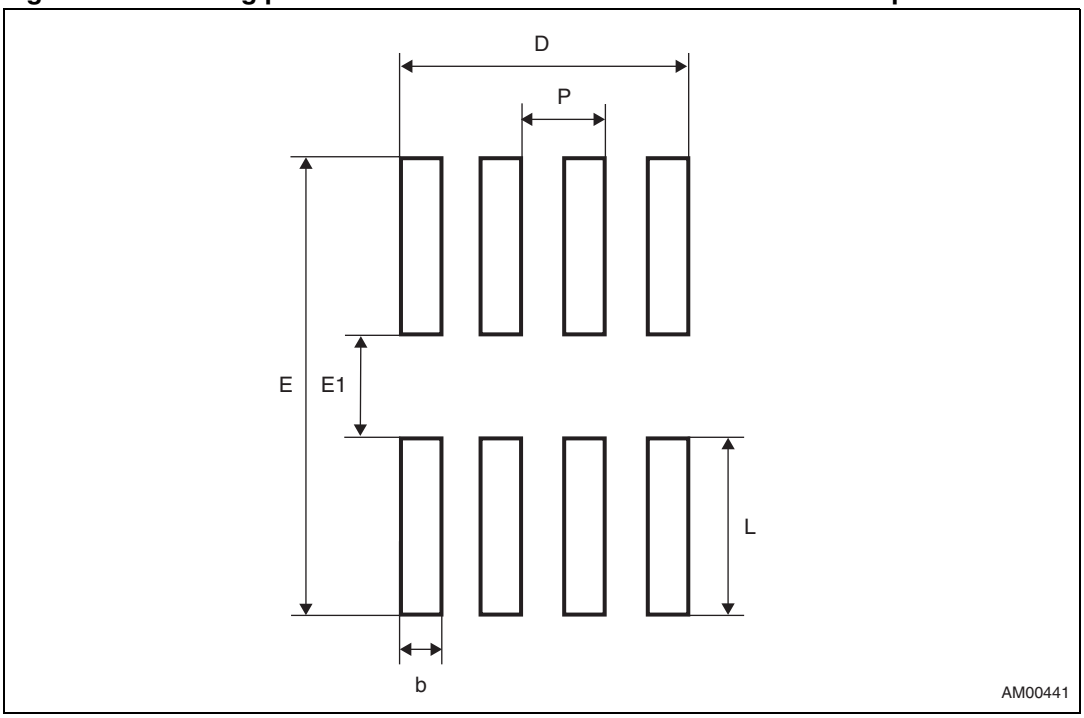


Table 9. Parameter for landing pattern - TDFN – 8-lead 2 x 2 mm package

Parameter	Description	Dimension (mm)		
		Min.	Nom.	Max.
L	Contact length	1.05	—	1.15
b	Contact width	0.25	—	0.30
E	Max. land pattern Y-direction	—	2.85	—
E1	Contact gap spacing	—	0.65	—
D	Max. land pattern X-direction	—	1.75	—
P	Contact pitch	—	0.5	—

Figure 17. Carrier tape

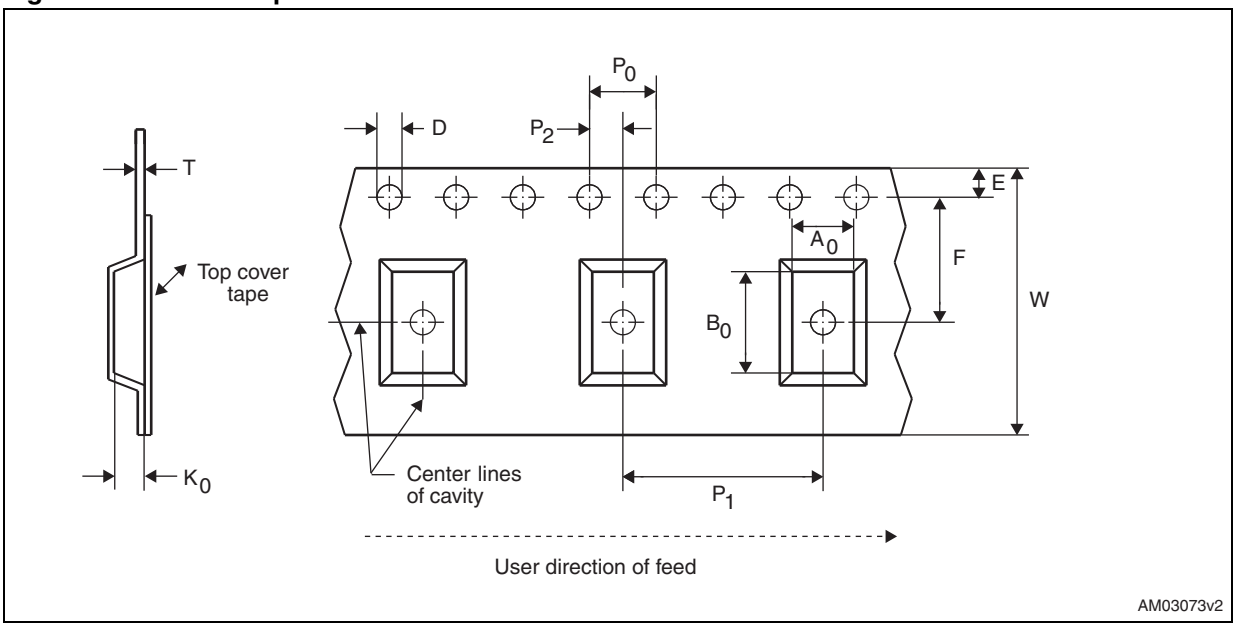


Table 10. Carrier tape dimensions

Package	W	D	E	P_0	P_2	F	A_0	B_0	K_0	P_1	T	Unit	Bulk qty.
TDFN8	8.00 +0.30 –0.10	1.50 +0.10/ –0.00	1.75 ±0.10	4.00 ±0.10	2.00 ±0.10	3.50 ±0.05	2.30 ±0.05	2.30 ±0.05	1.00 ±0.05	4.00 ±0.10	0.250 ±0.05	mm	3000

Figure 18. Reel dimensions

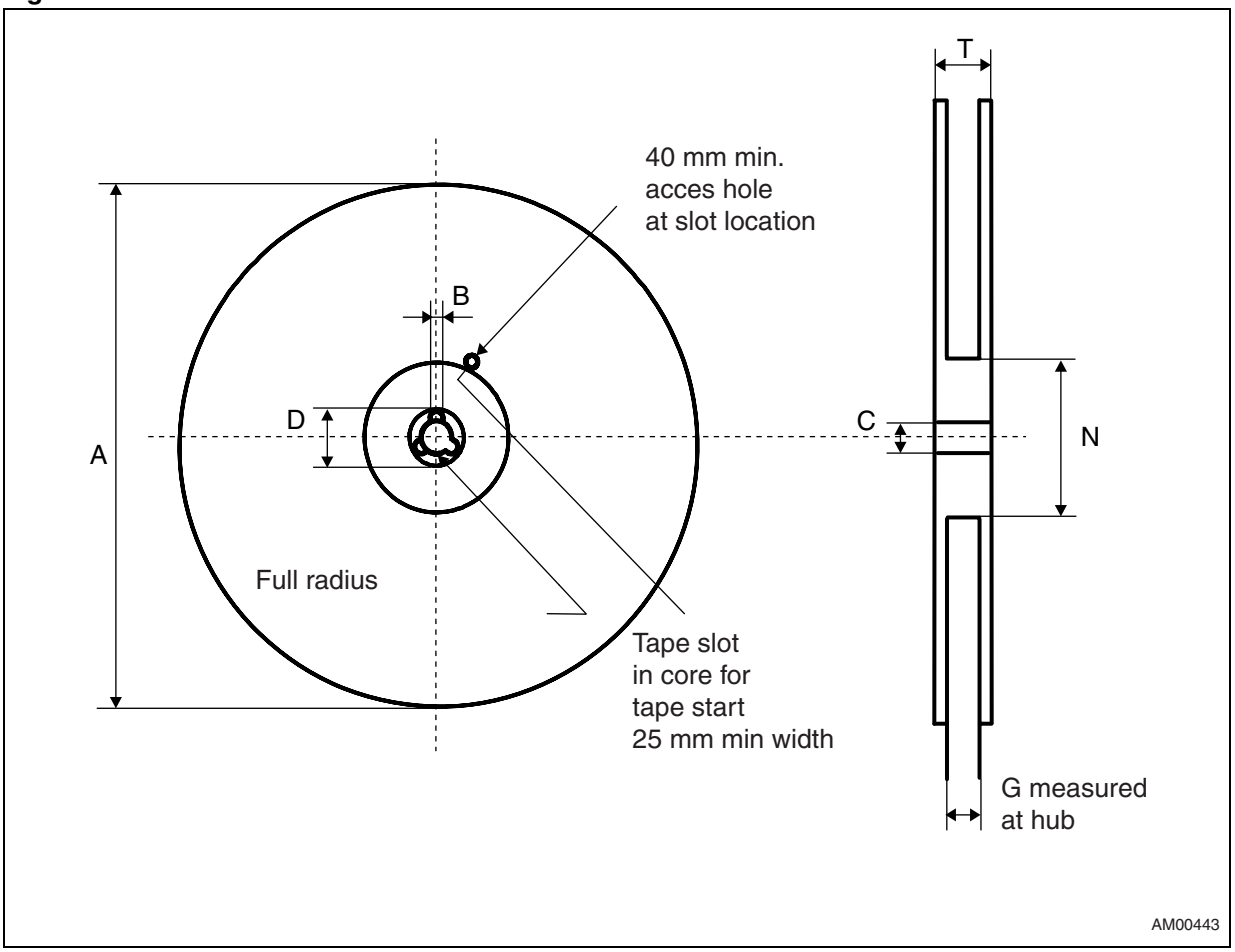


Table 11. Reel dimensions

Tape sizes	A max.	B min.	C	D min.	N min.	G	T max.
8 mm	180 (7 inches)	1.50	13.0 +/– 0.20	20.20	60	8.4 +2/–0	14.40

Figure 19. Tape trailer/leader

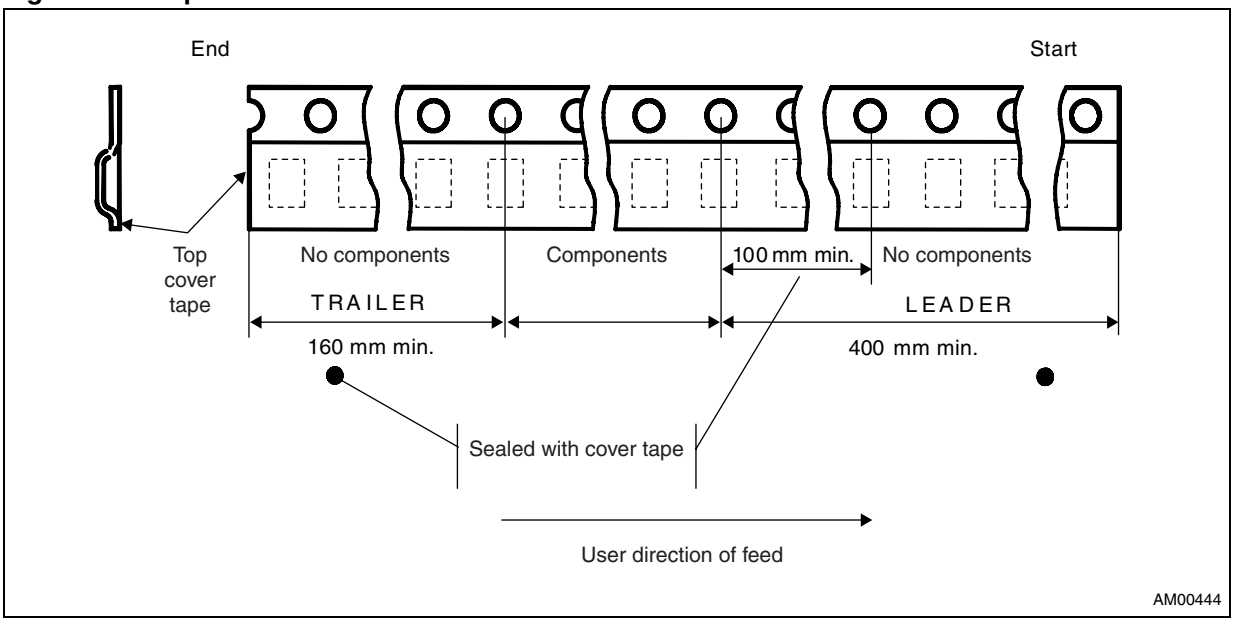
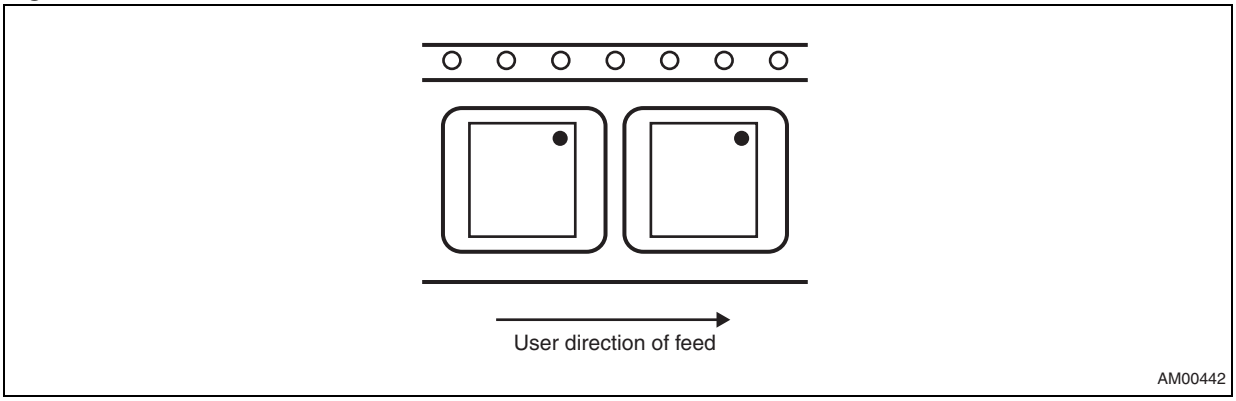


Figure 20. Pin 1 orientation



Note: 1 Drawings are not to scale.

2 All dimensions are in mm, unless otherwise noted.