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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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STM6600, STM6601

Smart push-button on/off controller with Smart Reset™ and power-on lockout

Datasheet - production data

TDFN12

Features

- Operating voltage 1.6 V to 5.5 V
- Low standby current of 0.6 µA
- Adjustable Smart Reset™ assertion delay time driven by external C_{SRD}
- Power-up duration determined primarily by push-button press (STM6600) or by fixed time period, t_{ON_BLANK} (STM6601)
- Debounced $\overline{PB}$ and $\overline{SR}$ inputs
- $\overline{PB}$ and $\overline{SR}$ ESD inputs withstand voltage up to ±15 kV (air discharge) ±8 kV (contact discharge)
- Active high or active low enable output option ($\overline{EN}$ or EN) provides control of MOSFET, DC-DC converter, regulator, etc.
- Secure startup, interrupt, Smart Reset™ or power-down driven by push-button
- Precise 1.5 V voltage reference with 1% accuracy
- Industrial operating temperature –40 to +85 °C
- Available in TDFN12 2 x 3 mm package

Applications

- Portable devices
- Terminals
- Audio and video players
- Cell phones and smart phones
- PDAs, palmtops, organizers

Table 1. Device summary

Device	$\overline{RST}$	C_{SRD}	$\overline{PB}$ / $\overline{SR}$	EN or $\overline{EN}$	$\overline{INT}$	Startup process
STM6600	open drain(1)	✓	✓	Push-pull	Open drain(1)	$\overline{PB}$ must be held low until the PS_{HOLD}(2) confirmation
STM6601	open drain(1)	✓	✓	Push-pull	Open drain(1)	PB can be released before the PS_{HOLD}(2) confirmation

1. External pull-up resistor needs to be connected to open drain outputs.
2. For a successful startup, the PS_{HOLD} (power supply hold) needs to be pulled high within specific time, t_{ON_BLANK}.

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1 Description

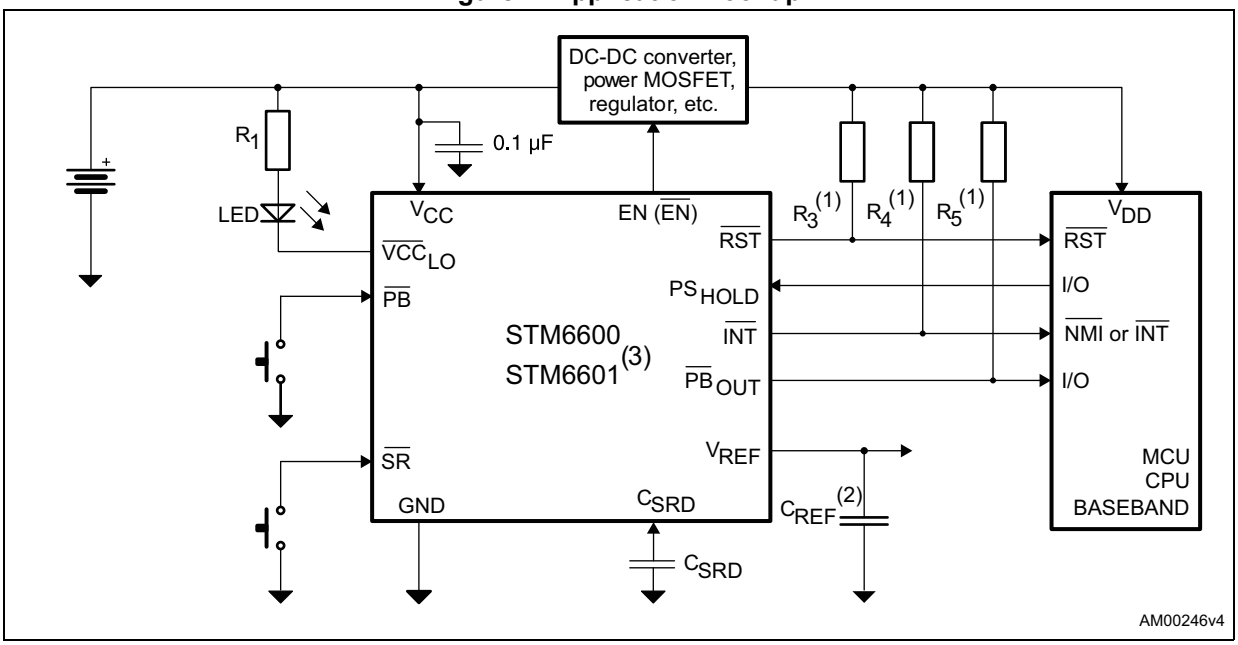
The STM6600-01 devices monitor the state of connected push-button(s) as well as sufficient supply voltage. An enable output controls power for the application through the MOSFET transistor, DC-DC converter, regulator, etc. If the supply voltage is above a precise voltage threshold, the enable output can be asserted by a simple press of the button. Factory-selectable supply voltage thresholds are determined by highly accurate and temperature-compensated references. An interrupt is asserted by pressing the push-button during normal operation and can be used to request a system power-down. The interrupt is also asserted if undervoltage is detected. By a long push of one button ($\overline{PB}$) or two buttons ($\overline{PB}$ and $\overline{SR}$) either a reset is asserted or power for the application is disabled depending on the option used.

The device also offers additional features such as precise 1.5 V voltage reference with very tight accuracy of 1%, separate output indicating undervoltage detection and separate output for distinguishing between interrupt by push-button or undervoltage.

The device consumes very low current of 6 µA during normal operation and only 0.6 µA current during standby.

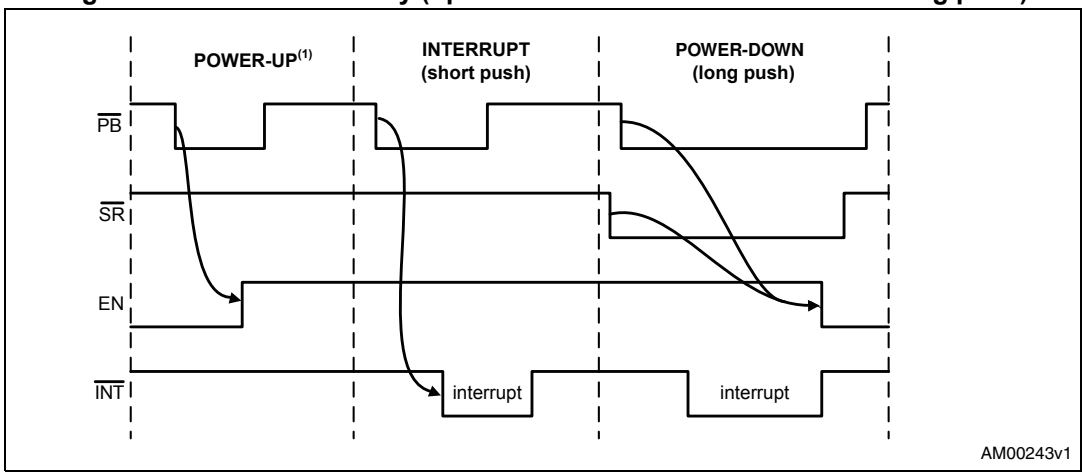
The STM6600-01 is available in the TDFN12 package and is offered in several options among features such as selectable threshold, hysteresis, timeouts, output types, etc.

Figure 1. Application hookup



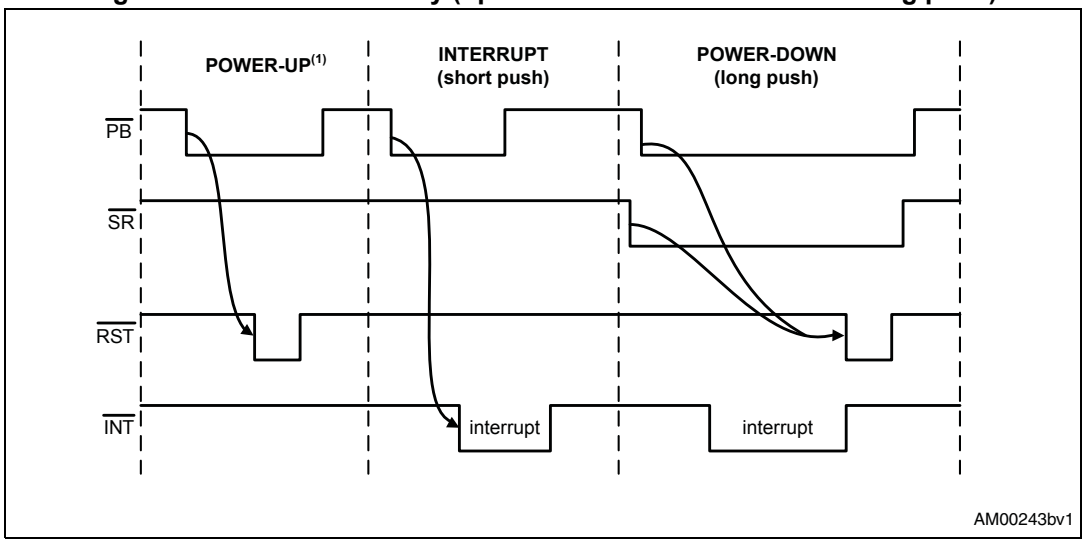
1. A resistor is required for open drain output type only. A 10 kΩ pull-up is sufficient in most applications.
2. Capacitor C_{REF} is mandatory on V_{REF} output (even if V_{REF} is not used). Capacitor value of 1 µF is recommended.
3. For the STM6601 the processor has to confirm the proper power-on during the fixed time period, t_{ON_BLANK}. This failsafe feature prevents the user from turning on the system when there is a faulty power switch or an unresponsive microprocessor.

Figure 2. Basic functionality (option with enable deassertion after long push)



1. For power-up the battery voltage has to be above V_{TH+} threshold.

Figure 3. Basic functionality (option with $\overline{RST}$ assertion after long push)



1. For power-up the battery voltage has to be above V_{TH+} threshold.

Figure 4. Logic diagram

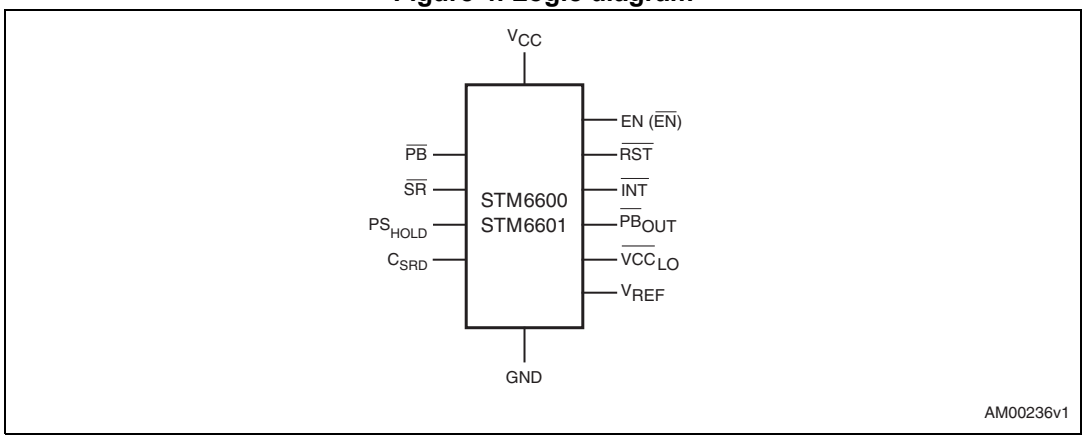


Table 2. Pin descriptions

Pin number	Symbol	Function
1	V_{CC}	Power supply input
2	$\overline{SR}$	Smart Reset™ button input
3	V_{REF}	Precise 1.5 V voltage reference
4	PS_{HOLD}	PS_{HOLD} input
5	C_{SRD}	Adjustable Smart Reset™ delay time input
6	$\overline{PB}$	Push-button input
7	$\overline{VCC}_{LO}$	Output for high threshold comparator output (V_{TH+})
8	$\overline{PB}_{OUT}$	Status of $\overline{PB}$ push-button input
9	EN or $\overline{EN}$	Enable output
10	$\overline{RST}$	Reset output
11	$\overline{INT}$	Interrupt output
12	GND	Ground

Figure 5. TDFN12 pin connections

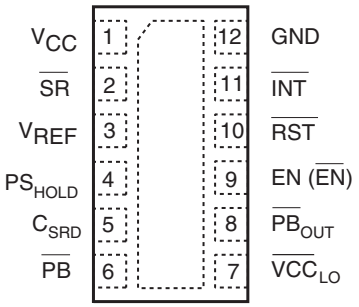


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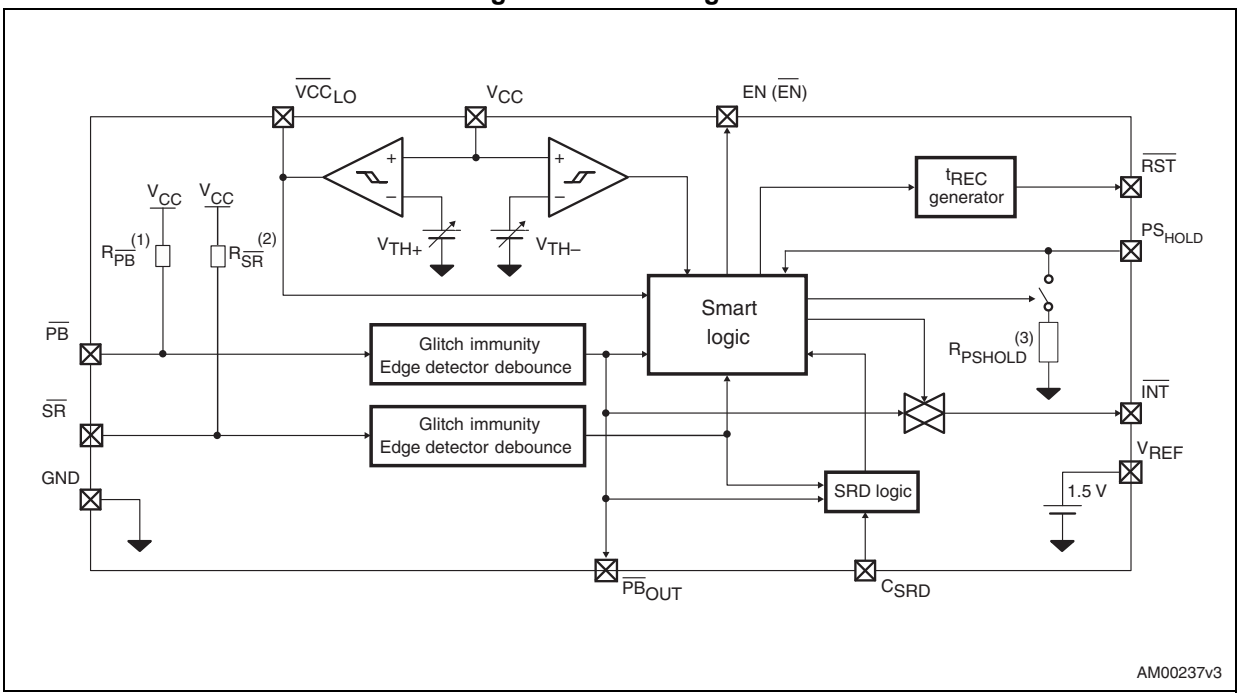
Figure 6. Block diagram



1. Internal pull-up resistor connected to $\overline{PB}$ input (see *Table 5* for precise specifications).
2. Optional internal pull-up resistor connected to $\overline{SR}$ input (see *Table 5* for precise specifications and *Table 10* for detailed device options).
3. Internal pull-down resistor is connected to PS_{HOLD} input only during startup (see *Figure 7*, *8*, *9*, *10*, *11*, *12*, *13*, and *18*).

2 Pin descriptions

V_{CC} - power supply input

V_{CC} is monitored during startup and normal operation for sufficient voltage level. Decouple the V_{CC} pin from ground by placing a 0.1 µF capacitor as close to the device as possible.

$\overline{SR}$ - Smart Reset™ button input

This input is equipped with voltage detector with a factory-trimmed threshold and has ±8 kV HBM ESD protection.

Both $\overline{PB}$ and $\overline{SR}$ buttons have to be pressed and held for t_{SRD} period so the long push is recognized and the reset is asserted (or the enable output is deasserted depending on the option) - see *Figure 15*, *16*, and *17*.

Active low $\overline{SR}$ input is usually connected to GND through the momentary push-button (see *Figure 1*) and it has an optional 100 kΩ pull-up resistor. It is also possible to drive this input using an external device with either open drain (recommended) or push-pull output. Open drain output can be connected in parallel with push-button or other open drain outputs, which is not possible with push-pull output. $\overline{SR}$ input is monitored for falling edge after power-up and must not be grounded permanently.

V_{REF} - external precise 1.5 V voltage reference

This 1.5 V voltage reference is specified with very tight accuracy of 1% (see *Table 5*). It has proper output voltage as soon as the reset output is deasserted (i.e. after t_{REC} expires) and it is disabled when the device enters standby mode. A mandatory capacitor needs to be connected to V_{REF} output (even if V_{REF} is not used). Capacitor value of 1 µF is recommended.

PS_{HOLD} input

This input is equipped with a voltage detector with a factory-trimmed threshold. It is used to confirm correct power-up of the device (if EN or $\overline{EN}$ is not asserted) or to initiate a shutdown (if EN or $\overline{EN}$ is asserted).

Forcing PS_{HOLD} high during power-up confirms the proper start of the application and keeps enable output asserted. Because most processors have outputs in high-Z state before initialization, an internal pull-down resistor is connected to PS_{HOLD} input during startup (see *Figure 7*, *8*, *9*, *10*, *11*, *12*, *13*, and *18*).

Forcing the PS_{HOLD} signal low during normal operation deasserts the enable output (see *Figure 14*). Input voltage on this pin is compared to an accurate voltage reference.

C_{SRD} - Smart Reset™ delay time input

A capacitor to ground determines the additional time (t_{SRD}) that $\overline{PB}$ with $\overline{SR}$ must be pressed and held before a long push is recognized. The connected C_{SRD} capacitor is charged with I_{SRD} current. Additional Smart Reset™ delay time t_{SRD} ends when voltage on the C_{SRD} capacitor reaches the V_{SRD} voltage threshold. It is recommended to use a low ESR capacitor (e.g. ceramic). If the capacitor is not used, leave the C_{SRD} pin open. If no capacitor is connected, there is no t_{SRD} and a long push is recognized right after $t_{\overline{INT}\_Min}$ expires (see *Figure 18* and *19*).

$\overline{PB}$ - power ON switch

This input is equipped with a voltage detector with a factory-trimmed threshold and has ± 8 kV HBM ESD protection.

When the $\overline{PB}$ button is pressed and held, the battery voltage is detected and EN (or $\overline{EN}$) is asserted if the battery voltage is above the threshold V_{TH+} during the whole $t_{DEBOUNCE}$ period (see *Figure 13*).

A short push of the push-button during normal operation can initiate an interrupt through debounced $\overline{INT}$ output (see *Figure 14*) and a long push of $\overline{PB}$ and $\overline{SR}$ simultaneously can either assert reset output $\overline{RST}$ (see *Figure 18*) or deassert the EN or $\overline{EN}$ output (see *Figure 19*) based on the option used.

Note: A switch to GND must be connected to this input (e.g. mechanical push-button, open drain output of external circuitry, etc.), see Figure 1. This ensures a proper startup signal on $\overline{PB}$ (i.e. a transition from full V_{CC} below specified V_{IL}). $\overline{PB}$ input has an internal 100 kΩ pull-up resistor connected.

$\overline{VCC}_{LO}$ - high threshold detection output

During power-up, $\overline{VCC}_{LO}$ is low when V_{CC} supply voltage is below the V_{TH+} threshold. After successful power-up (i.e. during normal operation) $\overline{VCC}_{LO}$ is low anytime undervoltage is detected (see *Figure 13*).

Output type is active low and open drain by default. Open drain output type requires a pull-up resistor. A 10 kΩ is sufficient in most applications.

$\overline{VCC}_{LO}$ is floating when STM660x is in standby mode.

$\overline{PB}_{OUT}$ - $\overline{PB}$ input state

If the push-button $\overline{PB}$ is pressed, the pin stays low during the $t_{DEBOUNCE}$ time period. If $\overline{PB}$ is asserted for the entire $t_{DEBOUNCE}$ period, $\overline{PB}_{OUT}$ will then stay low for at least $t_{\overline{INT}\_Min}$. If $\overline{PB}$ is asserted after $t_{\overline{INT}\_Min}$ expires, $\overline{PB}_{OUT}$ will return high as soon as $\overline{PB}$ is deasserted (see *Figure 22*). $\overline{PB}_{OUT}$ ignores $\overline{PB}$ assertion during an undervoltage condition. At startup on the STM6601 $\overline{PB}_{OUT}$ will respond only to the first $\overline{PB}$ assertion and any other assertion will be ignored until t_{ON_BLANK} expires. This output is active low and open drain by default. Open drain output type requires a pull-up resistor. A 10 kΩ is sufficient in most applications.

EN or $\overline{EN}$ - enable output

This output is intended to enable system power (see *Figure 1*). EN is asserted **high** after a valid turn-on event has been detected and confirmed (i.e. push-button has been pressed and held for $t_{DEBOUNCE}$ or more and $V_{CC} > V_{TH+}$ voltage level has been detected - see *Figure 13*). EN is released **low** if any of the conditions below occur:

a) the push-button is released before PS_{HOLD} is driven high (valid for STM6600, see *Figure 9*) or t_{ON_BLANK} expires before PS_{HOLD} is driven high during startup (valid for both STM6600 and STM6601, see *Figure 10* and *12*).

b) PS_{HOLD} is driven low during normal operation (see *Figure 14*).

c) an undervoltage condition is detected for more than $t_{SRD} + t_{\overline{INT}\_Min} + t_{DEBOUNCE}$ (see *Figure 21*).

d) a long push of the buttons is detected (only for the device with option “EN deasserted by long push” - see *Figure 19*) or PS_{HOLD} is not driven high during t_{ON_BLANK} after a long push of the buttons (only for the device with option “$\overline{RST}$ asserted by long push” - see *Figure 18*).

Described logic levels are inverted in case of $\overline{EN}$ output. Output type is push-pull by default.

$\overline{RST}$ - reset output

This output pulls low for t_{REC}:

a) during startup. $\overline{PB}$ has been pressed (falling edge on the $\overline{PB}$ detected) and held for at least $t_{DEBOUNCE}$ and $V_{CC} > V_{TH+}$ (see *Figure 7*, *8*, *9*, *10*, *11*, *12* and *13* for more details).

b) after long push detection (valid only for the device with option “$\overline{RST}$ asserted by long push”). $\overline{PB}$ has been pressed (falling edge on the $\overline{PB}$ detected) and held for more than $t_{DEBOUNCE} + t_{SRD}$ (additional Smart Reset™ delay time can be adjusted by the external capacitor C_{SRD}) - see *Figure 18*.

Output type is active low and open drain by default. Open drain output type requires a pull-up resistor. A 10 kΩ is sufficient in most applications.

$\overline{INT}$ - interrupt output

While the system is under normal operation (PS_{HOLD} is driven high, power for application is asserted), the $\overline{INT}$ is driven **low** if:

a) V_{CC} falls below V_{TH-} threshold (i.e. undervoltage is detected - see *Figure 20* and *21*).

b) the falling edge on the $\overline{PB}$ is detected and the push-button is held for $t_{DEBOUNCE}$ or more. $\overline{INT}$ is driven low after $t_{DEBOUNCE}$ and stays low as long as $\overline{PB}$ is held. The $\overline{INT}$ signal is held high during power-up.

The state of the $\overline{PB}_{OUT}$ output can be used to determine if the interrupt was caused by either the assertion of the $\overline{PB}$ input, or was due to the detection of an undervoltage condition on V_{CC}.

$\overline{INT}$ output is asserted low for at least $t_{\overline{INT}\_Min}$.

Output type is active low and open drain by default. Open drain output type requires a pull-up resistor. A 10 kΩ is sufficient in most applications.

GND - ground

3 Operation

The STM6600-STM6601 simplified smart push-button on/off controller with Smart Reset™ and power-on lockout enables and disables power for the application depending on push-button states, signals from the processor, and battery voltage.

Power-on

Because most of the processors have outputs in high-Z state before initialization, an internal pull-down resistor is connected to PS_{HOLD} input during startup (see *Figure 7*, *8*, *9*, *10*, *11*, *12*, *13*, and *18*).
To power up the device the push-button $\overline{PB}$ has to be pressed for at least $t_{DEBOUNCE}$ and V_{CC} has to be above V_{TH+} for the whole $t_{DEBOUNCE}$ period. If the battery voltage drops below V_{TH+} during the $t_{DEBOUNCE}$, the counter is reset and starts to count again when $V_{CC} > V_{TH+}$ (see *Figure 13*). After $t_{DEBOUNCE}$ the enable signal is asserted (EN goes high, $\overline{EN}$ goes low), reset output $\overline{RST}$ is asserted for t_{REC} and then the startup routine is performed by the processor. During initialization, the processor sets the PS_{HOLD} signal high.

On the STM6600 the PS_{HOLD} signal has to be set high prior to push-button release and t_{ON_BLANK} expiration, otherwise the enable signal is deasserted (EN goes low, $\overline{EN}$ goes high) - see *Figure 7*, *8*, *9*, and *10*. The time up to push-button release represents the maximum time allowed for the system to power up and initialize the circuits driving the PS_{HOLD} input. If the PS_{HOLD} signal is low at push-button release, the enable output is deasserted immediately, thus turning off the system power. If t_{ON_BLANK} expires prior to push-button release, the PS_{HOLD} state is checked at its expiration. This safety feature disables the power and prevents discharging the battery if the push-button is stuck or it is held for an unreasonable period of time and the application is not responding (see *Figure 8* and *10*). $\overline{PB}$ status, $\overline{INT}$ status and V_{CC} undervoltage detection are not monitored until power-up is completed.

On the STM6601 the PS_{HOLD} signal has to be set high before t_{ON_BLANK} expires, otherwise the enable signal is deasserted - see *Figure 11* and *12*. In this case the t_{ON_BLANK} period is the maximum time allowed for the power switch and processor to perform the proper power-on. If the PS_{HOLD} signal is low at the end of the blanking period, the enable output is released immediately, thus turning off the system power. $\overline{PB}$ status, $\overline{INT}$ status and V_{CC} undervoltage detection are not monitored during the entire t_{ON_BLANK} period. This failsafe feature prevents the user from turning on the system when there is a faulty power switch or an unresponsive microprocessor.

Push-button interrupt

If the device works under normal operation (i.e. PS_{HOLD} is high) and the push-button $\overline{PB}$ is pressed for more than $t_{DEBOUNCE}$, a negative pulse with minimum $t_{\overline{INT}\_Min}$ width is generated on the $\overline{INT}$ output. By connecting $\overline{INT}$ to the processor interrupt input ($\overline{INT}$ or $\overline{NMI}$) a safeguard routine can be performed and the power can be shut down by setting PS_{HOLD} low - see *Figure 14*.

Forced power-down mode

The PS_{HOLD} output can be forced low anytime during normal operation by the processor and can deassert the enable signal - see *Figure 14*.

Undervoltage detection

If V_{CC} voltage drops below V_{TH-} voltage threshold during normal operation, the $\overline{INT}$ output is driven low (see *Figure 20* and *Figure 21*).

If an undervoltage condition is detected for $t_{DEBOUNCE} + t_{\overline{INT}\_Min} + t_{SRD}$, the enable output is deasserted (see *Figure 21*).

Hardware reset or power-down while system not responding

If the system is not responding and the system hangs, the $\overline{PB}$ and $\overline{SR}$ push-buttons can be pressed simultaneously longer than $t_{DEBOUNCE} + t_{\overline{INT}\_Min} + t_{SRD}$, and then

a) either the reset output $\overline{RST}$ is asserted for t_{REC} and the processor is reset (valid only for the device with option "$\overline{RST}$ asserted by long push") – see *Figure 18*

b) or the power is disabled by EN or $\overline{EN}$ signal (valid only for the device with option "EN deasserted by long push") – see *Figure 19*

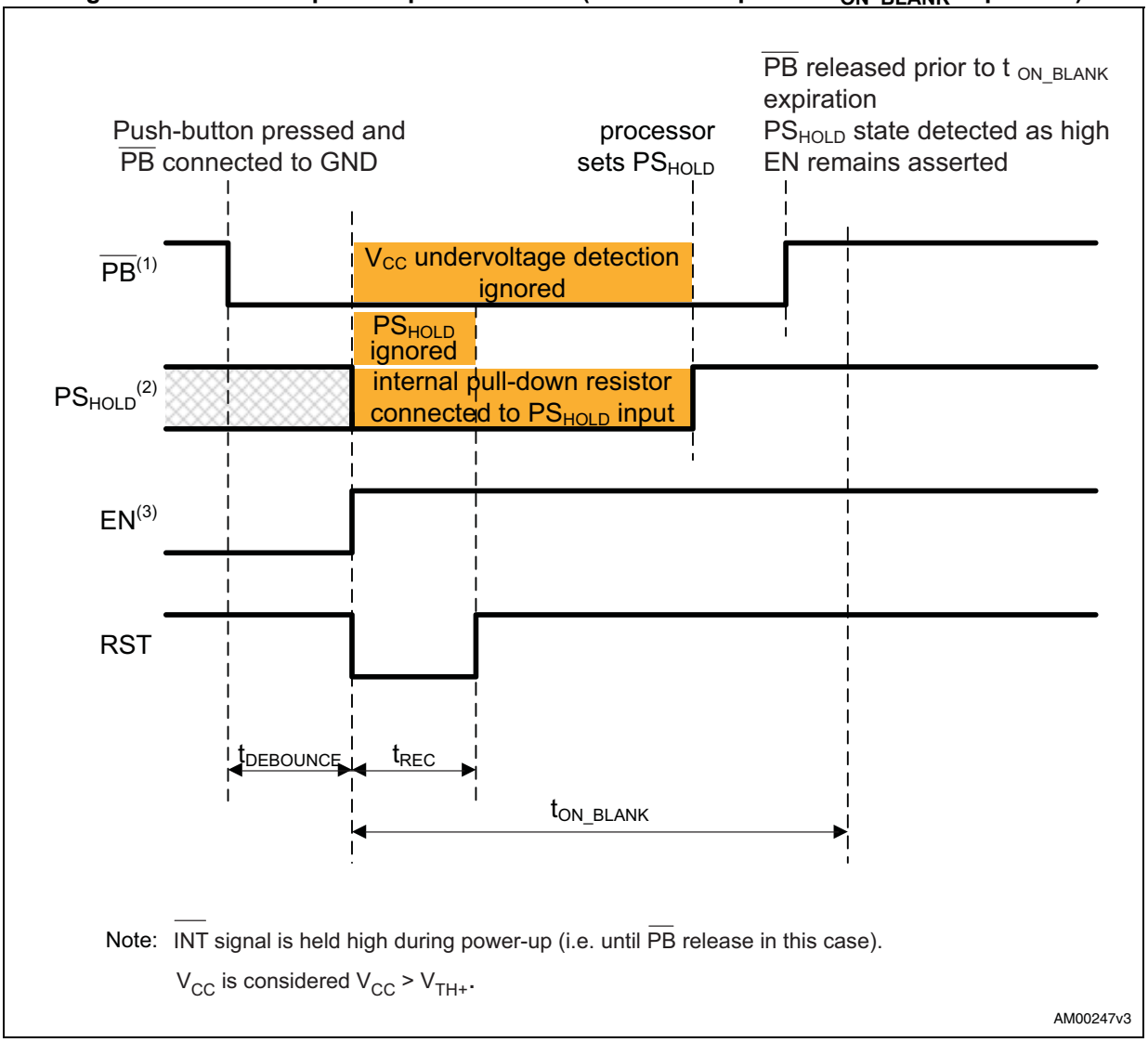
The t_{SRD} is set by the external capacitor connected to the C_{SRD} pin. $\overline{SR}$ input is monitored for falling edge after power-up and must not be grounded permanently.

Standby

If the enable output is deasserted (i.e. EN is low or $\overline{EN}$ is high), the STM660x device enters standby mode with low current consumption (see *Table 5*). In standby mode $\overline{PB}$ input is only monitored for the falling edge. The external 1.5 V voltage reference is also disabled in standby mode.

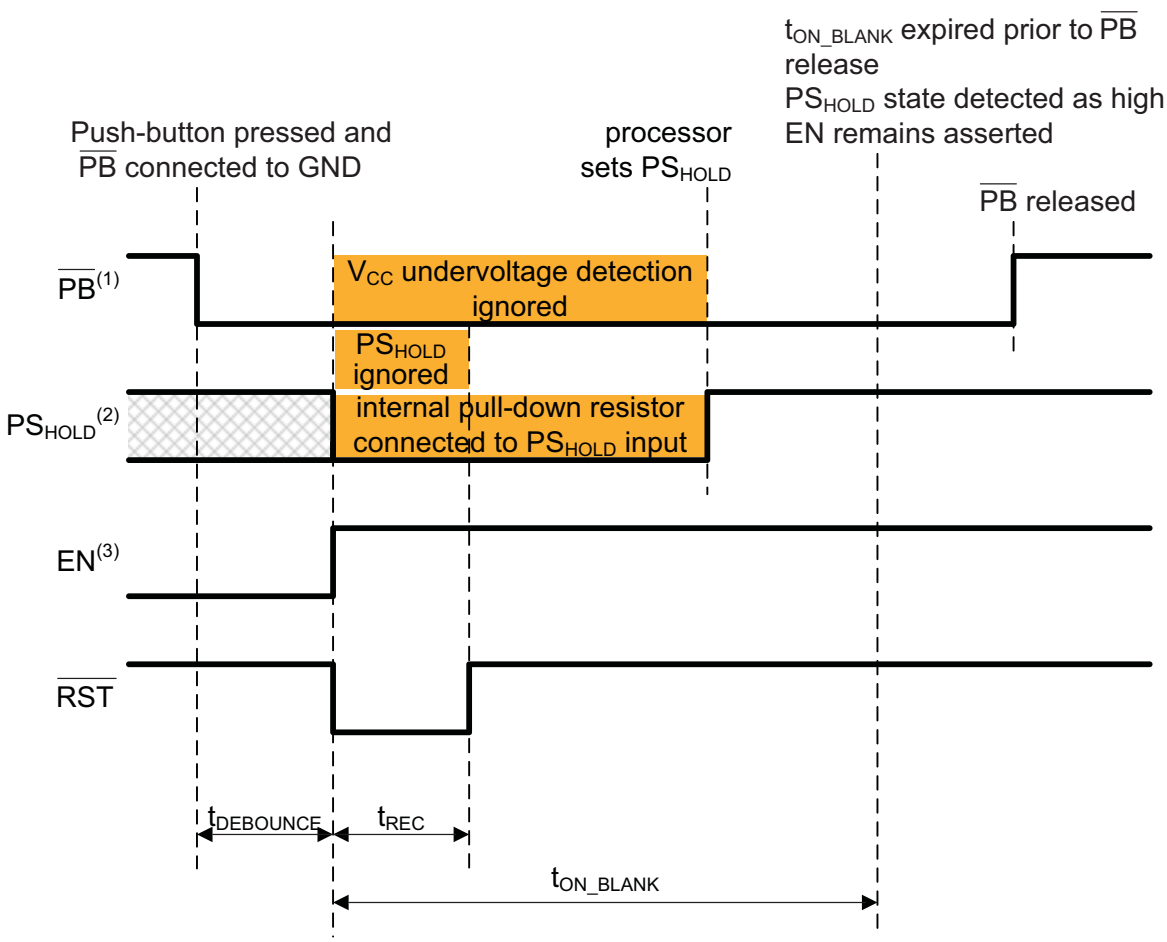
4 Waveforms

Figure 7. Successful power-up on STM6600 ($\overline{PB}$ released prior to t_{ON_BLANK} expiration)



1. $\overline{PB}$ detection on falling and rising edges.
2. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during power-up.
3. EN signal is high even after $\overline{PB}$ release, because processor sets PS_{HOLD} signal high before $\overline{PB}$ is released.

Figure 8. Successful power-up on STM6600 (t_{ON_BLANK} expires prior to $\overline{PB}$ release)

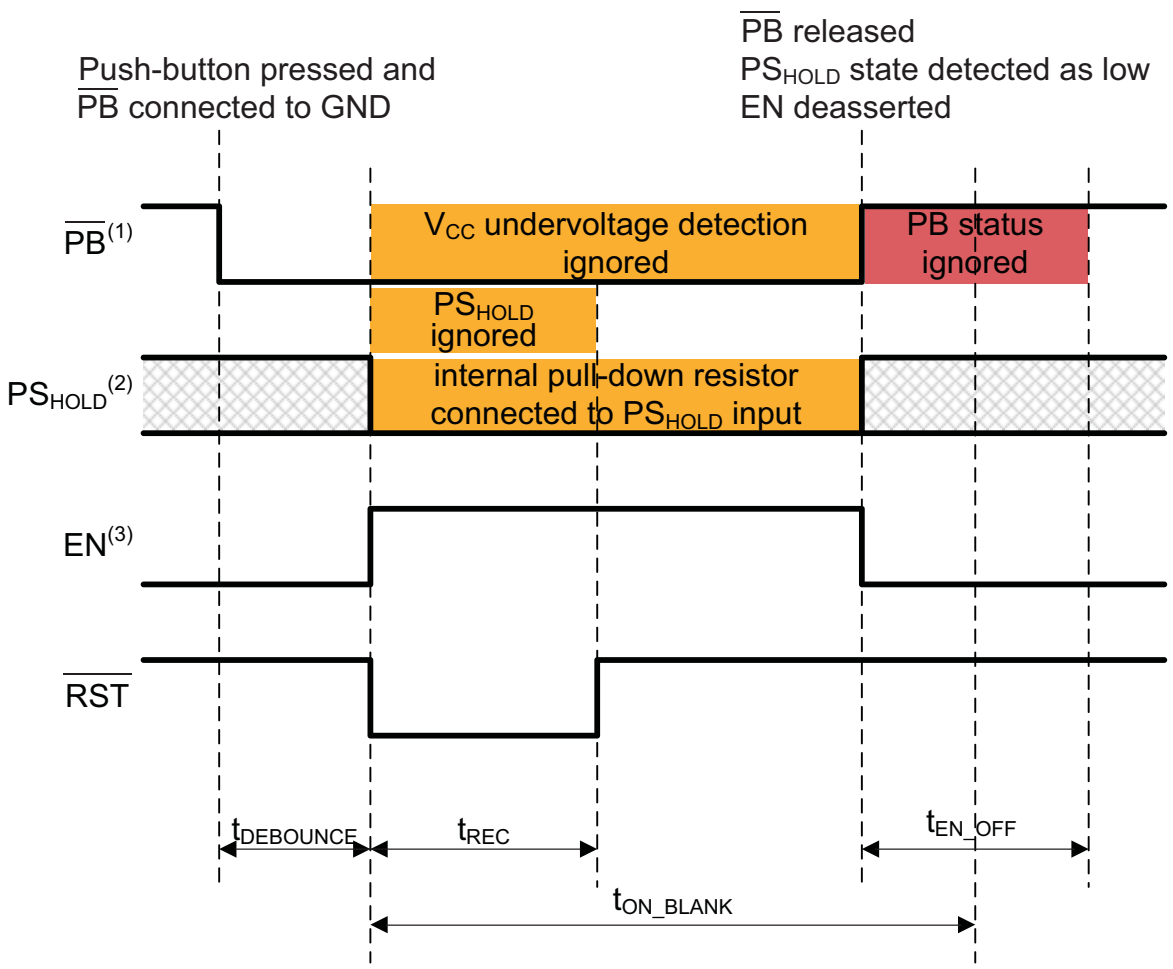


Note: $\overline{INT}$ signal is held high during power-up (i.e. until t_{ON_BLANK} expires in this case).
V_{CC} is considered $V_{CC} > V_{TH+}$.

AM00247bv2

1. $\overline{PB}$ detection on falling and rising edges.
2. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during power-up.
3. t_{ON_BLANK} expires prior to $\overline{PB}$ release so PS_{HOLD} is checked at its expiration.

Figure 9. Unsuccessful power-up on STM6600 ($\overline{PB}$ released prior to t_{ON_BLANK})

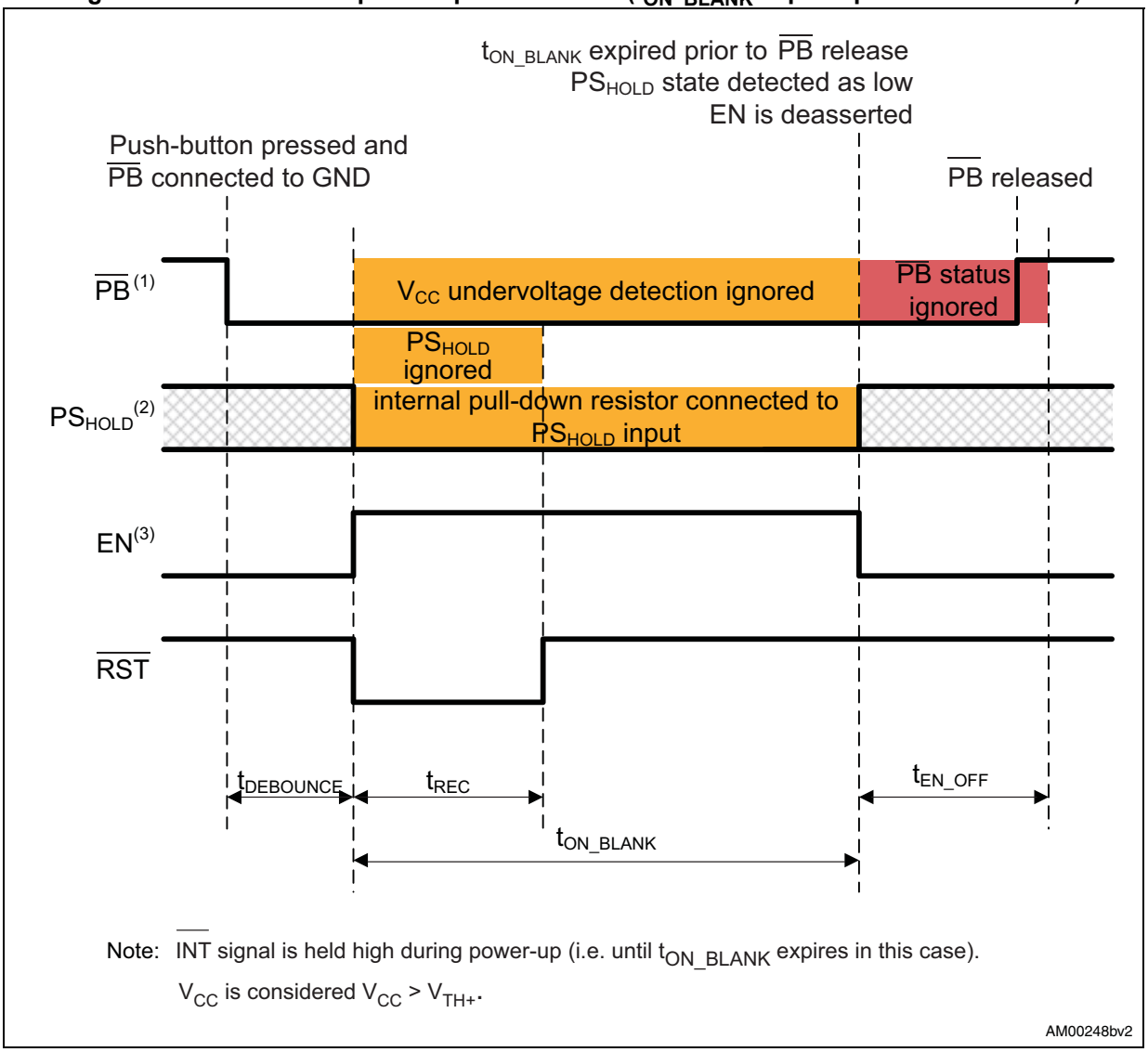


Note: $\overline{INT}$ signal is held high during power-up (i.e. until $\overline{PB}$ release in this case).
V_{CC} is considered $V_{CC} > V_{TH+}$.

AM00248v3

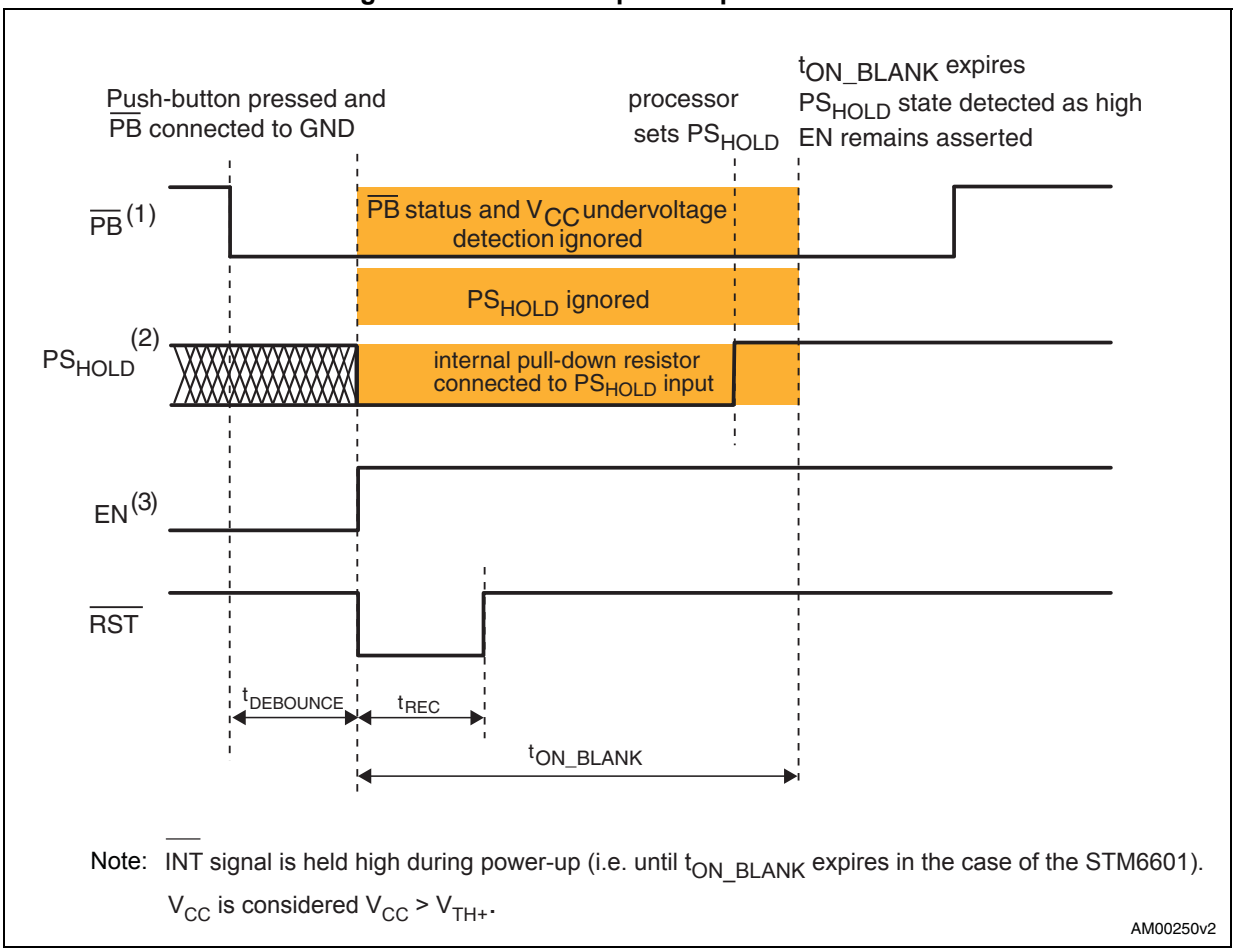
1. $\overline{PB}$ detection on falling and rising edges.
2. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during power-up.
3. EN signal goes low with $\overline{PB}$ release, because processor did not force PS_{HOLD} signal high.

Figure 10. Unsuccessful power-up on STM6600 (t_{ON_BLANK} expires prior to $\overline{PB}$ release)



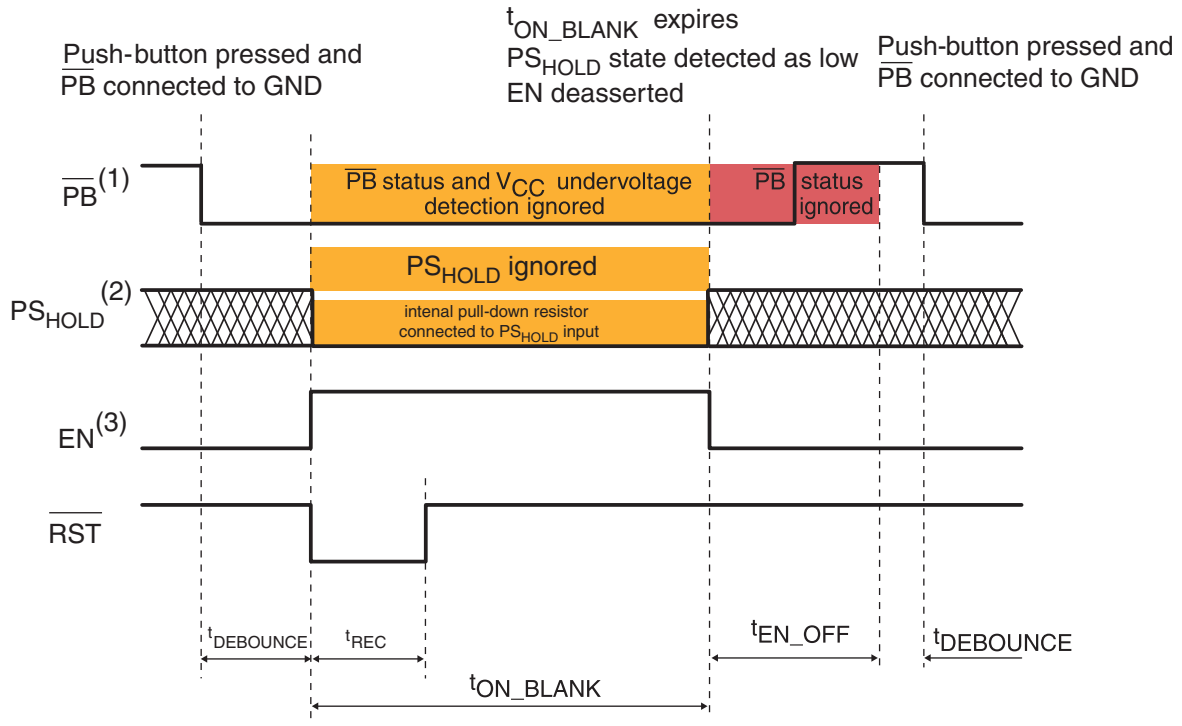
1. $\overline{PB}$ detection on falling and rising edges.
2. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during power-up.
3. t_{ON_BLANK} expires prior to $\overline{PB}$ release so PS_{HOLD} is checked at its expiration.

Figure 11. Successful power-up on STM6601



1. $\overline{PB}$ detection on falling edge.
2. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during power-up.
3. PS_{HOLD} signal is ignored during t_{ON_BLANK}. When t_{ON_BLANK} expires, the level of the PS_{HOLD} signal is high therefore the EN signal remains asserted.

Figure 12. Unsuccessful power-up on STM6601

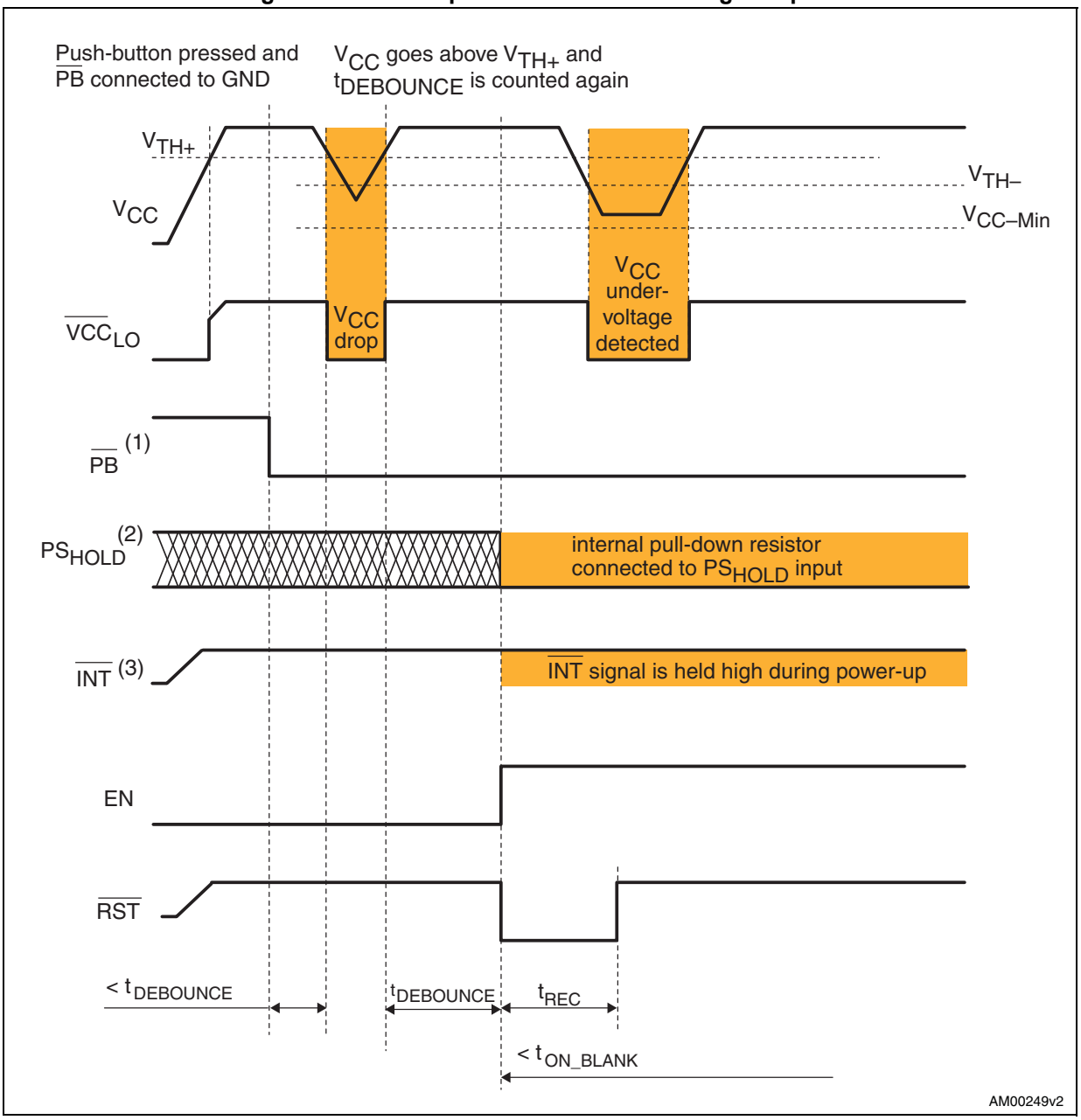


Note: INT signal is held high during power-up (i.e. until t_{ON_BLANK} expires in the case of the STM6601).
V_{CC} is considered $V_{CC} > V_{TH+}$.

AM00238v2

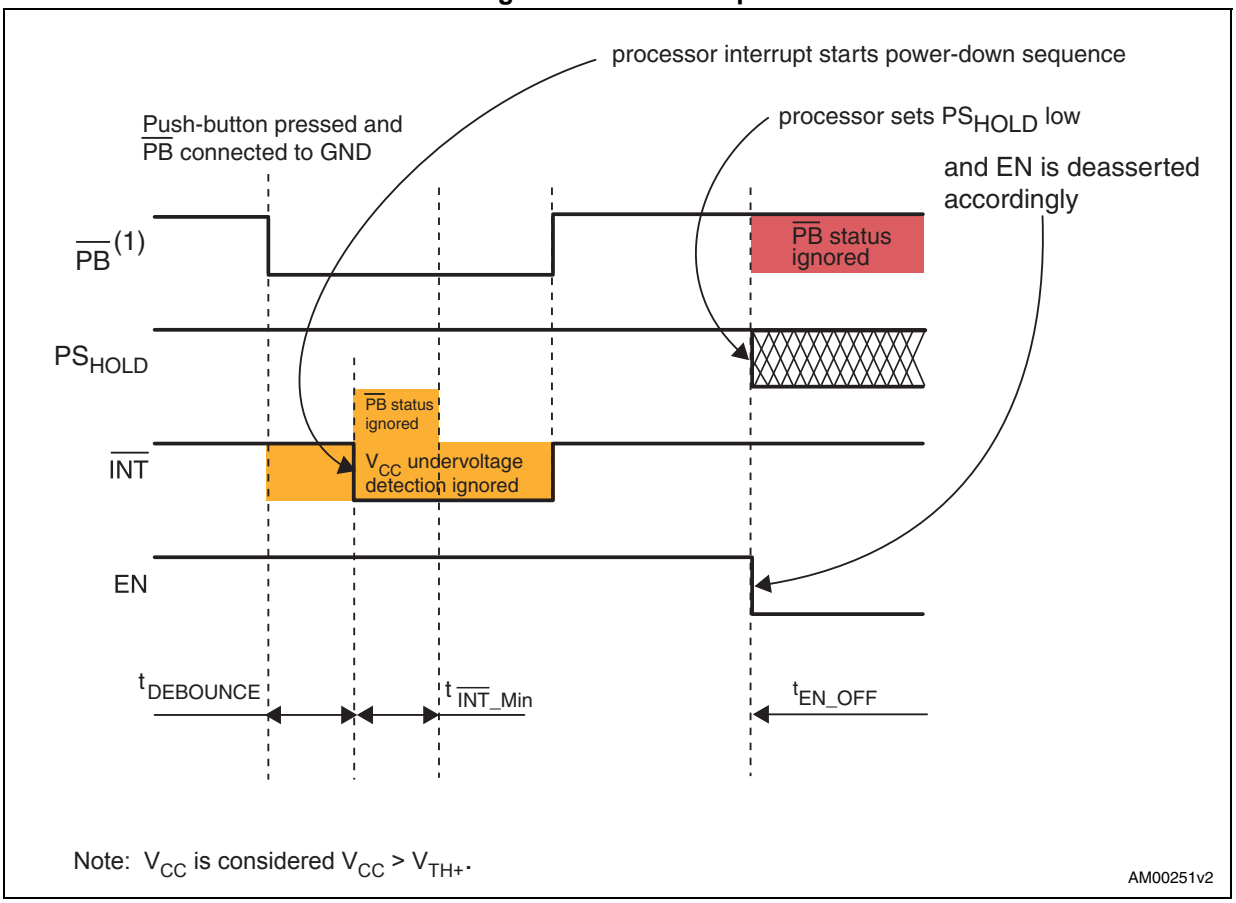
1. PB detection on falling edge.
2. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during power-up.
3. PS_{HOLD} signal is ignored during t_{ON_BLANK}. When t_{ON_BLANK} expires, the level of the PS_{HOLD} signal is not high therefore the EN signal goes low. Even releasing the PB button after the t_{ON_BLANK} will not prevent this.

Figure 13. Power-up on STM660x with voltage dropout



1. $\overline{PB}$ detection on falling and rising edges.
2. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during power-up.
3. $\overline{INT}$ signal is held high during power-up.

Figure 14. $\overline{PB}$ interrupt



1. $\overline{PB}$ detection on falling edge.

Figure 15. Long push, $\overline{PB}$ pressed first

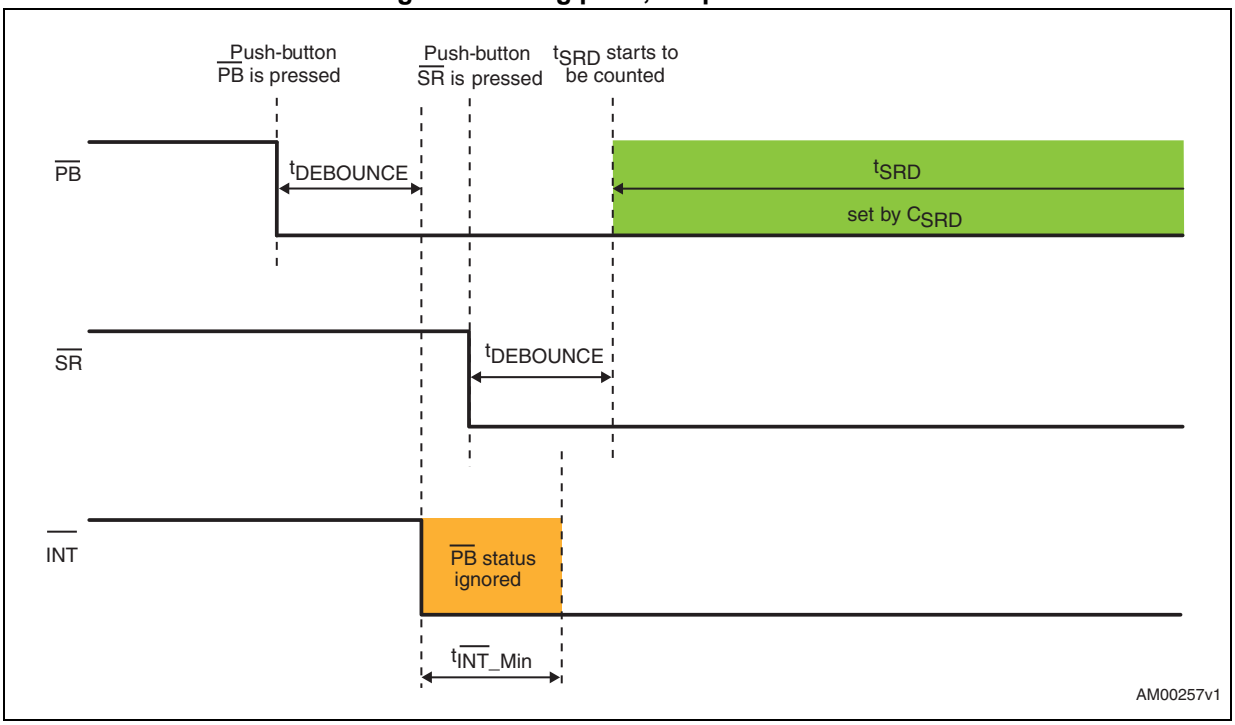


Figure 16. Long push, $\overline{SR}$ pressed first

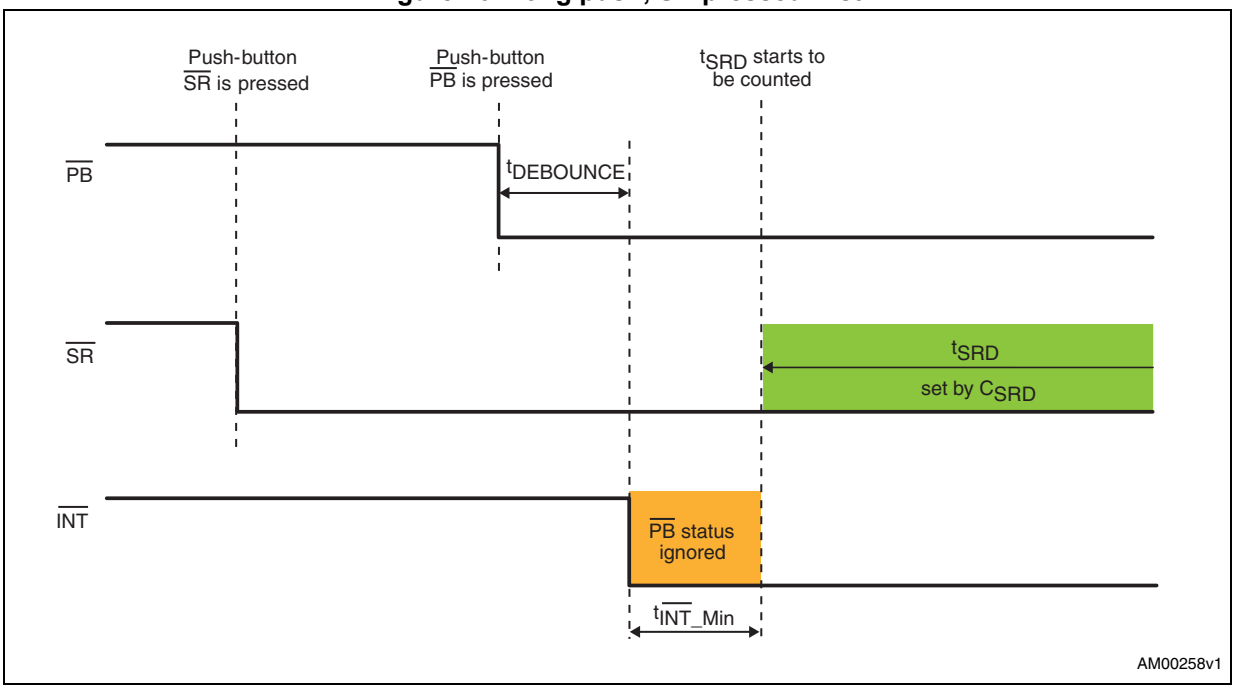


Figure 17. Invalid long push

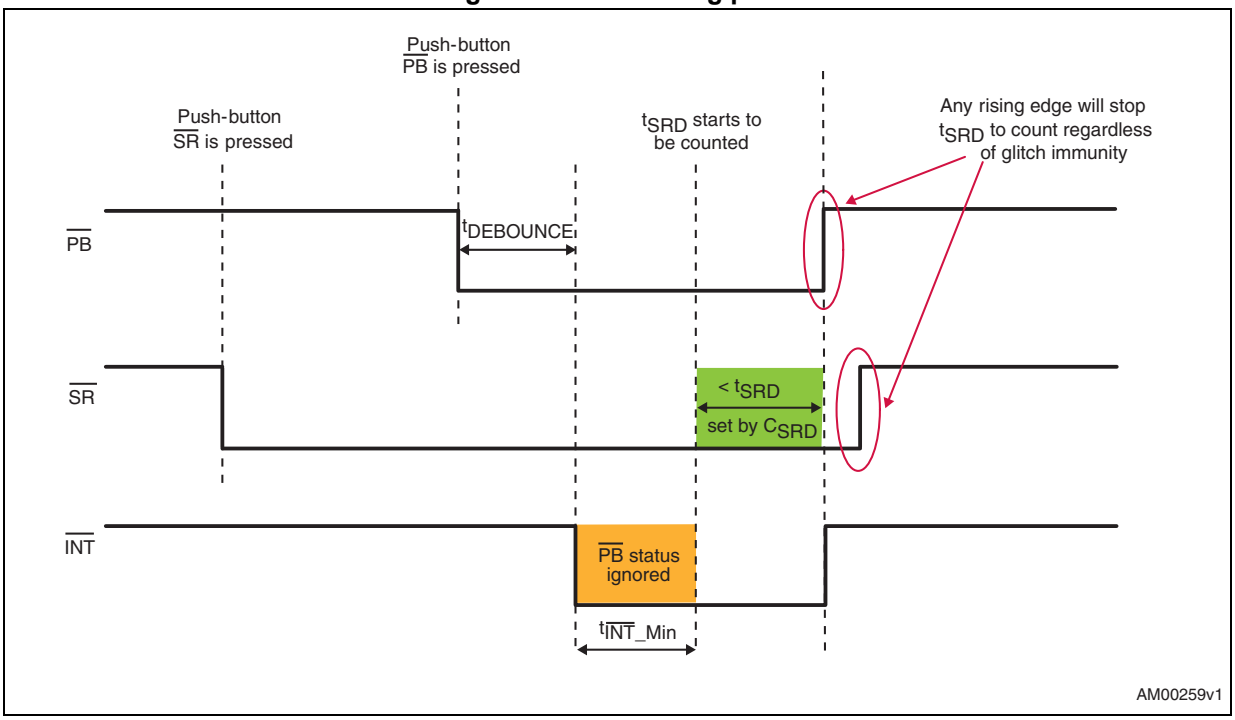
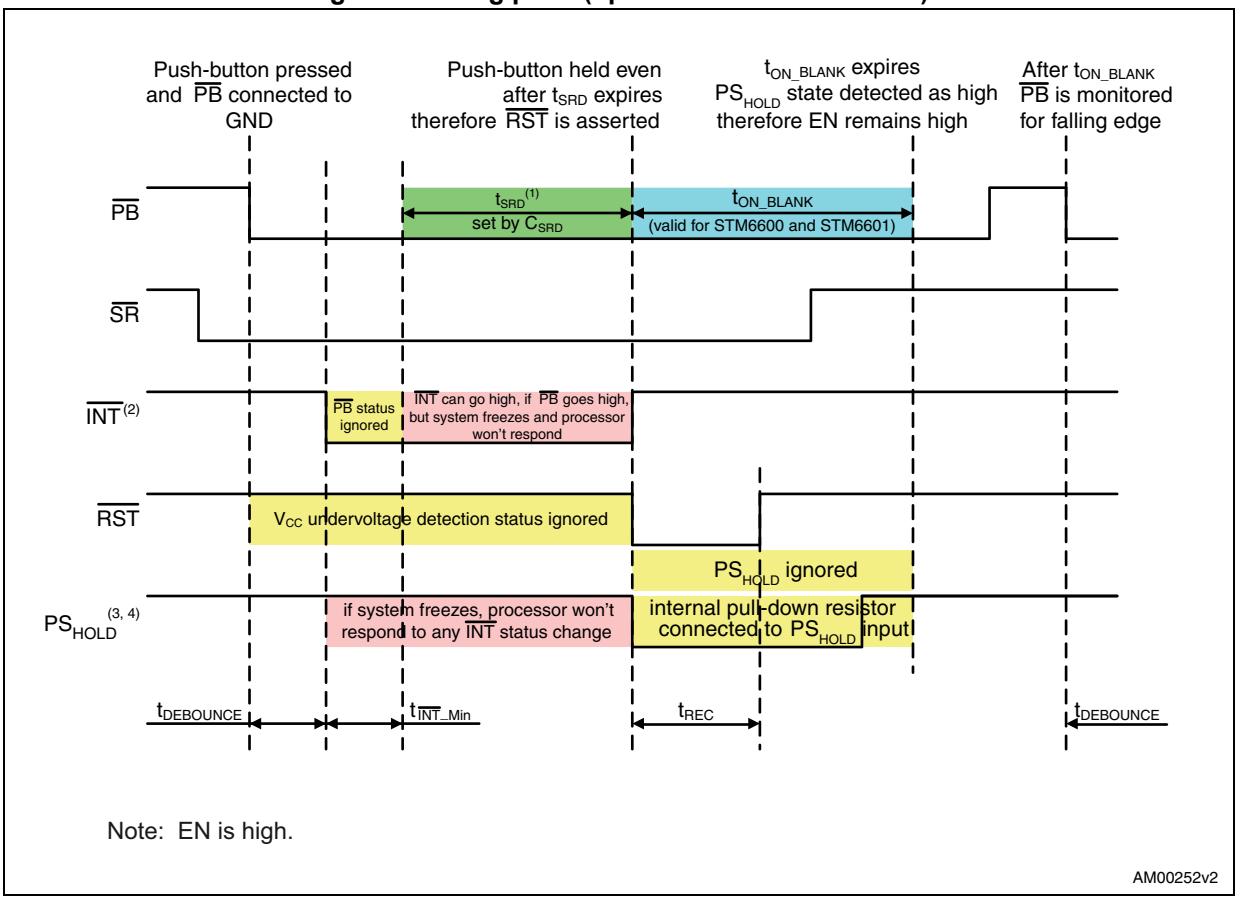
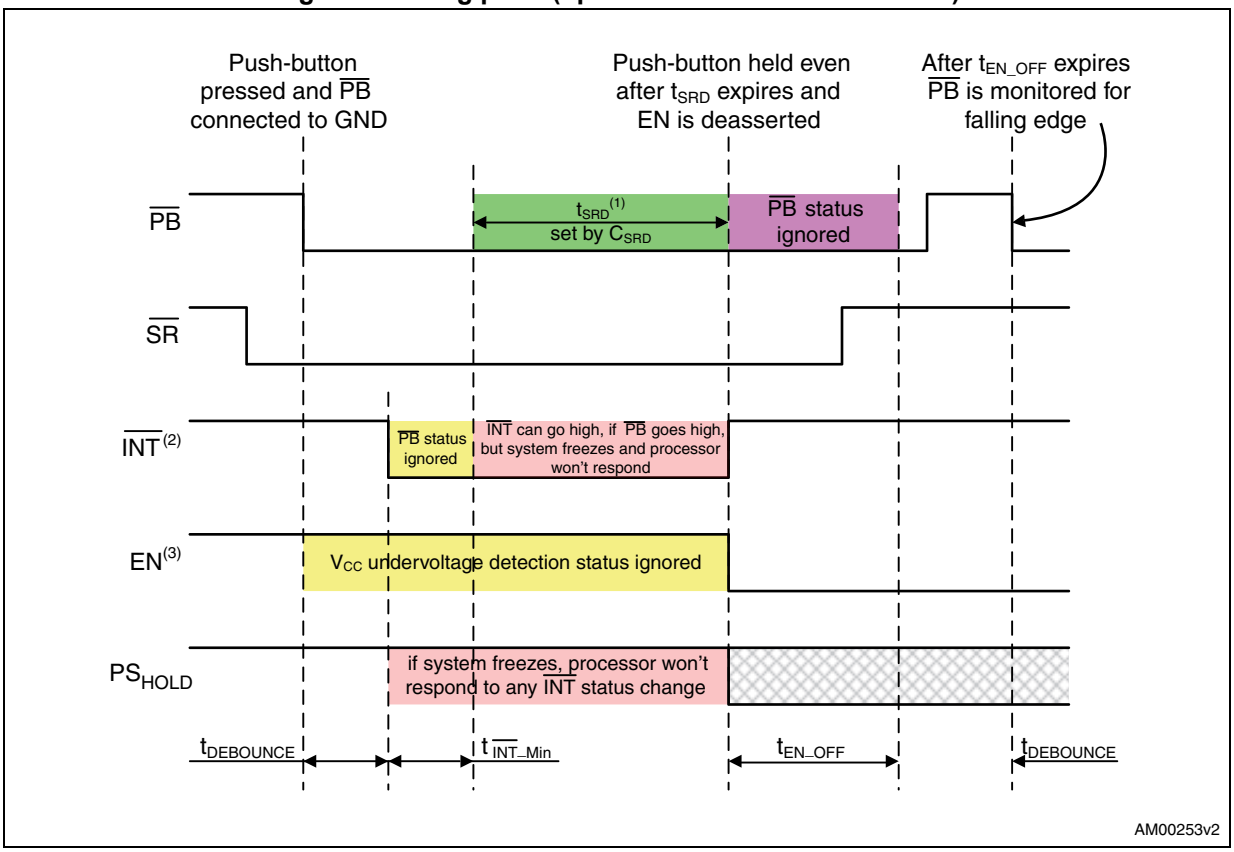


Figure 18. Long push (option with $\overline{RST}$ assertion)



1. t_{SRD} period is set by external capacitor C_{SRD}.
2. $\overline{PB}$ ignored during $t_{\overline{INT}\_Min}$.
3. PS_{HOLD} signal is ignored during t_{ON_BLANK}. Its level is checked after t_{ON_BLANK} expires and if it is high the EN signal remains asserted, otherwise EN goes low.
4. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during startup when device is reset.

Figure 19. Long push (option with enable deassertion)



1. t_{SRD} period is set by external capacitor C_{SRD}.
2. $\overline{PB}$ ignored during $t_{\overline{INT}\_Min}$.
3. After t_{SRD} expires EN is forced low.