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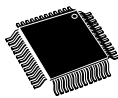


Automotive 8-bit ultra-low-power MCU, up to 32 Kbyte Flash, RTC, data EEPROM, LCD, timers, USART, I2C, SPI, ADC, DAC, COMPs

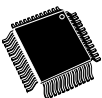
Datasheet production data

Features




- AEC-Q100 qualified
 - Operating conditions
 - Operating power supply range 1.8 V to 3.6 V (down to 1.65 V at power down)
 - Temperature range: - 40 °C to 85 or 125 °C
 - Low power features
 - Five low-power modes: Wait, low-power run (5.1 µA), low-power wait (3 µA), active-halt with full RTC (1.3 µA), halt with PDR (400 nA)
 - Run from Flash: 195 µA/MHz + 440 µA
 - Run from RAM: 90 µA/MHz + 400 µA
 - Ultra-low leakage per I/O: 50 nA
 - Fast wakeup from Halt: 4.7 µs
 - Advanced STM8 core
 - Harvard architecture and 3-stage pipeline
 - Max freq. 16 MHz, 16 CISC MIPS peak
 - Up to 40 external interrupt sources
 - Reset and supply management
 - Low power, ultra safe BOR reset with 5 selectable thresholds
 - Ultra-low power POR/PDR
 - Programmable voltage detector (PVD)
 - Clock management
 - 1 to 16 MHz crystal oscillator
 - 32 kHz crystal oscillator
 - Internal 16 MHz factory-trimmed RC
 - Internal 38 kHz low consumption RC
 - Clock security system
 - Low power RTC
 - BCD calendar with alarm interrupt
 - Auto-wakeup from Halt (0.95 ppm resolution) w/ periodic interrupt
 - LCD: up to 4x28 segments w/ step-up converter
- 

LQFP48
7 x 7 mm



LQFP32
7 x 7 mm



VFQFPN32
5 x 5 mm
- Memories
 - Program memory: up to 32 Kbyte Flash program; data retention 20 years at 55 °C
 - Data memory: up to 1 Kbyte true data EEPROM; endurance 300 kcycle
 - RAM: up to 2 Kbyte
 - DMA
 - Four channels; supported peripherals: ADC, DAC, SPI, I2C, USART, timers
 - One channel for memory-to-memory
 - 12-bit DAC with output buffer
 - 12-bit ADC up to 1 Mbps/25 channels
 - Temp sensor and internal reference voltage
 - Two ultra-low-power comparators
 - One with fixed threshold and one rail to rail
 - Wakeup capability
 - Timers
 - Two 16-bit timers with two channels (used as IC, OC, PWM), quadrature encoder
 - One 16-bit advanced control timer with three channels, supporting motor control
 - One 8-bit timer with 7-bit prescaler
 - Two watchdogs: one window, one independent
 - Beeper timer with 1-, 2- or 4 kHz frequencies
 - Communication interfaces
 - Synchronous serial interface (SPI)
 - Fast I2C 400 kHz SMBus and PMBus
 - USART (ISO 7816 interface, IrDA, LIN 1.3, LIN 2.0)
 - Up to 41 I/Os, all mappable on interrupt vectors

- Development support
 - Fast on-chip programming and non intrusive debugging with SWIM
 - Bootloader using USART
- 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM8AL313x/4x/6x (without LCD)	STM8AL3136, STM8AL3138, STM8AL3146, STM8AL3148, STM8AL3166, STM8AL3168
STM8AL3L4x/6x (with LCD)	STM8AL3L46, STM8AL3L48, STM8AL3L66, STM8AL3L68

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1 Introduction

This document describes the features, pinout, mechanical data and ordering information of the medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x devices (microcontrollers with up to 32-Kbyte Flash memory density). These devices are referred to as medium-density devices in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031) and in STM8L and STM8AL Flash programming manual (PM0054).

For more details on the whole STMicroelectronics ultra-low-power family please refer to [Section 3: Functional overview on page 13](#).

For information on the debug module and SWIM (single wire interface module), refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).

For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

Note: The medium-density devices provide the following benefits:

- Integrated system
 - Up to 32 Kbytes of medium-density embedded Flash program memory
 - 1 Kbytes of data EEPROM
 - Internal high speed and low-power low speed RC.
 - Embedded reset
- Ultra-low power consumption
 - 195 $\mu\text{A}/\text{MHZ}$ + 440 μA (consumption)
 - 0.9 μA with LSI in Active-halt mode
 - Clock gated system and optimized power management
 - Capability to execute from RAM for Low power wait mode and Low power run mode
- Advanced features
 - Up to 16 MIPS at 16 MHz CPU clock frequency
 - Direct memory access (DMA) for memory-to-memory or peripheral-to-memory access.
- Short development cycles
 - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals.
 - Wide choice of development tools

All devices offer 12-bit ADC, DAC, two comparators, Real-time clock three 16-bit timers, one 8-bit timer as well as standard communication interface such as SPI, I2C and USART. A 4x28-segment LCD is available on the medium-density STM8AL3Lxx line. [Table 2: Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x low-power device features and peripheral counts](#) and [Section 3: Functional overview](#) give an overview of the complete range of peripherals proposed in this family.

[Figure 1](#) shows the general block diagram of the device family.

2 Description

The medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x devices are members of the STM8AL automotive ultra-low-power 8-bit family. The medium-density STM8AL3xxx family operates from 1.8 V to 3.6 V (down to 1.65 V at power down) and is available in the -40 to +85°C and -40 to +125°C temperature ranges.

The medium-density STM8AL3xxx ultra-low-power family features the enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive In-Application debugging and ultrafast Flash programming.

All medium-density STM8AL3xxx microcontrollers feature embedded data EEPROM and low power low-voltage single-supply program Flash memory.

They incorporate an extensive range of enhanced I/Os and peripherals.

The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

Two different packages are proposed which include 32 and 48 pins. Depending on the device chosen, different sets of peripherals are included.

All STM8AL3xxx ultra-low-power products are based on the same architecture with the same memory mapping and a coherent pinout.

2.1 Device overview

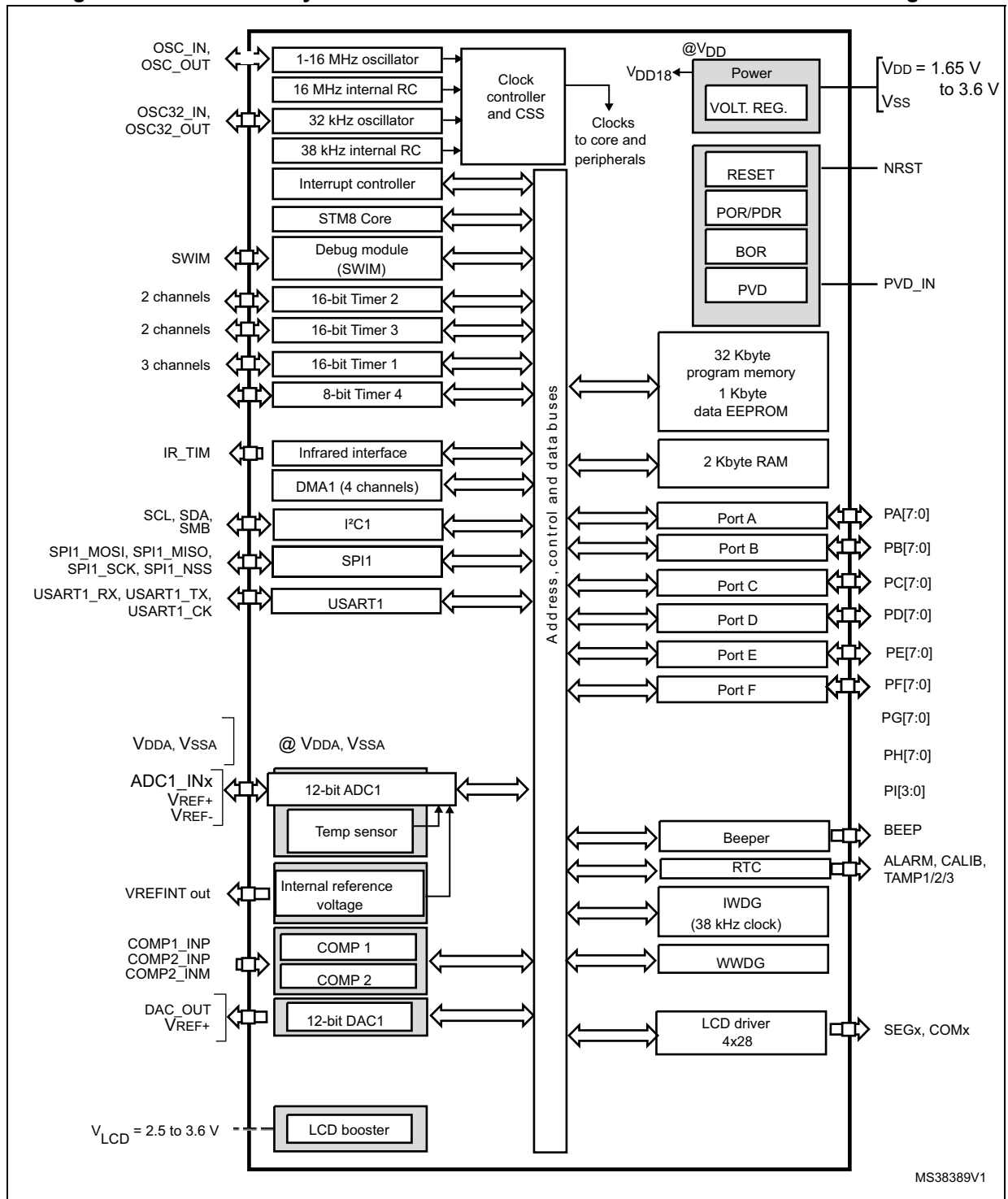
Table 2. Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x low-power device features and peripheral counts

Features		STM8AL3xx6			STM8AL3xx8		
		8	16	32	8	16	32
Flash (Kbyte)		8	16	32	8	16	32
Data EEPROM (Kbyte)		1					
RAM-Kbyte		2			2		
LCD		4x17 ⁽¹⁾			4x28 ⁽¹⁾		
Timers	Basic	1 (8-bit)			1 (8-bit)		
	General purpose	2 (16-bit)			2 (16-bit)		
	Advanced control	1 (16-bit)			1 (16-bit)		
Communication interfaces	SPI	1			1		
	I2C	1			1		
	USART	1			1		
GPIOs		30 ⁽²⁾⁽³⁾ or 29 ⁽¹⁾⁽³⁾			41 ⁽³⁾		
12-bit synchronized ADC (number of channels)		1 (22 ⁽²⁾ or 21 ⁽¹⁾)			1 (25)		
12-Bit DAC (number of channels)		1 (1)			1 (1)		
Comparators COMP1/COMP2		2			2		
Others		RTC, window watchdog, independent watchdog, 16-MHz and 38-kHz internal RC, 1- to 16-MHz and 32-kHz external oscillator					
CPU frequency		16 MHz					
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power down)					
Operating temperature		-40 to +85 °C/-40 to +125 °C					
Packages		LQFP32 (7 x7 mm) VFQFPN32 (5 x 5 mm)			LQFP48 (7x7) VFQFPN32 (5 x 5 mm)		

1. STM8AL3Lxx versions only
2. STM8AL31xx versions only
3. The number of GPIOs given in this table includes the NRST/PA1 pin but the application can use the NRST/PA1 pin as general purpose output only (PA1).

3 Functional overview

Figure 1. Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x device block diagram



- Legend:** ADC (Analog-to-digital converter), BOR (Brownout reset), DMA (Direct memory access), DAC (Digital-to-analog converter), I²C (Inter-integrated circuit multimaster interface), IWDG (Independent watchdog), LCD (Liquid crystal display), POR/PDR (Power on reset / power down reset), RTC (Real-time clock), SPI (Serial peripheral interface), SWIM (Single wire interface module), USART (Universal synchronous asynchronous receiver transmitter), WWDG (Window watchdog).

3.1 Low-power modes

The medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x devices support five low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Wait mode:** CPU clock is stopped, but selected peripherals keep running. An internal or external interrupt, event or a Reset can be used to exit the microcontroller from Wait mode (WFE or WFI mode). Wait consumption: refer to [Table 22](#).
- **Low power run mode:** The CPU and the selected peripherals are running. Execution is done from RAM with a low speed oscillator (LSI or LSE). Flash and data EEPROM are stopped and the voltage regulator is configured in ultra-low-power mode. The microcontroller enters Low power run mode by software and can exit from this mode by software or by a reset.
All interrupts must be masked. They cannot be used to exit the microcontroller from this mode. Low power run mode consumption: refer to [Table 23](#).
- **Low power wait mode:** This mode is entered when executing a Wait for event in Low power run mode. It is similar to Low power run mode except that the CPU clock is stopped. The wakeup from this mode is triggered by a Reset or by an internal or external event (peripheral event generated by the timers, serial interfaces, DMA controller (DMA1), comparators and I/O ports). When the wakeup is triggered by an event, the system goes back to Low power run mode.
All interrupts must be masked. They cannot be used to exit the microcontroller from this mode. Low power wait mode consumption: refer to [Table 24](#).
- **Active-halt mode:** CPU and peripheral clocks are stopped, except RTC. The wakeup can be triggered by RTC interrupts, external interrupts or reset. Active-halt consumption: refer to [Table 25](#) and [Table 26](#).
- **Halt mode:** CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. The wakeup is triggered by an external interrupt or reset. A few peripherals have also a wakeup from Halt capability. Switching off the internal reference voltage reduces power consumption. Through software configuration it is also possible to wake up the device without waiting for the internal reference voltage wakeup time to have a fast wakeup time of 5 μ s. Halt consumption: refer to [Table 27](#).

3.2 Central processing unit STM8

3.2.1 Advanced STM8 core

The 8-bit STM8 core is designed for code efficiency and performance with an Harvard architecture and a 3-stage pipeline.

It contains six internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing, and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16 Mbyte linear memory space
- 16-bit stack pointer - access to a 64 Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

3.2.2 Interrupt controller

The medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x feature a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 32 interrupt vectors with hardware priority
- Up to 40 external interrupt sources on 11 vectors
- Trap and reset interrupts

3.3 Reset and supply management

3.3.1 Power supply scheme

The STM8AL313x/4x/6x and STM8AL3L4x/6x require a 1.65 V to 3.6 V operating supply voltage (V_{DD}). The external power supply pins must be connected as follows:

- V_{SS1} ; V_{DD1} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supply for I/Os and for the internal regulator. Provided externally through V_{DD1} pins, the corresponding ground pin is V_{SS1} .
- V_{SSA} ; V_{DDA} = 1.8 V to 3.6 V, down to 1.65 V at power down: external power supplies for analog peripherals (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC1 is used). V_{DDA} and V_{SSA} must be connected to V_{DD1} and V_{SS1} , respectively.
- V_{SS2} ; V_{DD2} = 1.8 V to 3.6 V, down to 1.65 V at power down: external power supplies for I/Os. V_{DD2} and V_{SS2} must be connected to V_{DD1} and V_{SS1} , respectively.
- V_{REF+} ; V_{REF-} (for ADC1): external reference voltage for ADC1. Must be provided externally through V_{REF+} and V_{REF-} pin.
- V_{REF+} (for DAC): external voltage reference for DAC must be provided externally through V_{REF+} .

3.3.2 Power supply supervisor

The STM8AL313x/4x/6x and STM8AL3L4x/6x have an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR), coupled with a brownout reset (BOR) circuitry. At power-on, BOR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently (in which case, the V_{DD} min value at power down is 1.65 V).

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Halt mode, it is possible to automatically switch off the internal reference voltage (and consequently the BOR) in Halt mode. The device remains under reset when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for any external reset circuit.

The STM8AL313x/4x/6x and STM8AL3L4x/6x feature an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x embed an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals.

This regulator has two different modes:

- Main voltage regulator mode (MVR) for Run, Wait for interrupt (WFI) and Wait for event (WFE) modes.
- Low power voltage regulator mode (LPVR) for Halt, Active-halt, Low power run and Low power wait modes.

When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption.

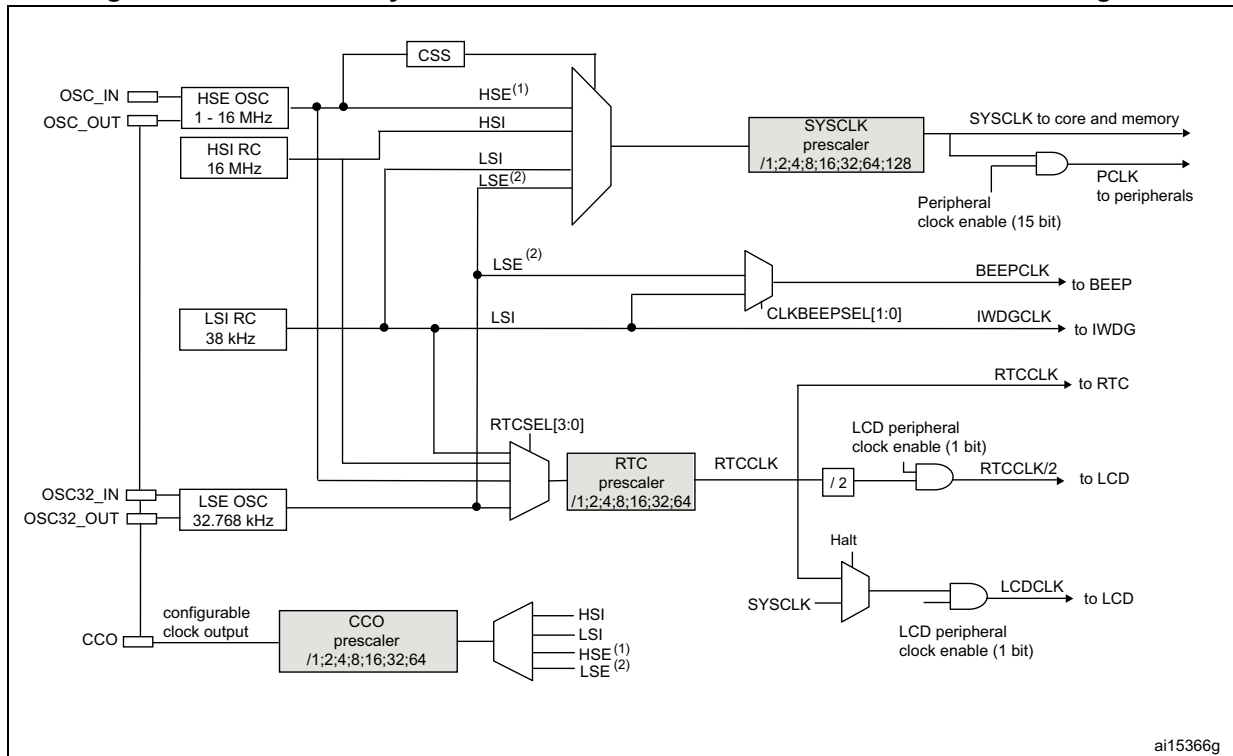
3.4 Clock management

The clock controller distributes the system clock (SYSCLK) coming from different oscillators to the core and the peripherals. It also manages the clock gating for low-power modes and ensures clock robustness.

Features

- **Clock prescaler:** to get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching:** the clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock sources:** four different clock sources can be used to drive the system clock:
 - 1-16 MHz High speed external crystal (HSE),
 - 16 MHz High speed internal RC oscillator (HSI),
 - 32.768 kHz Low speed external crystal (LSE),
 - 38 kHz Low speed internal RC (LSI).
- **RTC and LCD clock sources:** the above four sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If a HSE clock failure occurs, the system clock is automatically switched to HSI.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

Figure 2. Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x clock tree diagram



1. The HSE clock source can be either an external crystal/ceramic resonator or an external source (HSE bypass). Refer to *Section HSE clock* in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).
2. The LSE clock source can be either an external crystal/ceramic resonator or an external source (LSE bypass). Refer to *Section LSE clock* in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).

3.5 Low power real-time clock

The real-time clock (RTC) is an independent binary coded decimal (BCD) timer/counter.

Six byte locations contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day months are made automatically.

It provides a programmable alarm and programmable periodic interrupts with wakeup from Halt capability.

- Periodic wakeup time using the 32.768 kHz LSE with the lowest resolution (of 61 μs) is from min. 122 μs to max. 3.9 s. With a different resolution, the wakeup time can reach 36 hours.
- Periodic alarms based on the calendar can also be generated from every second to every year.

3.6 LCD (Liquid crystal display)

The liquid crystal display drives up to four common terminals and up to 28 segment terminals to drive up to 112 pixels.

- Internal step-up converter to guarantee contrast control whatever V_{DD} .
- Static 1/2, 1/3, 1/4 duty supported.
- Static 1/2, 1/3 bias supported.
- Phase inversion to reduce power consumption and EMI.
- Up to 4 pixels which can be programmed to blink.
- The LCD controller can operate in Halt mode.

Note: Unnecessary segments and common pins can be used as general I/O pins.

3.7 Memories

The medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x devices have the following main features:

- Up to 2 Kbytes of RAM
- The non-volatile memory is divided into three arrays:
 - Up to 32 Kbytes of medium-density embedded Flash program memory
 - 1 Kbytes of Data EEPROM
 - Option bytes.

It supports the read-while-write (RWW): it is possible to execute the code from the program matrix while programming/erasing the data matrix.

The option byte protects part of the Flash program memory from write and readout piracy.

3.8 DMA

A 4-channel direct memory access controller (DMA1) offers a memory-to-memory and peripherals-from/to-memory transfer capability. The 4 channels are shared between the following IPs with DMA capability: ADC1, DAC, I2C1, SPI1, USART1, the 4 Timers.

3.9 Analog-to-digital converter

- 12-bit analog-to-digital converter (ADC1) with 25 channels (including 1 fast channel), temperature sensor and internal reference voltage
- Conversion time down to 1 μ s with $f_{SYSCLK} = 16$ MHz
- Programmable resolution
- Programmable sampling time
- Single and continuous mode of conversion
- Scan capability: automatic conversion performed on a selected group of analog inputs
- Analog watchdog
- Triggered by timer

Note: ADC1 can be served by DMA1.

3.10 Digital-to-analog converter (DAC)

- 12-bit DAC with output buffer
- Synchronized update capability using TIM4
- DMA capability
- External triggers for conversion
- Input reference voltage V_{REF+} for better resolution

Note: DAC can be served by DMA1.

3.11 Ultra-low-power comparators

The medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x embed two comparators (COMP1 and COMP2) that share the same current bias and voltage reference. The voltage reference can be internal or external (coming from an I/O).

- One comparator with fixed threshold (COMP1).
- One comparator rail to rail with fast or slow mode (COMP2). The threshold can be one of the following:
 - DAC output,
 - External I/O,
 - Internal reference voltage or internal reference voltage sub multiple (1/4, 1/2, 3/4).

The two comparators can be used together to offer a window function. They can wake up from Halt mode.

3.12 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM4 and ADC1 DMA channels can also be remapped.

The highly flexible routing interface allows application software to control the routing of different I/Os to the TIM1 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1, COMP2, DAC and the internal reference voltage V_{REFINT} . It also provides a set of registers for efficiently managing the charge transfer acquisition sequence (see [Section 3.13: Timers](#)).

3.13 Timers

The medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x devices contain one advanced control timer (TIM1), two 16-bit general purpose timers (TIM2 and TIM3) and one 8-bit basic timer (TIM4).

All the timers can be served by DMA1.

[Table 3](#) compares the features of the advanced control, general-purpose and basic timers.

Table 3. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA1 request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	up/down	Any integer from 1 to 65536	Yes	3 + 1	3
TIM2			Any power of 2 from 1 to 128		2	None
TIM3					0	
TIM4	8-bit	up	Any power of 2 from 1 to 32768			

3.13.1 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver.

- 16-bit up, down and up/down auto reload counter with 16-bit prescaler
- Three independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output.
- One additional capture/compare channel which is not connected to an external I/O
- Synchronization module to control the timer with external signals
- Break input to force timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)

3.13.2 16-bit general purpose timers

- 16-bit auto reload (AR) up/down-counter
- 7-bit prescaler adjustable to fixed power of 2 ratios (1...128)
- Two individually configurable capture/compare channels
- PWM mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)
- Synchronization with other timers or external signals (external clock, reset, trigger and enable)

3.13.3 8-bit basic timer

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. It can be used for timebase generation with interrupt generation on timer overflow or for DAC trigger generation.

3.14 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

3.14.1 Window watchdog timer

The window watchdog (WWDG) is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

3.14.2 Independent watchdog timer

The independent watchdog peripheral (IWDG) can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the internal LSI RC clock source, and thus stays active even in case of a CPU clock failure.

3.15 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

3.16 Communication interfaces

3.16.1 SPI

The serial peripheral interface (SPI1) provides half/ full duplex synchronous serial communication with external devices.

- Maximum speed: 8 Mbit/s ($f_{\text{SYSCLK}}/2$) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- Hardware CRC calculation
- Slave/master selection input pin

Note: SPI1 can be served by the DMA1 Controller.

3.16.2 I²C

The I²C bus interface (I²C1) provides multi-master capability, and controls all I²C bus-specific sequencing, protocol, arbitration and timing.

- Master, slave and multi-master capability
- Standard mode up to 100 kHz and fast speed modes up to 400 kHz
- 7-bit and 10-bit addressing modes
- SMBus 2.0 and PMBus support
- Hardware CRC calculation

Note: I²C1 can be served by the DMA1 Controller.

3.16.3 USART

The USART interface (USART1) allows full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

- 1 Mbit/s full duplex SCI
- SPI1 emulation
- High precision baud rate generator
- SmartCard emulation
- IrDA SIR encoder decoder
- Single wire half duplex mode

Note: USART1 can be served by the DMA1 Controller.

USART1 can be used to implement LIN slave communication, with LIN Break detection on the framing error flag (FE in USART_SR register) with a value of 0 in the USART data register (USART_DR).

3.17 Infrared (IR) interface

The medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x devices contain an infrared interface which can be used with an IR LED for remote control functions. Two timer output compare channels are used to generate the infrared remote control signals.

3.18 Development support

Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment.
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

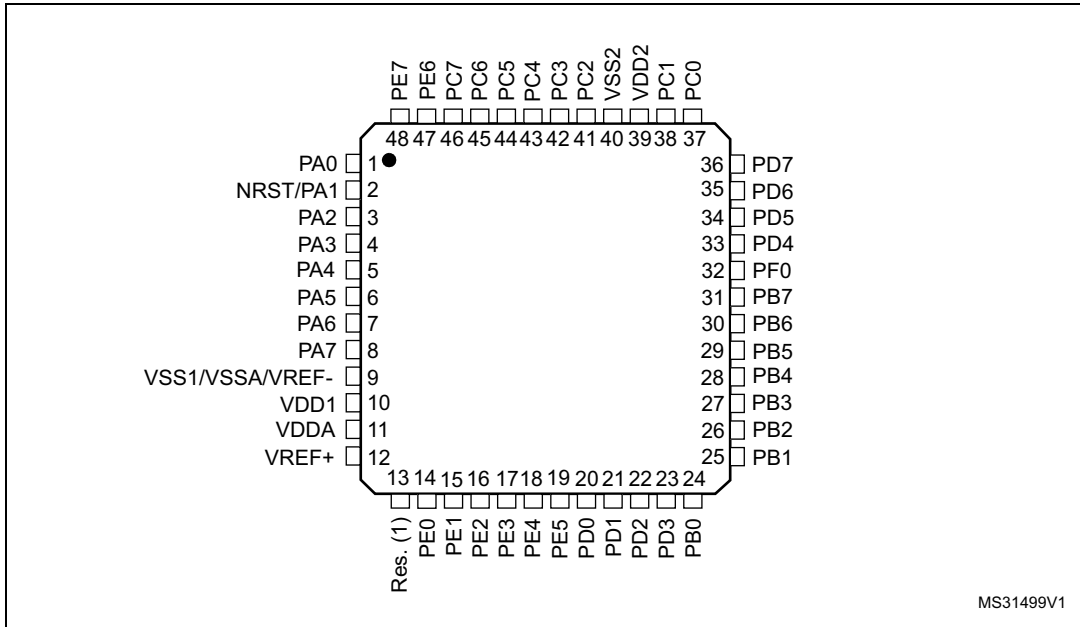
The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, CPU operation can also be monitored in real-time by means of shadow registers.

Bootloader

A bootloader is available to reprogram the Flash memory using the USART1 interface. The reference document for the bootloader is *UM0560: STM8 bootloader user manual*.

4 Pin description

Figure 3. STM8AL31x8T 48-pin pinout (without LCD)



1. Reserved. Must be tied to V_{DD}.

Figure 4. STM8AL3Lx8T 48-pin pinout (with LCD)

