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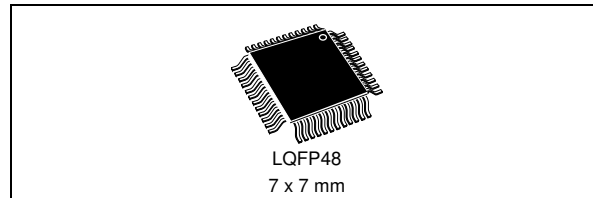


## Value Line, 8-bit ultra-low-power MCU, 32-KB Flash, 256-byte data EEPROM, RTC, LCD, timers, USART, I2C, SPI, ADC

Datasheet - production data

### Features

- Operating conditions
  - Operating power supply: 1.8 V to 3.6 V
  - Temperature range: -40 °C to 85 °C
- Low-power features
  - Five low-power modes: Wait, Low-power run (5.1  $\mu$ A), Low-power wait (3  $\mu$ A), Active-halt with full RTC (1.3  $\mu$ A), Halt (350 nA)
  - Consumption: 195  $\mu$ A/MHz + 440  $\mu$ A
  - Ultra-low leakage per I/O: 50 nA
  - Fast wakeup from Halt: 4.7  $\mu$ s
- Advanced STM8 core
  - Harvard architecture and 3-stage pipeline
  - Max freq. 16 MHz, 16 CISC MIPS peak
  - Up to 40 external interrupt sources
- Reset and supply management
  - Low-power, ultra-safe BOR reset with five selectable thresholds
  - Ultra-low-power POR/PDR
  - Programmable voltage detector (PVD)
- Clock management
  - 32 kHz and 1 to 16 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC
  - Internal 38 kHz low consumption RC
  - Clock security system
- Low-power RTC
  - BCD calendar with alarm interrupt
  - Auto-wakeup from Halt w/ periodic interrupt
- LCD: up to 4x28 segments w/ step-up converter
- Memories
  - 32 KB Flash program memory and 256 bytes data EEPROM with ECC, RWW
  - Flexible write and read protection modes
  - 2 Kbytes of RAM



- DMA
  - Four channels supporting ADC, SPI, I2C, USART, timers
  - One channel for memory-to-memory
- 12-bit ADC up to 1 Msps/25 channels
  - Internal reference voltage
- Timers
  - Two 16-bit timers with two channels (used as IC, OC, PWM), quadrature encoder
  - One 16-bit advanced control timer with three channels, supporting motor control
  - One 8-bit timer with 7-bit prescaler
  - Two watchdogs: one Window, one Independent
  - Beeper timer with 1-, 2- or 4-kHz frequencies
- Communication interfaces
  - Synchronous serial interface (SPI)
  - Fast I<sup>2</sup>C 400 kHz SMBus and PMBus
  - USART (ISO 7816 interface and IrDA)
- Up to 41 I/Os, all mappable on interrupt vectors
- Development support
  - Fast on-chip programming and non-intrusive debugging with SWIM
  - Bootloader using USART

# Contents

<b>1</b>	<b>Introduction</b>	<b>8</b>
<b>2</b>	<b>Description</b>	<b>9</b>
2.1	Device overview	10
2.2	Ultra-low-power continuum	11
<b>3</b>	<b>Functional overview</b>	<b>12</b>
3.1	Low-power modes	13
3.2	Central processing unit STM8	14
3.2.1	Advanced STM8 core	14
3.2.2	Interrupt controller	14
3.3	Reset and supply management	15
3.3.1	Power supply scheme	15
3.3.2	Power supply supervisor	15
3.3.3	Voltage regulator	15
3.4	Clock management	16
3.5	Low-power real-time clock	17
3.6	LCD (Liquid crystal display)	18
3.7	Memories	18
3.8	DMA	18
3.9	Analog-to-digital converter	19
3.10	System configuration controller and routing interface	19
3.11	Timers	19
3.11.1	TIM1 - 16-bit advanced control timer	20
3.11.2	16-bit general purpose timers	20
3.11.3	8-bit basic timer	20
3.12	Watchdog timers	20
3.12.1	Window watchdog timer	20
3.12.2	Independent watchdog timer	20
3.13	Beeper	21
3.14	Communication interfaces	21
3.14.1	SPI	21
3.14.2	I <sup>2</sup> C	21

3.14.3	USART	21
3.15	Infrared (IR) interface	22
3.16	Development support	22
<b>4</b>	<b>Pin description</b>	<b>23</b>
4.1	System configuration options	28
<b>5</b>	<b>Memory and register map</b>	<b>29</b>
5.1	Memory mapping	29
5.2	Register map	30
<b>6</b>	<b>Interrupt vector mapping</b>	<b>47</b>
<b>7</b>	<b>Option bytes</b>	<b>49</b>
<b>8</b>	<b>Electrical parameters</b>	<b>52</b>
8.1	Parameter conditions	52
8.1.1	Minimum and maximum values	52
8.1.2	Typical values	52
8.1.3	Typical curves	52
8.1.4	Loading capacitor	52
8.1.5	Pin input voltage	53
8.2	Absolute maximum ratings	53
8.3	Operating conditions	55
8.3.1	General operating conditions	55
8.3.2	Embedded reset and power control block characteristics	56
8.3.3	Supply current characteristics	57
8.3.4	Clock and timing characteristics	68
8.3.5	Memory characteristics	73
8.3.6	I/O current injection characteristics	73
8.3.7	I/O port pin characteristics	74
8.3.8	Communication interfaces	82
8.3.9	LCD controller	87
8.3.10	Embedded reference voltage	88
8.3.11	12-bit ADC1 characteristics	89
8.3.12	EMC characteristics	95

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<b>9</b>	<b>Package information</b> .....	<b>98</b>
	9.1 LQFP48 package information .....	98
<b>10</b>	<b>Part numbering</b> .....	<b>101</b>
<b>11</b>	<b>Revision history</b> .....	<b>102</b>

## List of tables

Table 1.	Medium-density value line STM8L052C6 low-power device features and peripheral counts	10
Table 2.	Timer feature comparison	19
Table 3.	Legend/abbreviation for <a href="#">Table 4</a>	23
Table 4.	Medium-density value line STM8L052C6 pin description	23
Table 5.	Flash and RAM boundary addresses	30
Table 6.	I/O port hardware register map	30
Table 7.	General hardware register map	31
Table 8.	CPU/SWIM/debug module/interrupt controller registers	45
Table 9.	Interrupt mapping	47
Table 10.	Option byte addresses	49
Table 11.	Option byte description	50
Table 12.	Voltage characteristics	53
Table 13.	Current characteristics	54
Table 14.	Thermal characteristics	54
Table 15.	General operating conditions	55
Table 16.	Embedded reset and power control block characteristics	56
Table 17.	Total current consumption in Run mode	58
Table 18.	Total current consumption in Wait mode	60
Table 19.	Total current consumption and timing in Low power run mode at VDD = 1.8 V to 3.6 V	62
Table 20.	Total current consumption in Low power wait mode at VDD = 1.8 V to 3.6 V	63
Table 21.	Total current consumption and timing in Active-halt mode at VDD = 1.8 V to 3.6 V	64
Table 22.	Typical current consumption in Active-halt mode, RTC clocked by LSE external crystal	65
Table 23.	Total current consumption and timing in Halt mode at VDD = 1.8 to 3.6 V	66
Table 24.	Peripheral current consumption	67
Table 25.	Current consumption under external reset	67
Table 26.	HSE external clock characteristics	68
Table 27.	LSE external clock characteristics	68
Table 28.	HSE oscillator characteristics	69
Table 29.	LSE oscillator characteristics	70
Table 30.	HSI oscillator characteristics	71
Table 31.	LSI oscillator characteristics	72
Table 32.	RAM and hardware registers	73
Table 33.	Flash program and data EEPROM memory	73
Table 34.	I/O current injection susceptibility	74
Table 35.	I/O static characteristics	75
Table 36.	Output driving current (high sink ports)	78
Table 37.	Output driving current (true open drain ports)	78
Table 38.	Output driving current (PA0 with high sink LED driver capability)	78
Table 39.	NRST pin characteristics	80
Table 40.	SPI1 characteristics	82
Table 41.	I <sup>2</sup> C characteristics	85
Table 42.	LCD characteristics	87
Table 43.	Reference voltage characteristics	88
Table 44.	ADC1 characteristics	89
Table 45.	ADC1 accuracy with VDDA = 3.3 V to 2.5 V	91
Table 46.	ADC1 accuracy with VDDA = 2.4 V to 3.6 V	91

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Table 47.	ADC1 accuracy with $VDDA = VREF_+ = 1.8\text{ V to }2.4\text{ V}$ . . . . .	91
Table 48.	$R_{AIN}$ max for $f_{ADC} = 16\text{ MHz}$ . . . . .	93
Table 49.	EMS data . . . . .	95
Table 50.	EMI data . . . . .	96
Table 51.	ESD absolute maximum ratings . . . . .	96
Table 52.	Electrical sensitivities . . . . .	97
Table 53.	LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data. . . . .	99
Table 54.	Ordering information scheme . . . . .	101
Table 55.	Document revision history . . . . .	102

## List of figures

Figure 1.	Medium-density value line STM8L052C6 device block diagram	12
Figure 2.	Medium-density value line STM8L052C6 clock tree diagram	17
Figure 3.	STM8L052C6 48-pin LQFP48 package pinout (with LCD)	23
Figure 4.	Memory map	29
Figure 5.	Pin loading conditions	52
Figure 6.	Pin input voltage	53
Figure 7.	POR/BOR thresholds	57
Figure 8.	Typ. $I_{DD}(RUN)$ vs. $V_{DD}$ , $f_{CPU} = 16$ MHz	59
Figure 9.	Typ. $I_{DD}(Wait)$ vs. $V_{DD}$ , $f_{CPU} = 16$ MHz 1)	61
Figure 10.	Typ. $I_{DD}(LPR)$ vs. $V_{DD}$ (LSI clock source)	62
Figure 11.	Typ. $I_{DD}(LPW)$ vs. $V_{DD}$ (LSI clock source)	63
Figure 12.	HSE oscillator circuit diagram	69
Figure 13.	LSE oscillator circuit diagram	70
Figure 14.	Typical HSI frequency vs. $V_{DD}$	71
Figure 15.	Typical LSI frequency vs. $V_{DD}$	72
Figure 16.	Typical $V_{IL}$ and $V_{IH}$ vs. $V_{DD}$ (high sink I/Os)	76
Figure 17.	Typical $V_{IL}$ and $V_{IH}$ vs. $V_{DD}$ (true open drain I/Os)	76
Figure 18.	Typical pull-up resistance $R_{PU}$ vs. $V_{DD}$ with $V_{IN}=V_{SS}$	77
Figure 19.	Typical pull-up current $I_{PU}$ vs. $V_{DD}$ with $V_{IN}=V_{SS}$	77
Figure 20.	Typ. $V_{OL}$ @ $V_{DD} = 3.0$ V (high sink ports)	79
Figure 21.	Typ. $V_{OL}$ @ $V_{DD} = 1.8$ V (high sink ports)	79
Figure 22.	Typ. $V_{OL}$ @ $V_{DD} = 3.0$ V (true open drain ports)	79
Figure 23.	Typ. $V_{OL}$ @ $V_{DD} = 1.8$ V (true open drain ports)	79
Figure 24.	Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 3.0$ V (high sink ports)	79
Figure 25.	Typ. $V_{DD} - V_{OH}$ @ $V_{DD} = 1.8$ V (high sink ports)	79
Figure 26.	Typical NRST pull-up resistance $R_{PU}$ vs. $V_{DD}$	80
Figure 27.	Typical NRST pull-up current $I_{PU}$ vs. $V_{DD}$	81
Figure 28.	Recommended NRST pin configuration	81
Figure 29.	SPI1 timing diagram - slave mode and $CPHA=0$	83
Figure 30.	SPI1 timing diagram - slave mode and $CPHA=1^{(1)}$	83
Figure 31.	SPI1 timing diagram - master mode	84
Figure 32.	Typical application with I2C bus and timing diagram 1)	86
Figure 33.	ADC1 accuracy characteristics	92
Figure 34.	Typical connection diagram using the ADC	92
Figure 35.	Maximum dynamic current consumption on $V_{REF+}$ supply pin during ADC conversion	93
Figure 36.	Power supply and reference decoupling ( $V_{REF+}$ not connected to $V_{DDA}$ )	94
Figure 37.	Power supply and reference decoupling ( $V_{REF+}$ connected to $V_{DDA}$ )	94
Figure 38.	LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline	98
Figure 39.	LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint	100
Figure 40.	LQFP48 marking example (package top view)	100



# 1 Introduction

This document describes the features, pinout, mechanical data and ordering information of the medium-density value line STM8L052C6 microcontroller with 32-Kbyte Flash memory density. For further details on the whole STMicroelectronics medium-density family please refer to [Section 2.2: Ultra-low-power continuum](#).

For detailed information on device operation and registers, refer to the reference manual (RM0031).

For information on to the Flash program memory and data EEPROM, refer to the programming manual (PM0054).

For information on the debug module and SWIM (single wire interface module), refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).

For information on the STM8 core, refer to the STM8 CPU programming manual (PM0044).

Medium density value line devices provide the following benefits:

- Integrated system
  - 32 Kbytes of medium-density embedded Flash program memory
  - 256 bytes of data EEPROM
  - 2 Kbytes of RAM
  - Internal high-speed and low-power low-speed RC
  - Embedded reset
- Ultra-low-power consumption
  - 195  $\mu\text{A}/\text{MHZ}$  + 440  $\mu\text{A}$  (consumption)
  - 0.9  $\mu\text{A}$  with LSI in Active-halt mode
  - Clock gated system and optimized power management
  - Capability to execute from RAM for low-power wait mode and low-power-run mode
- Advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Direct memory access (DMA) for memory-to-memory or peripheral-to-memory access
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals
  - Wide choice of development tools

These features make the value line STM8L05xxx ultra-low-power microcontroller family suitable for a wide range of consumer and mass market applications.

Refer to [Table 1: Medium-density value line STM8L052C6 low-power device features and peripheral counts](#) and [Section 3: Functional overview](#) for an overview of the complete range of peripherals proposed in this family.

[Figure 1](#) shows the block diagram of the medium-density value line STM8L052C6 device.

## 2 Description

The medium-density value line STM8L052C6 devices are members of the STM8L ultra-low-power 8-bit family.

The value line STM8L05xxx ultra-low-power family features the enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive In-application debugging and ultra-fast Flash programming.

Medium-density value line STM8L052C6 microcontrollers feature embedded data EEPROM and low-power, low-voltage, single-supply program Flash memory.

All devices offer 12-bit ADC, real-time clock, 16-bit timers, one 8-bit timer as well as standard communication interface such as SPI, I2C, USART and 4x28-segment LCD. The 4x 28-segment LCD is available on the medium-density value line STM8L052C6.

The STM8L052C6 operates from 1.8 V to 3.6 V and is available in the -40 to +85 °C temperature range.

The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

All value line STM8L ultra-low-power products are based on the same architecture with the same memory mapping and a coherent pinout.

## 2.1 Device overview

**Table 1. Medium-density value line STM8L052C6 low-power device features and peripheral counts**

Features		STM8L052C6
Flash (Kbytes)		32
Data EEPROM (bytes)		256
RAM (Kbytes)		2
LCD		4x28
Timers	Basic	1 (8-bit)
	General purpose	2 (16-bit)
	Advanced control	1 (16-bit)
Communication interfaces	SPI	1
	I2C	1
	USART	1
GPIOs		41 <sup>(1)</sup>
12-bit synchronized ADC (number of channels)		1 (25)
Others		RTC, window watchdog, independent watchdog, 16-MHz and 38-kHz internal RC, 1- to 16-MHz and 32-kHz external oscillator
CPU frequency		16 MHz
Operating voltage		1.8 V to 3.6 V
Operating temperature		-40 to +85 °C
Package		LQFP48

1. The number of GPIOs given in this table includes the NRST/PA1 pin but the application can use the NRST/PA1 pin as general purpose output only (PA1).

## 2.2 Ultra-low-power continuum

The ultra-low-power value line STM8L05xxx and STM8L15xxx are fully pin-to-pin, software and feature compatible. Besides the full compatibility within the STM8L family, the devices are part of STMicroelectronics microcontrollers ultra-low-power strategy which also includes STM8L101xx and STM32L15xxx. The STM8L and STM32L families allow a continuum of performance, peripherals, system architecture, and features.

They are all based on STMicroelectronics 0.13  $\mu\text{m}$  ultra-low leakage process.

- Note:*
- 1 The STM8L05xxx is pin-to-pin compatible with STM8L101xx devices.
  - 2 The STM32L family is pin-to-pin compatible with the general purpose STM32F family. Please refer to STM32L15x documentation for more information on these devices.

### Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM<sup>®</sup> Cortex<sup>®</sup>-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-low-power performance to range from 5 up to 33.3 DMIPs.

### Shared peripherals

STM8L05x, STM8L15x and STM32L15x share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripheral: ADC1
- Digital peripherals: RTC and some communication interfaces

### Common system strategy

To offer flexibility and optimize performance, the STM8L and STM32L devices use a common architecture:

- Same power supply range from 1.8 to 3.6 V
- Architecture optimized to reach ultra-low consumption both in low power modes and Run mode
- Fast startup strategy from low power modes
- Flexible system clock
- Ultra-safe reset: same reset strategy for both STM8L and STM32L including power-on reset, power-down reset, brownout reset and programmable voltage detector

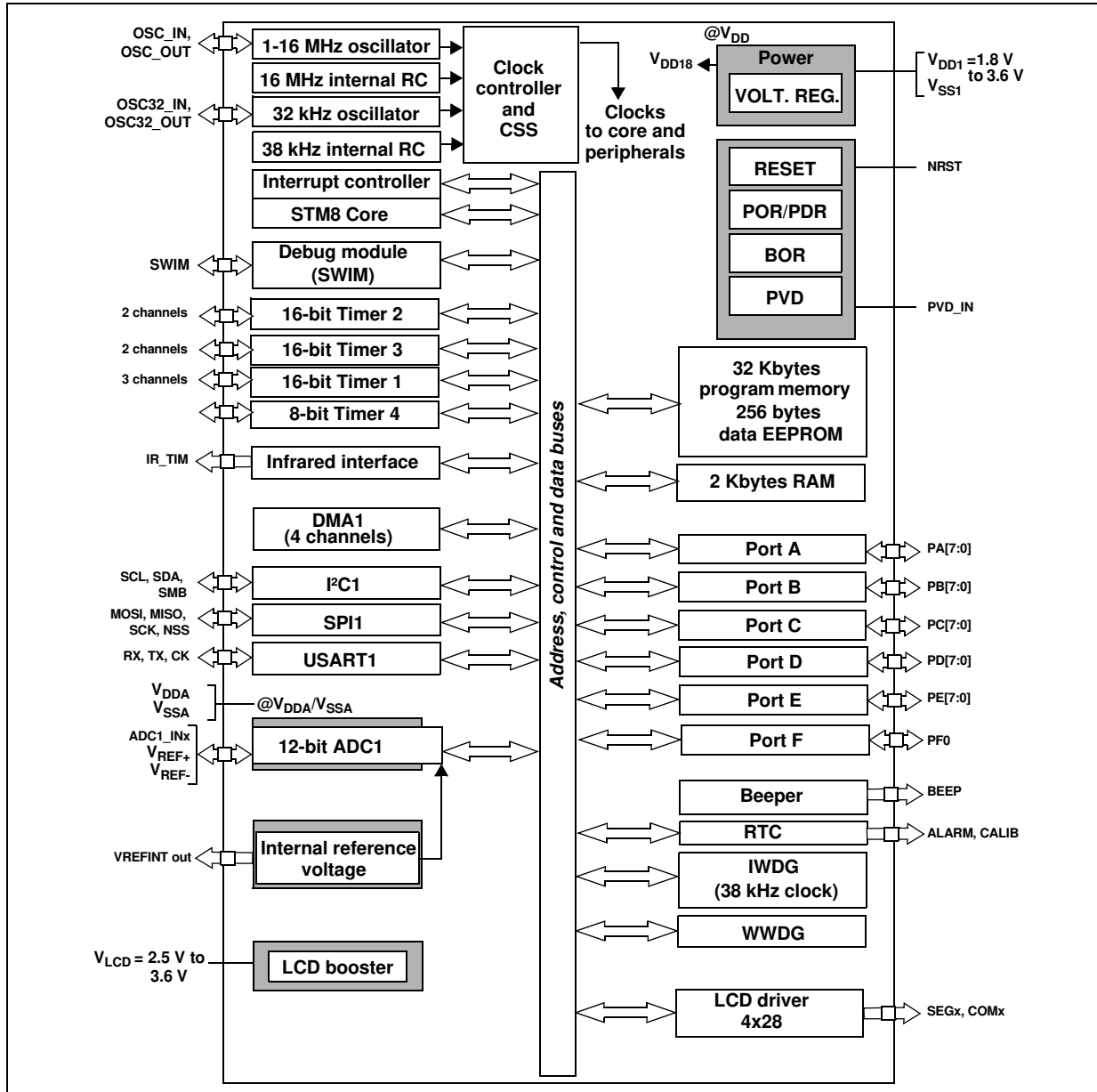
### Features

ST ultra-low-power continuum also lies in feature compatibility:

- More than 10 packages with pin count from 20 to 100 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 128 Kbytes

### 3 Functional overview

Figure 1. Medium-density value line STM8L052C6 device block diagram



- Legend:**  
 ADC: Analog-to-digital converter  
 BOR: Brownout reset  
 DMA: Direct memory access  
 I<sup>2</sup>C: Inter-integrated circuit multimaster interface  
 LCD: Liquid crystal display  
 POR/PDR: Power on reset / power down reset  
 RTC: Real-time clock  
 SPI: Serial peripheral interface  
 SWIM: Single wire interface module  
 USART: Universal synchronous asynchronous receiver transmitter  
 WWDG: Window watchdog  
 IWDG: independent watchdog

## 3.1 Low-power modes

The medium-density value line STM8L052C6 supports five low power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Wait mode:** The CPU clock is stopped, but selected peripherals keep running. An internal or external interrupt, event or a Reset can be used to exit the microcontroller from Wait mode (WFE or WFI mode).
- **Low power run mode:** The CPU and the selected peripherals are running. Execution is done from RAM with a low speed oscillator (LSI or LSE). Flash memory and data EEPROM are stopped and the voltage regulator is configured in ultra-low-power mode. The microcontroller enters Low power run mode by software and can exit from this mode by software or by a reset.  
All interrupts must be masked. They cannot be used to exit the microcontroller from this mode.
- **Low power wait mode:** This mode is entered when executing a Wait for event in Low power run mode. It is similar to Low power run mode except that the CPU clock is stopped. The wakeup from this mode is triggered by a Reset or by an internal or external event (peripheral event generated by the timers, serial interfaces, DMA controller (DMA1) and I/O ports). When the wakeup is triggered by an event, the system goes back to Low power run mode.  
All interrupts must be masked. They cannot be used to exit the microcontroller from this mode.
- **Active-halt mode:** CPU and peripheral clocks are stopped, except RTC. The wakeup can be triggered by RTC interrupts, external interrupts or reset.
- **Halt mode:** CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. The wakeup is triggered by an external interrupt or reset. A few peripherals have also a wakeup from Halt capability. Switching off the internal reference voltage reduces power consumption. Through software configuration it is also possible to wake up the device without waiting for the internal reference voltage wakeup time to have a fast wakeup time of 5  $\mu$ s.

## 3.2 Central processing unit STM8

### 3.2.1 Advanced STM8 core

The 8-bit STM8 core is designed for code efficiency and performance with an Harvard architecture and a 3-stage pipeline.

It contains six internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing, and 80 instructions.

#### Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16-Mbyte linear memory space
- 16-bit stack pointer - access to a 64-Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

#### Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

#### Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

### 3.2.2 Interrupt controller

The medium-density value line STM8L052C6 features a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 32 interrupt vectors with hardware priority
- Up to 40 external interrupt sources on 11 vectors
- Trap and reset interrupts

## 3.3 Reset and supply management

### 3.3.1 Power supply scheme

The device requires a 1.8 V to 3.6 V operating supply voltage ( $V_{DD}$ ). The external power supply pins must be connected as follows:

- $V_{SS1}$  ;  $V_{DD1}$  = 1.8 to 3.6 V: external power supply for I/Os and for the internal regulator. Provided externally through  $V_{DD1}$  pins, the corresponding ground pin is  $V_{SS1}$ .
- $V_{SSA}$  ;  $V_{DDA}$  = 1.8 to 3.6 V: external power supplies for analog peripherals.  $V_{DDA}$  and  $V_{SSA}$  must be connected to  $V_{DD1}$  and  $V_{SS1}$ , respectively.
- $V_{SS2}$  ;  $V_{DD2}$  = 1.8 to 3.6 V: external power supplies for I/Os.  $V_{DD2}$  and  $V_{SS2}$  must be connected to  $V_{DD1}$  and  $V_{SS1}$ , respectively.
- $V_{REF+}$  ;  $V_{REF-}$  (for ADC1): external reference voltage for ADC1. Must be provided externally through  $V_{REF+}$  and  $V_{REF-}$  pin.

### 3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR), coupled with a brownout reset (BOR) circuitry. At power-on, BOR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Halt mode, it is possible to automatically switch off the internal reference voltage (and consequently the BOR) in Halt mode. The device remains under reset when  $V_{DD}$  is below a specified threshold,  $V_{POR/PDR}$  or  $V_{BOR}$ , without the need for any external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the  $V_{DD}/V_{DDA}$  power supply and compares it to the  $V_{PVD}$  threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when  $V_{DD}/V_{DDA}$  drops below the  $V_{PVD}$  threshold and/or when  $V_{DD}/V_{DDA}$  is higher than the  $V_{PVD}$  threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

### 3.3.3 Voltage regulator

The medium-density value line STM8L052C6 embeds an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals.

This regulator has two different modes:

- Main voltage regulator mode (MVR) for Run, Wait for interrupt (WFI) and Wait for event (WFE) modes
- Low power voltage regulator mode (LPVR) for Halt, Active-halt, Low power run and Low power wait modes

When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption.



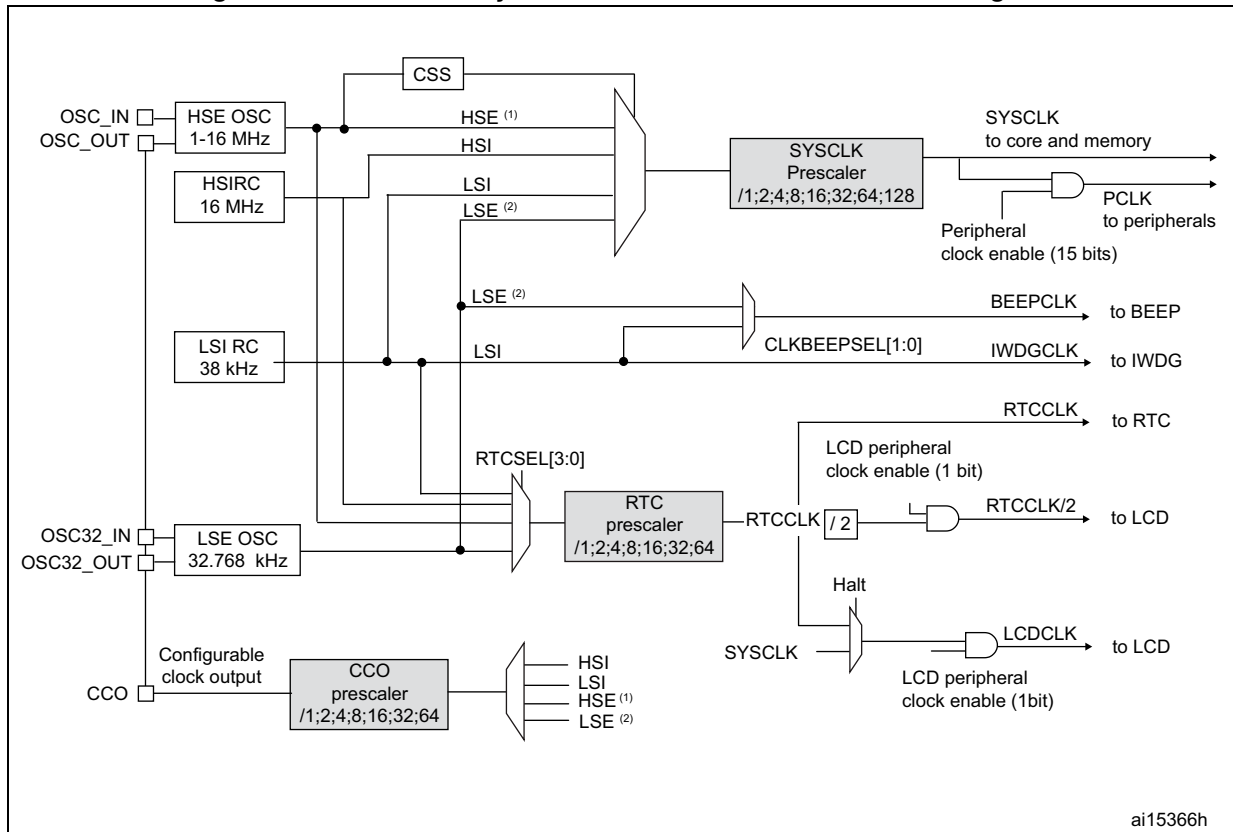
## 3.4 Clock management

The clock controller distributes the system clock (SYSCLK) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

### Features

- **Clock prescaler:** To get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching:** Clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock sources:** 4 different clock sources can be used to drive the system clock:
  - 1-16 MHz High speed external crystal (HSE)
  - 16 MHz High speed internal RC oscillator (HSI)
  - 32.768 kHz Low speed external crystal (LSE)
  - 38 kHz Low speed internal RC (LSI)
- **RTC and LCD clock sources:** The above four sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If a HSE clock failure occurs, the system clock is automatically switched to HSI.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

Figure 2. Medium-density value line STM8L052C6 clock tree diagram



1. The HSE clock source can be either an external crystal/ceramic resonator or an external source (HSE bypass). Refer to *Section HSE clock* in the STM8L15x and STM8L16x reference manual (RM0031).
2. The LSE clock source can be either an external crystal/ceramic resonator or a external source (LSE bypass). Refer to *Section LSE clock* in the STM8L15x and STM8L16x reference manual (RM0031).

### 3.5 Low-power real-time clock

The real-time clock (RTC) is an independent binary coded decimal (BCD) timer/counter.

Six byte locations contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day months are made automatically. It provides a programmable alarm and programmable periodic interrupts with wakeup from Halt capability.

- Periodic wakeup time using the 32.768 kHz LSE with the lowest resolution (of 61 μs) is from min. 122 μs to max. 3.9 s. With a different resolution, the wakeup time can reach 36 hours.
- Periodic alarms based on the calendar can also be generated from every second to every year.

### 3.6 LCD (Liquid crystal display)

The LCD is only available on STM8L052xx devices.

- The liquid crystal display drives up to 4 common terminals and up to 28 segment terminals to drive up to 112 pixels. Internal step-up converter to guarantee contrast control whatever  $V_{DD}$ .
- Static 1/2, 1/3, 1/4 duty supported.
- Static 1/2, 1/3 bias supported.
- Phase inversion to reduce power consumption and EMI.
- Up to 4 pixels which can be programmed to blink.
- The LCD controller can operate in Halt mode.

*Note: Unnecessary segments and common pins can be used as general I/O pins.*

### 3.7 Memories

The medium-density value line STM8L052C6 has the following main features:

- 2 Kbytes of RAM
- The non-volatile memory is divided into three arrays:
  - 32 Kbytes of medium-density embedded Flash program memory
  - 256 bytes of data EEPROM
  - Option bytes

The EEPROM embeds the error correction code (ECC) feature. It supports the read-while-write (RWW): it is possible to execute the code from the program matrix while programming/erasing the data matrix.

The option byte protects part of the Flash program memory from write and readout piracy.

### 3.8 DMA

A 4-channel direct memory access controller (DMA1) offers a memory-to-memory and peripherals-from/to-memory transfer capability. The 4 channels are shared between the following IPs with DMA capability: ADC1, I2C1, SPI1, USART1 and the four timers.

### 3.9 Analog-to-digital converter

- 12-bit analog-to-digital converter (ADC1) with 25 channels (including 1 fast channel) and internal reference voltage
- Conversion time down to 1  $\mu$ s with  $f_{SYSCLK} = 16$  MHz
- Programmable resolution
- Programmable sampling time
- Single and continuous mode of conversion
- Scan capability: automatic conversion performed on a selected group of analog inputs
- Analog watchdog
- Triggered by timer

Note: ADC1 can be served by DMA1.

### 3.10 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM4 and ADC1 DMA channels can also be remapped.

The highly flexible routing interface allows application software to control the routing of different I/Os to the TIM1 timer input captures. It also controls the routing of internal analog signals to ADC1 and the internal reference voltage  $V_{REFINT}$ .

### 3.11 Timers

The medium-density value line STM8L052C6 contains one advanced control timer (TIM1), two 16-bit general purpose timers (TIM2 and TIM3) and one 8-bit basic timer (TIM4).

All the timers can be served by DMA1.

Table 2 compares the features of the advanced control, general-purpose and basic timers.

Table 2. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA1 request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	up/down	Any integer from 1 to 65536	Yes	3 + 1	3
TIM2			Any power of 2 from 1 to 128		2	None
TIM3					0	
TIM4	8-bit	up	Any power of 2 from 1 to 32768			

### 3.11.1 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver.

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- 3 independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- 1 additional capture/compare channel which is not connected to an external I/O
- Synchronization module to control the timer with external signals
- Break input to force timer outputs into a defined state
- 3 complementary outputs with adjustable dead time
- Encoder mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)

### 3.11.2 16-bit general purpose timers

- 16-bit autoreload (AR) up/down-counter
- 7-bit prescaler adjustable to fixed power of 2 ratios (1...128)
- 2 individually configurable capture/compare channels
- PWM mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)
- Synchronization with other timers or external signals (external clock, reset, trigger and enable)

### 3.11.3 8-bit basic timer

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. It can be used for timebase generation with interrupt generation on timer overflow.

## 3.12 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

### 3.12.1 Window watchdog timer

The window watchdog (WWDG) is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

### 3.12.2 Independent watchdog timer

The independent watchdog peripheral (IWDG) can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the internal LSI RC clock source, and thus stays active even in case of a CPU clock failure.

### 3.13 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

## 3.14 Communication interfaces

### 3.14.1 SPI

The serial peripheral interface (SPI1) provides half/ full duplex synchronous serial communication with external devices.

- Maximum speed: 8 Mbit/s ( $f_{\text{SYSCLK}}/2$ ) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- Hardware CRC calculation
- Slave/master selection input pin

*Note:* SPI1 can be served by the DMA1 Controller.

### 3.14.2 I<sup>2</sup>C

The I<sup>2</sup>C bus interface (I<sup>2</sup>C1) provides multi-master capability, and controls all I<sup>2</sup>C bus-specific sequencing, protocol, arbitration and timing.

- Master, slave and multi-master capability
- Standard mode up to 100 kHz and fast speed modes up to 400 kHz
- 7-bit and 10-bit addressing modes
- SMBus 2.0 and PMBus support
- Hardware CRC calculation

*Note:* I<sup>2</sup>C1 can be served by the DMA1 Controller.

### 3.14.3 USART

The USART interface (USART1) allows full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

- 1 Mbit/s full duplex SCI
- SPI1 emulation
- High precision baud rate generator
- SmartCard emulation
- IrDA SIR encoder decoder
- Single wire half duplex mode

*Note:* USART1 can be served by the DMA1 Controller.

### 3.15 Infrared (IR) interface

The medium-density value line STM8L052C6 contains an infrared interface which can be used with an IR LED for remote control functions. Two timer output compare channels are used to generate the infrared remote control signals.

### 3.16 Development support

#### Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

#### Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, CPU operation can also be monitored in real-time by means of shadow registers.

#### Bootloader

A bootloader is available to reprogram the Flash memory using the USART1 interface. The reference document for the bootloader is *UM0560: STM8 bootloader user manual*.

The bootloader is used to download application software into the device memories, including RAM, program and data memory, using standard serial interfaces. It is a complementary solution to programming via the SWIM debugging interface.

# 4 Pin description

Figure 3. STM8L052C6 48-pin LQFP48 package pinout (with LCD)

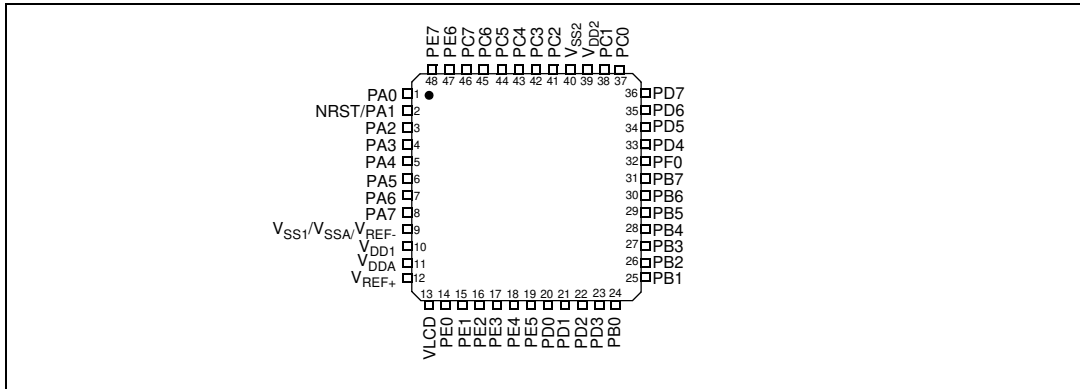


Table 3. Legend/abbreviation for Table 4

<b>Type</b>	I= input, O = output, S = power supply	
<b>Level</b>	FT	Five-volt tolerant
	TT	3.6 V tolerant
	Output	HS = high sink/source (20 mA)
<b>Port and control configuration</b>	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
<b>Reset state</b>	Bold X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. "under reset") and after internal reset release (i.e. at reset state).	

Table 4. Medium-density value line STM8L052C6pin description

Pin #	Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
2	NRST/PA1 <sup>(1)</sup>	I/O			X		HS		X	Reset	PA1
3	PA2/OSC_IN/ [USART1_TX] <sup>(8)</sup> / [SPI1_MISO] <sup>(8)</sup>	I/O		X	X	X	HS	X	X	Port A2	HSE oscillator input / [USART1 transmit] / [SPI1 master in- slave out]
4	PA3/OSC_OUT/[USART1_RX] <sup>(8)</sup> / [SPI1_MOSI] <sup>(8)</sup>	I/O		X	X	X	HS	X	X	Port A3	HSE oscillator output / [USART1 receive] / [SPI1 master out/slave in]



Table 4. Medium-density value line STM8L052C6pin description (continued)

Pin #	Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
5	PA4/TIM2_BKIN/ LCD_COM0/ADC1_IN2	I/O	TT <sup>(2)</sup>	X	X	X	HS	X	X	<b>Port A4</b>	Timer 2 - break input / LCD COM 0 / ADC1 input 2
6	PA5/TIM3_BKIN/ LCD_COM1/ADC1_IN1	I/O	TT <sup>(2)</sup>	X	X	X	HS	X	X	<b>Port A5</b>	Timer 3 - break input / LCD_COM 1 / ADC1 input 1
7	PA6/[ADC1_TRIG]/ LCD_COM2/ADC1_IN0	I/O	TT <sup>(2)</sup>	X	X	X	HS	X	X	<b>Port A6</b>	[ADC1 - trigger] / LCD_COM2 /ADC1 input 0
8	PA7/LCD_SEG0 <sup>(3)</sup>	I/O	FT	X	X	X	HS	X	X	<b>Port A7</b>	LCD segment 0
24	PB0 <sup>(4)</sup> /TIM2_CH1/ LCD_SEG10/ADC1_IN18	I/O	TT <sup>(2)</sup>	X <sup>(4)</sup>	X <sup>(4)</sup>	X	HS	X	X	<b>Port B0</b>	Timer 2 - channel 1 / LCD segment 10 / ADC1_IN18
25	PB1/TIM3_CH1/ LCD_SEG11/ ADC1_IN17	I/O	TT <sup>(2)</sup>	X	X	X	HS	X	X	<b>Port B1</b>	Timer 3 - channel 1 / LCD segment 11 / ADC1_IN17
26	PB2/ TIM2_CH2/ LCD_SEG12/ ADC1_IN16	I/O	TT <sup>(2)</sup>	X	X	X	HS	X	X	<b>Port B2</b>	Timer 2 - channel 2 / LCD segment 12 / ADC1_IN16
27	PB3/TIM2_ETR/ LCD_SEG13/ ADC1_IN15	I/O	TT <sup>(2)</sup>	X	X	X	HS	X	X	<b>Port B3</b>	Timer 2 - external trigger / LCD segment 13 /ADC1_IN15
28	PB4 <sup>(4)</sup> /[SPI1_NSS] <sup>(8)</sup> / LCD_SEG14/ ADC1_IN14	I/O	TT <sup>(2)</sup>	X <sup>(4)</sup>	X <sup>(4)</sup>	X	HS	X	X	<b>Port B4</b>	[SPI1 master/slave select] / LCD segment 14 / ADC1_IN14
29	PB5/[SPI1_SCK] <sup>(8)</sup> / LCD_SEG15/ ADC1_IN13	I/O	TT <sup>(2)</sup>	X	X	X	HS	X	X	<b>Port B5</b>	[SPI1 clock] / LCD segment 15 / ADC1_IN13
30	PB6/[SPI1_MOSI] <sup>(8)</sup> / LCD_SEG16/ ADC1_IN12	I/O	TT <sup>(2)</sup>	X	X	X	HS	X	X	<b>Port B6</b>	[SPI1 master out/slave in] / LCD segment 16 / ADC1_IN12
31	PB7/[SPI1_MISO] <sup>(8)</sup> / LCD_SEG17/ ADC1_IN11	I/O	TT <sup>(2)</sup>	X	X	X	HS	X	X	<b>Port B7</b>	[SPI1 master in- slave out] / LCD segment 17 / ADC1_IN11
37	PC0 <sup>(3)</sup> /I2C1_SDA	I/O	FT	X		X			T <sup>(5)</sup>	<b>Port C0</b>	I2C1 data
38	PC1 <sup>(3)</sup> /I2C1_SCL	I/O	FT	X		X			T <sup>(5)</sup>	<b>Port C1</b>	I2C1 clock
41	PC2/USART1_RX/ LCD_SEG22/ADC1_IN6/ VREFINT	I/O	TT <sup>(2)</sup>	X	X	X	HS	X	X	<b>Port C2</b>	USART1 receive / LCD segment 22 / ADC1_IN6 /Internal voltage reference output

Table 4. Medium-density value line STM8L052C6pin description (continued)

Pin #	Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
42	PC3/USART1_TX/ LCD_SEG23/ ADC1_IN5	I/O	TT <sup>(2)</sup>	X	X	X	HS	X	X	Port C3	USART1 transmit / LCD segment 23 / ADC1_IN5
43	PC4/USART1_CK/ I2C1_SMB/CCO/ LCD_SEG24/ ADC1_IN4	I/O	TT <sup>(2)</sup>	X	X	X	HS	X	X	Port C4	USART1 synchronous clock / I2C1_SMB / Configurable clock output / LCD segment 24/ ADC1_IN4
44	PC5/OSC32_IN /[SPI1_NSS] <sup>(8)</sup> / [USART1_TX] <sup>(8)</sup>	I/O		X	X	X	HS	X	X	Port C5	LSE oscillator input / [SPI1 master/slave select] / [USART1 transmit]
45	PC6/OSC32_OUT/ [SPI1_SCK] <sup>(8)</sup> / [USART1_RX] <sup>(8)</sup>	I/O		X	X	X	HS	X	X	Port C6	LSE oscillator output / [SPI1 clock] / [USART1 receive]
46	PC7/LCD_SEG25/ ADC1_IN3	I/O	TT <sup>(2)</sup>	X	X	X	HS	X	X	Port C7	LCD segment 25 /ADC1_IN3
20	PD0/TIM3_CH2/ [ADC1_TRIG] <sup>(8)</sup> / LCD_SEG7/ADC1_IN22/	I/O	TT <sup>(2)</sup>	X	X	X	HS	X	X	Port D0	Timer 3 - channel 2 / [ADC1_Trigger] / LCD segment 7 / ADC1_IN22
21	PD1/TIM3_ETR/ LCD_COM3/ ADC1_IN21	I/O	TT <sup>(2)</sup>	X	X	X	HS	X	X	Port D1	Timer 3 - external trigger / LCD_COM3 / ADC1_IN21
22	PD2/TIM1_CH1 /LCD_SEG8/ ADC1_IN20	I/O	TT <sup>(2)</sup>	X	X	X	HS	X	X	Port D2	Timer 1 - channel 1 / LCD segment 8 / ADC1_IN20
23	PD3/ TIM1_ETR/ LCD_SEG9/ADC1_IN19	I/O	TT <sup>(2)</sup>	X	X	X	HS	X	X	Port D3	Timer 1 - external trigger / LCD segment 9 / ADC1_IN19
33	PD4/TIM1_CH2 /LCD_SEG18/ ADC1_IN10	I/O	TT <sup>(2)</sup>	X	X	X	HS	X	X	Port D4	Timer 1 - channel 2 / LCD segment 18 / ADC1_IN10
34	PD5/TIM1_CH3 /LCD_SEG19/ ADC1_IN9	I/O	TT <sup>(2)</sup>	X	X	X	HS	X	X	Port D5	Timer 1 - channel 3 / LCD segment 19 / ADC1_IN9
35	PD6/TIM1_BKIN /LCD_SEG20/ ADC1_IN8/RTC_CALIB/ /VREFINT	I/O	TT <sup>(2)</sup>	X	X	X	HS	X	X	Port D6	Timer 1 - break input / LCD segment 20 / ADC1_IN8 / RTC calibration / Internal voltage reference output