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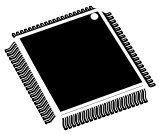
STM8L052R8

Value Line, 8-bit ultralow power MCU, 64-KB Flash, 256-byte data EEPROM, RTC, LCD, timers, USART, I2C, SPI, ADC

Datasheet - production data

Features

- Operating conditions
  - Operating power supply: 1.8 V to 3.6 V
  - Temperature range: -40 °C to 85 °C
- Low power features
  - 5 low power modes: Wait, Low power run (5.9 µA), Low power wait (3 µA), Active-halt with full RTC (1.4 µA), Halt (400 nA)
  - Dynamic power consumption: 200 µA/MHz + 330 µA
  - Ultra-low leakage per I/0: 50 nA
  - Fast wakeup from Halt: 4.7 µs
- Advanced STM8 core
  - Harvard architecture and 3-stage pipeline
  - Max freq. 16 MHz, 16 CISC MIPS peak
  - Up to 40 external interrupt sources
- Reset and supply management
  - Low power, ultra-safe BOR reset with 5 programmable thresholds
  - Ultra low power POR/PDR
  - Programmable voltage detector (PVD)
- Clock management
  - 32 kHz and 1 to 16 MHz crystal oscillators
  - Internal 16 MHz factory-trimmed RC
  - 38 kHz low consumption RC
  - Clock security system
- Low power RTC
  - BCD calendar with alarm interrupt
  - Digital calibration with +/- 0.5ppm accuracy
  - Advanced anti-tamper detection
- LCD: 8x24 or 4x28 w/ step-up converter
- Memories
  - 64 KB Flash program memory and 256 bytes data EEPROM with ECC, RWW
  - Flexible write and read protection modes
  - 4 KB of RAM



LQFP64

- DMA
  - 4 channels supporting ADC, SPIs, I2C, USARTs, timers
  - 1 channel for memory-to-memory
- 12-bit ADC up to 1 Msps/27 channels
  - Internal reference voltage
- Timers
  - Three 16-bit timers with 2 channels (used as IC, OC, PWM), quadrature encoder
  - One 16-bit advanced control timer with 3 channels, supporting motor control
  - One 8-bit timer with 7-bit prescaler
  - 2 watchdogs: 1 Window, 1 Independent
  - Beeper timer with 1, 2 or 4 kHz frequencies
- Communication interfaces
  - Two synchronous serial interfaces (SPI)
  - Fast I2C 400 kHz SMBus and PMBus
  - Three USARTs (ISO 7816 interface + IrDA)
- Up to 54 I/Os, all mappable on interrupt vectors
- Development support
  - Fast on-chip programming and non-intrusive debugging with SWIM
  - Bootloader using USART

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1 Introduction

This document describes the features, pinout, mechanical data and ordering information of the high density value line STM8L052R8 microcontroller with a Flash memory density of 64 Kbytes.

For further details on the whole STMicroelectronics high density family please refer to *Section 2.2: Ultra low power continuum*.

For detailed information on device operation and registers, refer to the reference manual (RM0031).

For information on to the Flash program memory and data EEPROM, refer to the programming manual (PM0054).

For information on the debug module and SWIM (single wire interface module), refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).

For information on the STM8 core, refer to the STM8 CPU programming manual (PM0044).

High density value line devices provide the following benefits:

- Integrated system
  - 64 Kbytes of high density embedded Flash program memory
  - 256 bytes of data EEPROM
  - 4 Kbytes of RAM
  - Internal high speed and low-power low speed RC
  - Embedded reset
- Ultra low power consumption
  - 1 µA in Active-halt mode
  - Clock gated system and optimized power management
  - Capability to execute from RAM for Low power wait mode and low power run mode
- Advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Direct memory access (DMA) for memory-to-memory or peripheral-to-memory access
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals
  - Wide choice of development tools

These features make the value line STM8L05xxx ultra low power microcontroller family suitable for a wide range of consumer and mass market applications.

Refer to *Table 1: High density value line STM8L05xxx low power device features and peripheral counts* and *Section 3: Functional overview* for an overview of the complete range of peripherals proposed in this family.

Figure 1 shows the block diagram of the high density value line STM8L05xxx family.

2 Description

The high density value line STM8L05xxx devices are members of the STM8L ultra low power 8-bit family.

The value line STM8L05xxx ultra low power family features the enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive In-application debugging and ultra-fast Flash programming.

High density value line STM8L05xxx microcontrollers feature embedded data EEPROM and low-power, low-voltage, single-supply program Flash memory.

All devices offer 12-bit ADC, real-time clock, four 16-bit timers, one 8-bit timer as well as standard communication interface such as two SPIs, I2C, three USARTs and 8x24 or 4x28-segment LCD. The 8x24 or 4x 28-segment LCD is available on the high density value line STM8L05xxx.

The STM8L05xxx family operates from 1.8 V to 3.6 V and is available in the -40 to +85 °C temperature range.

The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

All value line STM8L ultra low power products are based on the same architecture with the same memory mapping and a coherent pinout.

2.1 Device overview

Table 1. High density value line STM8L05xxx low power device features and peripheral counts

Features		STM8L052R8
Flash (Kbytes)		64
Data EEPROM (bytes)		256
RAM (Kbytes)		4
LCD		8x24 or 4x28
Timers	Basic	1 (8-bit)
	General purpose	3 (16-bit)
	Advanced control	1 (16-bit)
Communication interfaces	SPI	2
	I2C	1
	USART	3
GPIOs		54(1)
12-bit synchronized ADC (number of channels)		1 (26)
Others		RTC, window watchdog, independent watchdog, 16-MHz and 38-kHz internal RC, 1- to 16-MHz and 32-kHz external oscillator
CPU frequency		16 MHz
Operating voltage		1.8 V to 3.6 V
Operating temperature		-40 to +85 °C
Package		LQFP64

1. The number of GPIOs given in this table includes the NRST/PA1 pin but the application can use the NRST/PA1 pin as general purpose output only (PA1).

2.2 Ultra low power continuum

The ultra low power value line STM8L05xxx and STM8L15xxx are fully pin-to-pin, software and feature compatible. Besides the full compatibility within the STM8L family, the devices are part of STMicroelectronics microcontrollers ultra low power strategy which also includes STM8L101xx and STM32L15xxx. The STM8L and STM32L families allow a continuum of performance, peripherals, system architecture, and features.

They are all based on STMicroelectronics 0.13 µm ultra-low leakage process.

Note: 1 The STM8L05xxx is pin-to-pin compatible with STM8L101xx devices.

2 The STM32L family is pin-to-pin compatible with the general purpose STM32F family. Please refer to STM32L15x documentation for more information on these devices.

Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM Cortex™-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra low power performance to range from 5 up to 33.3 DMIPs.

Shared peripherals

STM8L05x, STM8L15x and STM32L15xx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripheral: ADC1
- Digital peripherals: RTC and some communication interfaces

Common system strategy

To offer flexibility and optimize performance, the STM8L and STM32L devices use a common architecture:

- Same power supply range from 1.8 to 3.6 V
- Architecture optimized to reach ultra-low consumption both in low power modes and Run mode
- Fast startup strategy from low power modes
- Flexible system clock
- Ultra-safe reset: same reset strategy for both STM8L and STM32L including power-on reset, power-down reset, brownout reset and programmable voltage detector

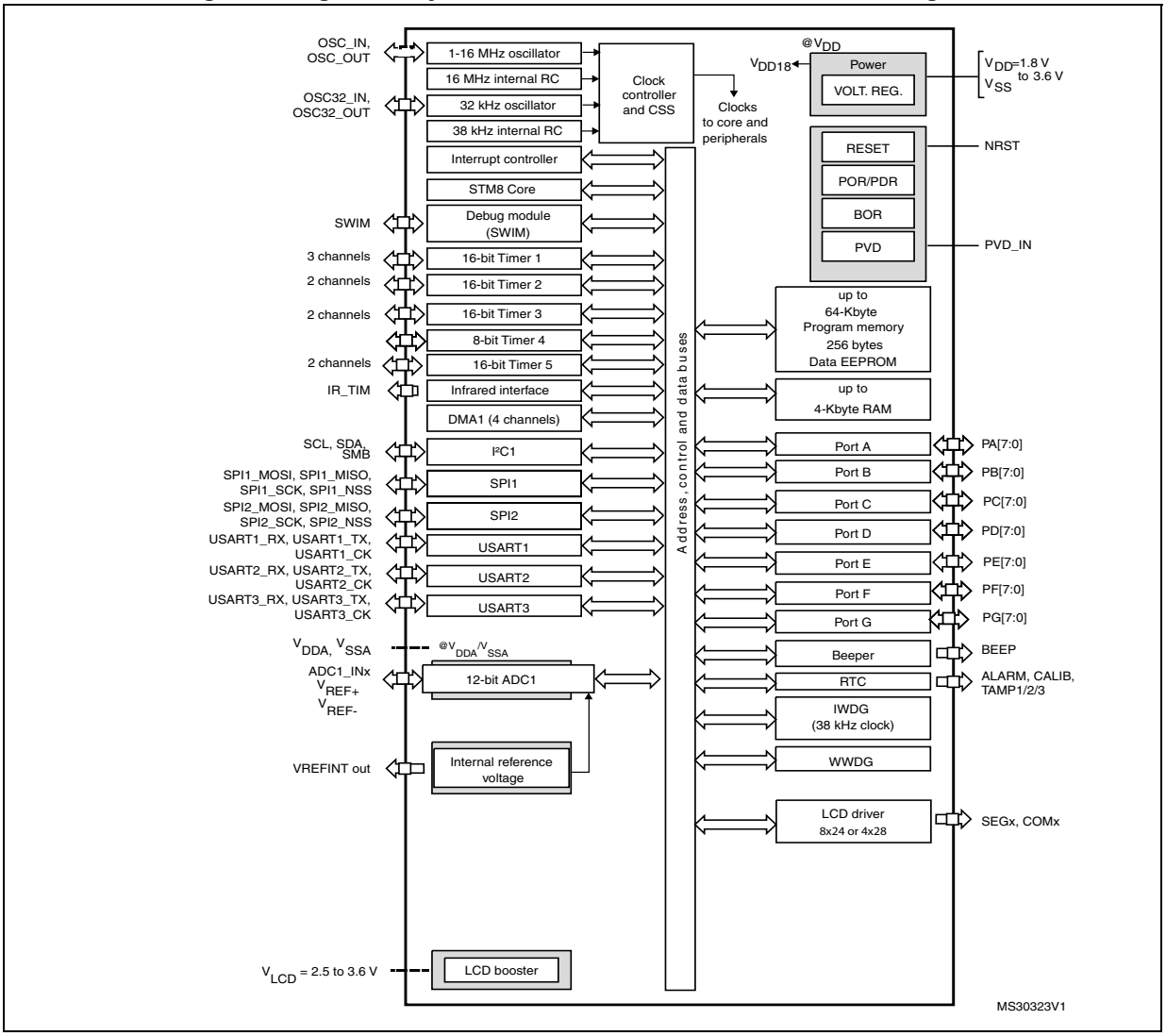
Features

ST ultra low power continuum also lies in feature compatibility:

- More than 10 packages with pin count from 20 to 100 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 128 Kbytes

3 Functional overview

Figure 1. High density value line STM8L05xxx device block diagram



1. **Legend**:
   ADC: Analog-to-digital converter
   BOR: Brownout reset
   DMA: Direct memory access
   I²C: Inter-integrated circuit multimaster interface
   LCD: Liquid crystal display
   POR/PDR: Power on reset / power down reset
   RTC: Real-time clock
   SPI: Serial peripheral interface
   SWIM: Single wire interface module
   USART: Universal synchronous asynchronous receiver transmitter
   WWDG: Window watchdog
   IWDG: independent watchdog

3.1 Low power modes

The high density value line STM8L05xxx devices support five low power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Wait mode**: The CPU clock is stopped, but selected peripherals keep running. An internal or external interrupt, event or a Reset can be used to exit the microcontroller from Wait mode (WFE or WFI mode).
- **Low power run mode**: The CPU and the selected peripherals are running. Execution is done from RAM with a low speed oscillator (LSI or LSE). Flash memory and data EEPROM are stopped and the voltage regulator is configured in ultra low power mode. The microcontroller enters Low power run mode by software and can exit from this mode by software or by a reset.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode.
- **Low power wait mode:** This mode is entered when executing a Wait for event in Low power run mode. It is similar to Low power run mode except that the CPU clock is stopped. The wakeup from this mode is triggered by a Reset or by an internal or external event (peripheral event generated by the timers, serial interfaces, DMA controller (DMA1) and I/O ports). When the wakeup is triggered by an event, the system goes back to Low power run mode.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode.
- **Active-halt mode**: CPU and peripheral clocks are stopped, except RTC. The wakeup can be triggered by RTC interrupts, external interrupts or reset.
- **Halt mode**: CPU and peripheral clocks are stopped, the device remains powered on. The wakeup is triggered by an external interrupt or reset. A few peripherals have also a wakeup from Halt capability. Switching off the internal reference voltage reduces power consumption. Through software configuration it is also possible to wake up the device without waiting for the internal reference voltage wakeup time to have a fast wakeup time of 5 µs.

3.2 Central processing unit STM8

3.2.1 Advanced STM8 Core

The 8-bit STM8 core is designed for code efficiency and performance with an Harvard architecture and a 3-stage pipeline.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing, and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16-Mbyte linear memory space
- 16-bit stack pointer - access to a 64-Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

3.2.2 Interrupt controller

The high density value line STM8L05xxx devices feature a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 32 interrupt vectors with hardware priority
- Up to 40 external interrupt sources on 11 vectors
- Trap and reset interrupts

3.3 Reset and supply management

3.3.1 Power supply scheme

The device requires a 1.8 V to 3.6 V operating supply voltage (V_{DD}). The external power supply pins must be connected as follows:

- V_{SS1}, V_{DD1}, V_{SS2}, V_{DD2}, V_{SS3}, V_{DD3} = 1.8 to 3.6 V: external power supply for I/Os and for the internal regulator. Provided externally through V_{DD} pins, the corresponding ground pin is VSS. V_{SS1}/V_{SS2}/V_{SS3}/V_{SS4} and V_{DD1}/V_{DD2}/V_{DD3} must not be left unconnected.
- V_{SSA} ; V_{DDA} = 1.8 to 3.6 V: external power supplies for analog peripherals. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{REF+} ; V_{REF-} (for ADC1): external reference voltage for ADC1. Must be provided externally through V_{REF+} and V_{REF-} pin.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR), coupled with a brownout reset (BOR) circuitry that ensures proper operation starting from 1.8 V. After the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Halt mode, it is possible to automatically switch off the internal reference voltage (and consequently the BOR) in Halt mode. The device remains under reset when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The high density value line STM8L05xxx embeds an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals.

This regulator has two different modes:

- Main voltage regulator mode (MVR) for Run, Wait for interrupt (WFI) and Wait for event (WFE) modes
- Low power voltage regulator mode (LPVR) for Halt, Active-halt, Low power run and Low power wait modes

When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption.

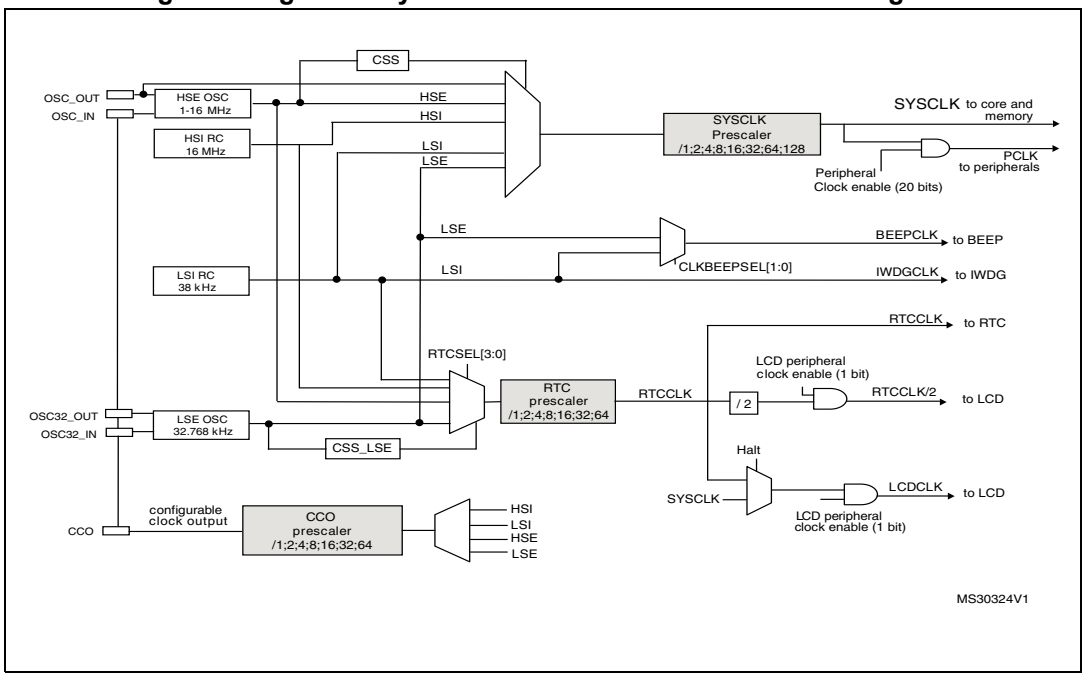
3.4 Clock management

The clock controller distributes the system clock (SYSCLK) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

Features

- **Clock prescaler:** To get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching:** Clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock sources:** 4 different clock sources can be used to drive the system clock:
  - 1-16 MHz High speed external crystal (HSE)
  - 16 MHz High speed internal RC oscillator (HSI)
  - 32.768 kHz Low speed external crystal (LSE)
  - 38 kHz Low speed internal RC (LSI)
- **RTC and LCD clock sources:** The above four sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If a HSE clock failure occurs, the system clock is automatically switched to HSI.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

Figure 2. High density value line STM8L05xxx clock tree diagram



1. The HSE clock source can be either an external crystal/ceramic resonator or an external source (HSE bypass). Refer to *Section HSE clock* in the STM8L15x and STM8L16x reference manual (RM0031).
2. The LSE clock source can be either an external crystal/ceramic resonator or a external source (LSE bypass). Refer to *Section LSE clock* in the STM8L15x and STM8L16x reference manual (RM0031).

3.5 Low power real-time clock

The real-time clock (RTC) is an independent binary coded decimal (BCD) timer/counter.

Six byte locations contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day months are made automatically.The subsecond field can also be read in binary format.

The calendar can be corrected from 1 to 32767 RTC clock pulses. This allows to make a synchronization to a master clock.

The RTC offers a digital calibration which allows an accuracy of +/-0.5ppm.

It provides a programmable alarm and programmable periodic interrupts with wakeup from Halt capability.

- Periodic wakeup time using the 32.768 kHz LSE with the lowest resolution (of 61 µs) is from min. 122 µs to max. 3.9 s. With a different resolution, the wakeup time can reach 36 hours.
- Periodic alarms based on the calendar can also be generated from every second to every year.

A clock security system detects a failure on LSE, and can provide an interrupt with wakeup capability. The RTC clock can automatically switch to LSI in case of LSE failure.

The RTC also provides 3 anti-tamper detection pins. This detection embeds a programmable filter and can wakeup the MCU.

3.6 LCD (Liquid crystal display)

The LCD is only available on STM8L052xx devices.

The liquid crystal display drives up to 8 common terminals and up to 24 segment terminals to drive up to 192 pixels. It can also be configured to drive up to 4 common and 28 segments (up to 112 pixels).

- Internal step-up converter to guarantee contrast control whatever V_{DD}.
- Static 1/2, 1/3, 1/4, 1/8 duty supported.
- Static 1/2, 1/3, 1/4 bias supported.
- Phase inversion to reduce power consumption and EMI.
- Up to 8 pixels which can be programmed to blink.
- The LCD controller can operate in Halt mode.

Note: Unnecessary segments and common pins can be used as general I/O pins.

3.7 Memories

The high density value line STM8L05xxx devices have the following main features:

- 4 Kbytes of RAM
- The non-volatile memory is divided into three arrays:
  - 64 Kbytes of high density embedded Flash program memory
  - 256 bytes of data EEPROM
  - Option bytes

The EEPROM embeds the error correction code (ECC) feature. It supports the read-while-write (RWW): it is possible to execute the code from the program matrix while programming/erasing the data matrix.

The option byte protects part of the Flash program memory from write and readout piracy.

3.8 DMA

A 4-channel direct memory access controller (DMA1) offers a memory-to-memory and peripherals-from/to-memory transfer capability. The 4 channels are shared between the following IPs with DMA capability: ADC1, I2C1, SPI1, SPI 2, USART1, USART2, USART3 and the five timers.

3.9 Analog-to-digital converter

- 12-bit analog-to-digital converter (ADC1) with 27 channels (including 4 fast channels) and internal reference voltage
- Conversion time down to 1 µs with f_{SYSCLK}= 16 MHz
- Programmable resolution
- Programmable sampling time
- Single and continuous mode of conversion
- Scan capability: automatic conversion performed on a selected group of analog inputs
- Analog watchdog: interrupt generation when the converted voltage is outside the programmed threshold
- Triggered by timer

Note: ADC1 can be served by DMA1.

3.10 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM4 and ADC1 DMA channels can also be remapped.

The highly flexible routing interface allows application software to control the routing of different I/Os to the TIM1 timer input captures. It also controls the routing of internal analog signals to ADC1 and the internal reference voltage V_{REFINT}.

3.11 Timers

The high density value line STM8L05xxx devices contain one advanced control timer (TIM1), three 16-bit general purpose timers (TIM2, TIM3 and TIM5) and one 8-bit basic timer (TIM4).

All the timers can be served by DMA1.

Table 2 compares the features of the advanced control, general-purpose and basic timers.

Table 2. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA1 request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	up/down	Any integer from 1 to 65536	Yes	3 + 1	3
TIM2			Any power of 2 from 1 to 128		2	None
TIM3						
TIM5						
TIM4	8-bit	up	Any power of 2 from 1 to 32768		0	

3.11.1 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver.

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- 3 independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- 1 additional capture/compare channel which is not connected to an external I/O
- Synchronization module to control the timer with external signals
- Break input to force timer outputs into a defined state
- 3 complementary outputs with adjustable dead time
- Encoder mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)

3.11.2 16-bit general purpose timers

- 16-bit autoreload (AR) up/down-counter
- 7-bit prescaler adjustable to fixed power of 2 ratios (1…128)
- 2 individually configurable capture/compare channels
- PWM mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)
- Synchronization with other timers or external signals (external clock, reset, trigger and enable)

3.11.3 8-bit basic timer

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. It can be used for timebase generation with interrupt generation on timer overflow.

3.12 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

3.12.1 Window watchdog timer

The window watchdog (WWDG) is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

3.12.2 Independent watchdog timer

The independent watchdog peripheral (IWDG) can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the internal LSI RC clock source, and thus stays active even in case of a CPU clock failure.

3.13 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

3.14 Communication interfaces

3.14.1 SPI

The serial peripheral interfaces (SPI1 and SPI2) provide half/ full duplex synchronous serial communication with external devices.

- Maximum speed: 8 Mbit/s (f_{SYSCLK}/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- Hardware CRC calculation
- Slave/master selection input pin

Note: SPI1 and SPI2 *can be served by the DMA1 Controller.*

3.14.2 I²C

The I^2C bus interface (I^2C1) provides multi-master capability, and controls all I²C bus-specific sequencing, protocol, arbitration and timing.

- Master, slave and multi-master capability
- Standard mode up to 100 kHz and fast speed modes up to 400 kHz
- 7-bit and 10-bit addressing modes
- SMBus 2.0 and PMBus support
- Hardware CRC calculation

Note: I^2C1 can be served by the DMA1 Controller.

3.14.3 USART

The USART interfaces (USART1, USART2 and USART3) allow full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

- 1 Mbit/s full duplex SCI
- SPI1 emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- Single wire half duplex mode

Note: USART1, USART2 and USART3 *can be served by the DMA1 Controller.*

3.15 Infrared (IR) interface

The high density value line STM8L05xxx devices contain an infrared interface which can be used with an IR LED for remote control functions. Two timer output compare channels are used to generate the infrared remote control signals.

3.16 Development support

Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, CPU operation can also be monitored in real-time by means of shadow registers.

Bootloader

A bootloader is available to reprogram the Flash memory using the USART1, USART2,

USART3 (USARTs in asynchronous mode), SPI1 or SPI2 interfaces. The reference document for the bootloader is *UM0560: STM8 bootloader user manual*.

The bootloader is used to download application software into the device memories, including RAM, program and data memory, using standard serial interfaces. It is a complementary solution to programming via the SWIM debugging interface.

4 Pin description

Figure 3. STM8L052R8 64-pin LQFP64 package pinout

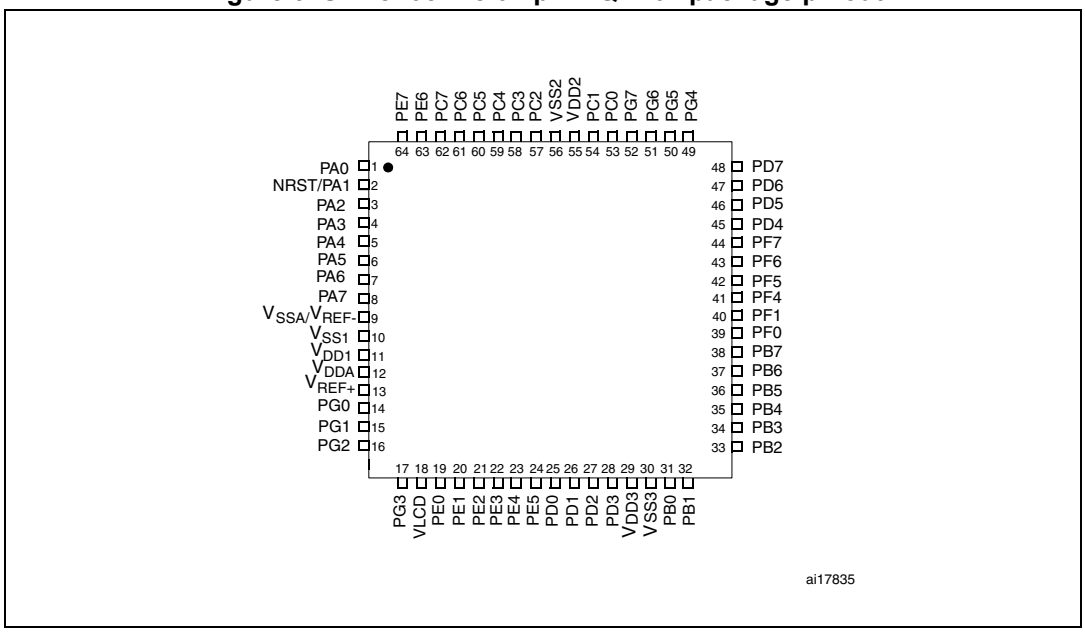


Table 3. Legend/abbreviation for *Table 4*

Type	I= input, O = output, S = power supply	
Level	FT	Five-volt tolerant
	TT	3.6 V tolerant
	Output	HS = high sink/source (20 mA)
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state).	

Table 4. High density value line STM8L05xxx pin description

Pin number	Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP64				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
2	NRST/PA1(1)	I/O	-	-	X	-	HS	X	X	**Reset**	PA1
3	PA2/OSC_IN/ *[USART1_TX]*(8)/ *[SPI1_MISO]*(8)	I/O	-	X	X	X	HS	X	X	**Port A2**	HSE oscillator input / *[USART1 transmit] / [SPI1 master in- slave out]*
4	PA3/OSC_OUT/*[USART1_RX]*(8)/*[SPI1_MOSI]*(8)	I/O	-	X	X	X	HS	X	X	**Port A3**	HSE oscillator output / *[USART1 receive]/ [SPI1 master out/slave in]/*
5	PA4/TIM2_BKIN/ *[TIM2_ETR]*(8)/ LCD_COM0/ADC1_IN2	I/O	FT(2)	X	X	X	HS	X	X	**Port A4**	Timer 2 - break input */[Timer 2 - trigger]/* LCD COM 0 / ADC1 input 2
6	PA5/TIM3_BKIN/ *[TIM3_ETR]*(8)/ LCD_COM1/ADC1_IN1	I/O	FT(2)	X	X	X	HS	X	X	**Port A5**	Timer 3 - break input */[Timer 3 - trigger]/* LCD_COM 1 / ADC1 input 1
7	PA6/*[ADC1_TRIG]*/ LCD_COM2/ADC1_IN0	I/O	FT(2)	X	X	X	HS	X	X	**Port A6**	*[ADC1 - trigger]* / LCD_COM2 / ADC1 input 0
8	PA7/LCD_SEG0(2) /TIM5_CH1	I/O	FT(2)	X	X	X	HS	X	X	**Port A7**	LCD segment 0/ TIM5 channel 1
31	PB0(3)/TIM2_CH1/ LCD_SEG10/ADC1_IN18	I/O	FT(2)	X	X	X	HS	X	X	**Port B0**	Timer 2 - channel 1 / LCD segment 10 / ADC1_IN18

Table 4. High density value line STM8L05xxx pin description (continued)

Pin number	Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP64				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
32	PB1/TIM3_CH1/ LCD_SEG11/ ADC1_IN17	I/O	FT(2)	X	X	X	HS	X	X	**Port B1**	Timer 3 - channel 1 / LCD segment 11 / ADC1_IN17
33	PB2/ TIM2_CH2/ LCD_SEG12/ ADC1_IN16	I/O	FT(2)	X	X	X	HS	X	X	**Port B2**	Timer 2 - channel 2 / LCD segment 12 / ADC1_IN16
34	PB3/TIM2_ETR/ LCD_SEG13/ ADC1_IN15	I/O	FT(2)	X	X	X	HS	X	X	**Port B3**	Timer 2 - trigger / LCD segment 13 /ADC1_IN15
35	PB4(3)/*[SPI1_NSS]*(8)/ LCD_SEG14/ ADC1_IN14	I/O	FT(2)	X(3)	X(3)	X	HS	X	X	**Port B4**	*[SPI1 master/slave select]* / LCD segment 14 / ADC1_IN14
36	PB5/*[SPI1_SCK]*(8)/ LCD_SEG15/ ADC1_IN13	I/O	FT(2)	X	X	X	HS	X	X	**Port B5**	*[SPI1 clock]* / LCD segment 15 / ADC1_IN13
37	PB6/[*SPI1_MOSI]*(8)/ LCD_SEG16/ ADC1_IN12	I/O	FT(2)	X	X	X	HS	X	X	**Port B6**	*[SPI1 master out/slave in]*/ LCD segment 16 / ADC1_IN12
38	PB7/*[SPI1_MISO]*(8)/ LCD_SEG17/ ADC1_IN11	I/O	FT(2)	X	X	X	HS	X	X	**Port B7**	*[SPI1 master in- slave out]* /LCD segment 17 / ADC1_IN11
53	PC0(2)/I2C1_SDA	I/O	FT(2)	X	-	X		T(4)		**Port C0**	I2C1 data
54	PC1(2)/I2C1_SCL	I/O	FT(2)	X	-	X		T(4)		**Port C1**	I2C1 clock
57	PC2/USART1_RX/ LCD_SEG22/ADC1_IN6/ VREFINT	I/O	FT(2)	X	X	X	HS	X	X	**Port C2**	USART1 receive / LCD segment 22 / ADC1_IN6 /Internal voltage reference output
58	PC3/USART1_TX/ LCD_SEG23/ ADC1_IN5	I/O	FT(2)	X	X	X	HS	X	X	**Port C3**	USART1 transmit / LCD segment 23 / ADC1_IN5
59	PC4/USART1_CK/ I2C1_SMB/CCO/ ADC1_IN4	I/O	FT(2)	X	X	X	HS	X	X	**Port C4**	USART1 synchronous clock / I2C1_SMB / Configurable clock output / ADC1_IN4