Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

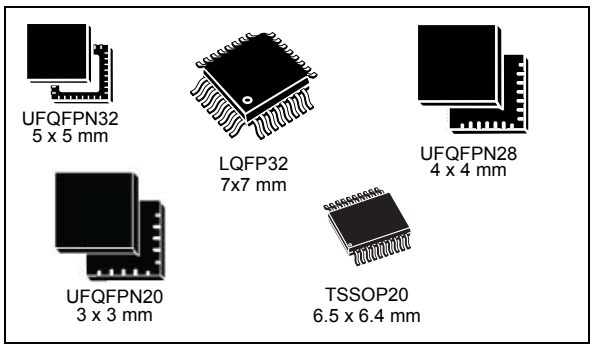
STM8L101x1 STM8L101x2 STM8L101x3

8-bit ultra-low power microcontroller with up to 8 Kbytes Flash, multifunction timers, comparators, USART, SPI, I2C

Datasheet - production data

Features

- Main microcontroller features
  - Supply voltage range 1.65 V to 3.6 V
  - Low power consumption (Halt: 0.3 µA, Active-halt: 0.8 µA, Dynamic Run: 150 µA/MHz)
  - STM8 Core with up to 16 CISC MIPS throughput
  - Temp. range: -40 to 85 °C and 125 °C
- Memories
  - Up to 8 Kbytes of Flash program including up to 2 Kbytes of data EEPROM
  - Error correction code (ECC)
  - Flexible write and read protection modes
  - In-application and in-circuit programming
  - Data EEPROM capability
  - 1.5 Kbytes of static RAM
- Clock management
  - Internal 16 MHz RC with fast wakeup time (typ. 4 µs)
  - Internal low consumption 38 kHz RC driving both the IWDG and the AWU
- Reset and supply management
  - Ultra-low power POR/PDR
  - Three low-power modes: Wait, Active-halt, Halt
- Interrupt management
  - Nested interrupt controller with software priority control
  - Up to 29 external interrupt sources
- I/Os
  - Up to 30 I/Os, all mappable on external interrupt vectors
  - I/Os with programmable input pull-ups, high sink/source capability and one LED driver infrared output



- Peripherals
  - Two 16-bit general purpose timers (TIM2 and TIM3) with up and down counter and 2 channels (used as IC, OC, PWM)
  - One 8-bit timer (TIM4) with 7-bit prescaler
  - Infrared remote control (IR)
  - Independent watchdog
  - Auto-wakeup unit
  - Beeper timer with 1, 2 or 4 kHz frequencies
  - SPI synchronous serial interface
  - Fast I2C Multimaster/slave 400 kHz
  - USART with fractional baud rate generator
  - 2 comparators with 4 inputs each
- Development support
  - Hardware single wire interface module (SWIM) for fast on-chip programming and non intrusive debugging
  - In-circuit emulation (ICE)
- 96-bit unique ID

Table 1. Device summary

Reference	Part numbers
STM8L101x1	STM8L101F1
STM8L101x2	STM8L101F2, STM8L101G2
STM8L101x3	STM8L101F3, STM8L101G3, STM8L101K3

Contents

List of tables

List of figures

1 Introduction

This datasheet provides the STM8L101x1 STM8L101x2 STM8L101x3 pinout, ordering information, mechanical and electrical device characteristics.

For complete information on the STM8L101x1 STM8L101x2 STM8L101x3 microcontroller memory, registers and peripherals, please refer to the STM8L reference manual.

The STM8L101x1 STM8L101x2 STM8L101x3devices are members of the STM8L low-power 8-bit family. They are
referred to as low-density devices in the STM8L101x1 STM8L101x2 STM8L101x3 microcontroller family reference manual (RM0013) and in the STM8L Flash programming manual (PM0054).

All devices of the SM8L product line provide the following benefits:

- Reduced system cost
  - Up to 8 Kbytes of low-density embedded Flash program memory including up to 2 Kbytes of data EEPROM
  - High system integration level with internal clock oscillators and watchdogs.
  - Smaller battery and cheaper power supplies.
- Low power consumption and advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Less than 150 µA/MH, 0.8 µA in Active-halt mode, and 0.3 µA in Halt mode
  - Clock gated system and optimized power management
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals.
  - Full documentation and a wide choice of development tools
- Product longevity
  - Advanced core and peripherals made in a state-of-the art technology
  - Product family operating from 1.65 V to 3.6 V supply.

2 Description

The STM8L101x1 STM8L101x2 STM8L101x3 low-power family features the enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive in-application debugging and ultrafast Flash programming.

All STM8L101xx microcontrollers feature low power low-voltage single-supply program Flash memory. The 8-Kbyte devices embed data EEPROM.

The STM8L101xx low power family is based on a generic set of state-of-the-art peripherals. The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

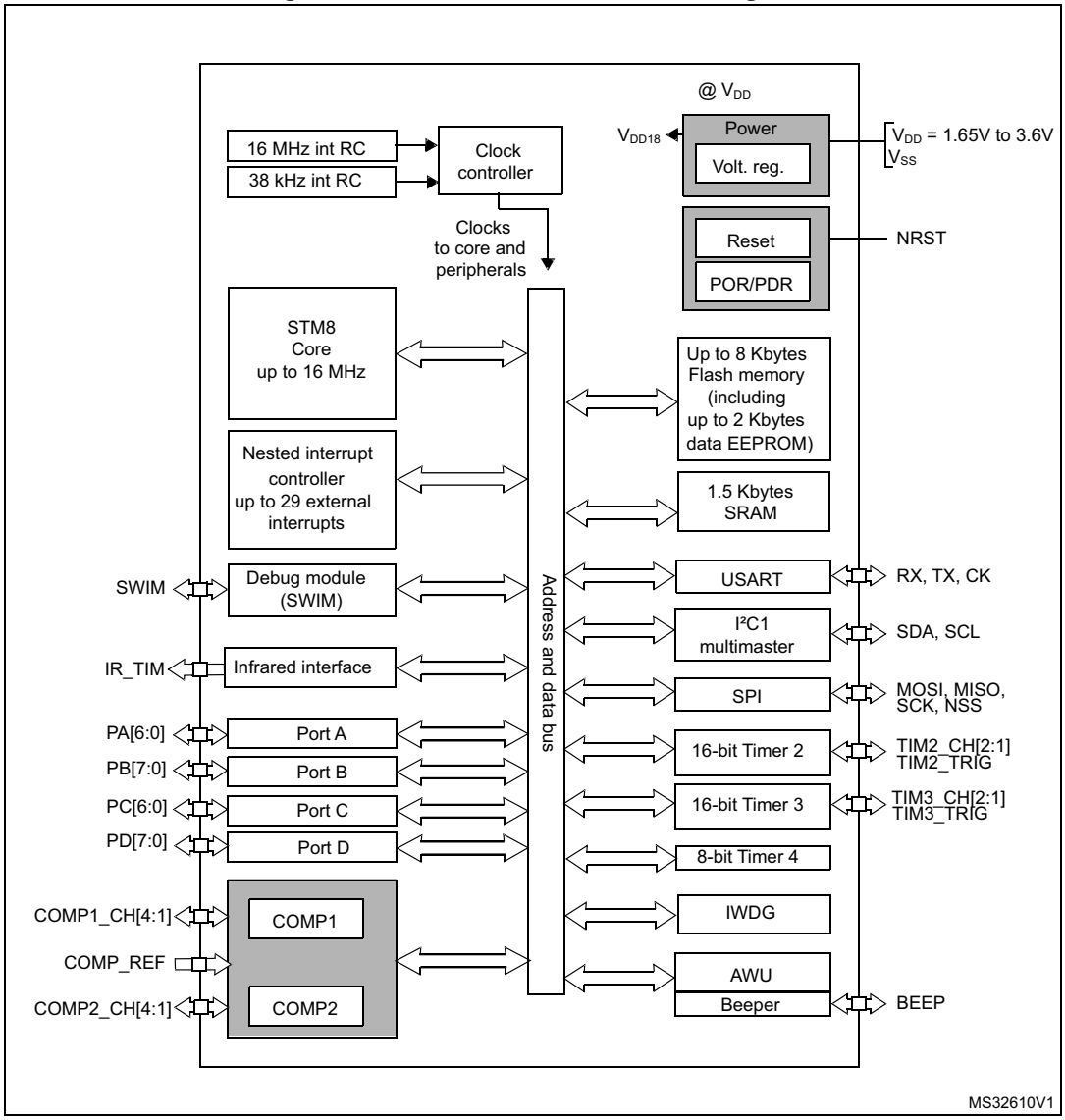
All STM8L low power products are based on the same architecture with the same memory mapping and a coherent pinout.

Table 2. STM8L101xx device feature summary

Features	STM8L101xx		
Flash	2 Kbytes of Flash program memory	4 Kbytes of Flash program memory	8 Kbytes of Flash program memory including up to 2 Kbytes of Data EEPROM
RAM	1.5 Kbytes		
Peripheral functions	Independent watchdog (IWDG), Auto-wakeup unit (AWU), Beep, Serial peripheral interface (SPI), Inter-integrated circuit (I²C), Universal synchronous / asynchronous receiver / transmitter (USART), 2 comparators, Infrared (IR) interface		
Timers	Two 16-bit timers, one 8-bit timer		
Operating voltage	1.65 to 3.6 V		
Operating temperature	-40 to +85 °C		-40 to +85 °C or -40 to +125 °C
Packages	UFQFPN20 3x3	UFQFPN28 4x 4 UFQFPN20 3x3 TSSOP20 4.4 x 6.4	UFQFPN28 4x4 UFQFPN20 3x3 UFQFPN32 LQFP32

3 Product overview

Figure 1. STM8L101xx device block diagram



Legend:

AWU: Auto-wakeup unit
Int. RC: internal RC oscillator
I²C: Inter-integrated circuit multimaster interface
POR/PDR: Power on reset / power down reset
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous / asynchronous receiver / transmitter
IWDG: Independent watchdog

3.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It features 21 internal registers, 20 addressing modes including indexed, indirect and relative addressing, and 80 instructions.

3.2 Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

3.3 Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, also CPU operation can be monitored in real-time by means of shadow registers.

3.4 Interrupt controller

The STM8L101xx features a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 26 interrupt vectors with hardware priority
- Up to 29 external interrupt sources on 10 vectors
- Trap and reset interrupts.

3.5 Memory

The STM8L101xx devices have the following main features:

- 1.5 Kbytes of RAM
- The EEPROM is divided into two memory arrays (see the STM8L reference manual for details on the memory mapping):
  - Up to 8 Kbytes of low-density embedded Flash program including up to 2 Kbytes of data EEPROM. Data EEPROM and Flash program areas can be write protected independently by using the memory access security mechanism (MASS).
  - 64 option bytes (one block) of which 5 bytes are already used for the device.

Error correction code is implemented on the EEPROM.

3.6 Low power modes

To minimize power consumption, the product features three low power modes:

- Wait mode: CPU clock stopped, selected peripherals at full clock speed.
- Active-halt mode: CPU and peripheral clocks are stopped. The programmable wakeup time is controlled by the AWU unit.
- Halt mode: CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. Wakeup is triggered by an external interrupt.

3.7 Voltage regulators

The STM8L101xx embeds an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals.

This regulator has two different modes: main voltage regulator mode (MVR) and low power voltage regulator mode (LPVR). When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption.

3.8 Clock control

The STM8L101xx embeds a robust clock controller. It is used to distribute the system clock to the core and the peripherals and to manage clock gating for low power modes. This system clock is a 16-MHz High Speed Internal RC oscillator (HSI RC), followed by a programmable prescaler.

In addition, a 38 kHz low speed internal RC oscillator is used by the independent watchdog (IWDG) and Auto-wakeup unit (AWU).

3.9 Independent watchdog

The independent watchdog (IWDG) peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 38 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure.

3.10 Auto-wakeup counter

The auto-wakeup (AWU) counter is used to wakeup the device from Active-halt mode.

3.11 General purpose and basic timers

STM8L101xx devices contain two 16-bit general purpose timers (TIM2 and TIM3) and one 8-bit basic timer (TIM4).

16-bit general purpose timers

The 16-bit timers consist of 16-bit up/down auto-reload counters driven by a programmable prescaler. They perform a wide range of functions, including:

- Time base generation
- Measuring the pulse lengths of input signals (input capture)
- Generating output waveforms (output compare, PWM and One pulse mode)
- Interrupt capability on various events (capture, compare, overflow, break, trigger)

8-bit basic timer

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. It can be used for timebase generation with interrupt generation on timer overflow.

3.12 Beeper

The STM8L101xx devices include a beeper function used to generate a beep signal in the range of 1, 2 or 4 kHz when the LSI clock is operating at a frequency of 38 kHz.

3.13 Infrared (IR) interface

The STM8L101xx devices contain an infrared interface which can be used with an IR LED for remote control functions. Two timer output compare channels are used to generate the infrared remote control signals.

3.14 Comparators

The STM8L101xx features two zero-crossing comparators (COMP1 and COMP2) sharing the same current bias and voltage reference. The voltage reference can be internal (comparison with ground) or external (comparison to a reference pin voltage).

Each comparator is connected to 4 channels, which can be used to generate interrupt, timer input capture or timer break. Their polarity can be inverted.

3.15 USART

The USART interface (USART) allows full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

3.16 SPI

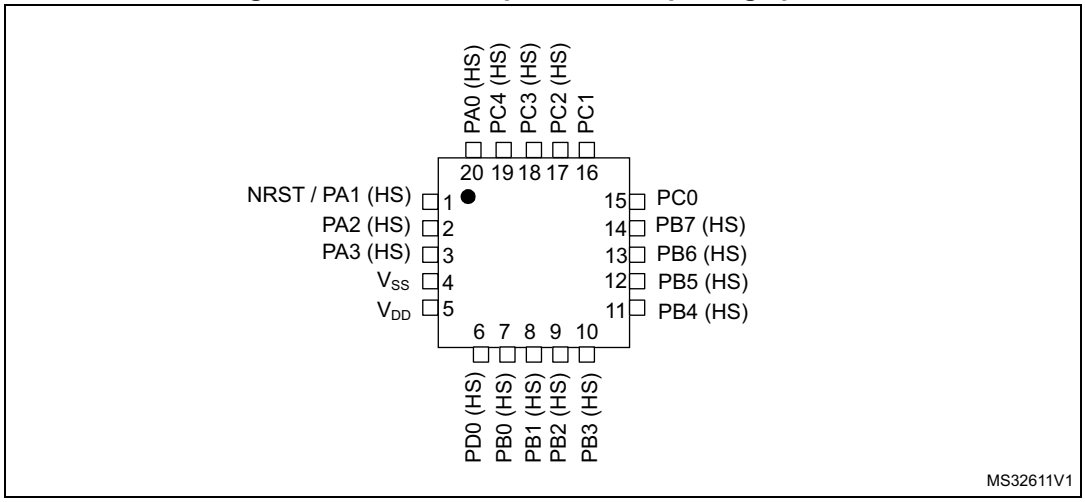
The serial peripheral interface (SPI) provides half/ full duplex synchronous serial communication with external devices. It can be configured as the master and in this case it provides the communication clock (SCK) to the external slave device. The interface can also operate in multi-master configuration.

3.17 I²C

The inter-integrated circuit (I2C) bus interface is designed to serve as an interface between the microcontroller and the serial I^2C bus. It provides multi-master capability, and controls all I²C bus-specific sequencing, protocol, arbitration and timing. It manages standard and fast speed modes.

4 Pin description

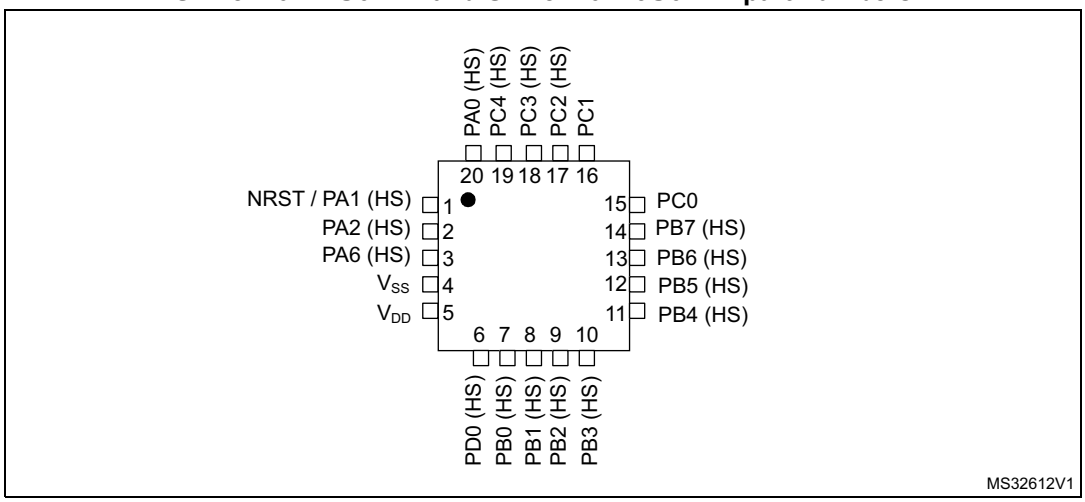
Figure 2. Standard 20-pin UFQFPN package pinout



1. HS corresponds to 20 mA high sink/source capability.
2. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

Note: The COMP_REF pin is not available in this standard 20-pin UFQFPN package. It is available on Port A6 in the Figure 3: 20-pin UFQFPN package pinout for STM8L101F1U6ATR, STM8L101F2U6ATR and STM8L101F3U6ATR part numbers.

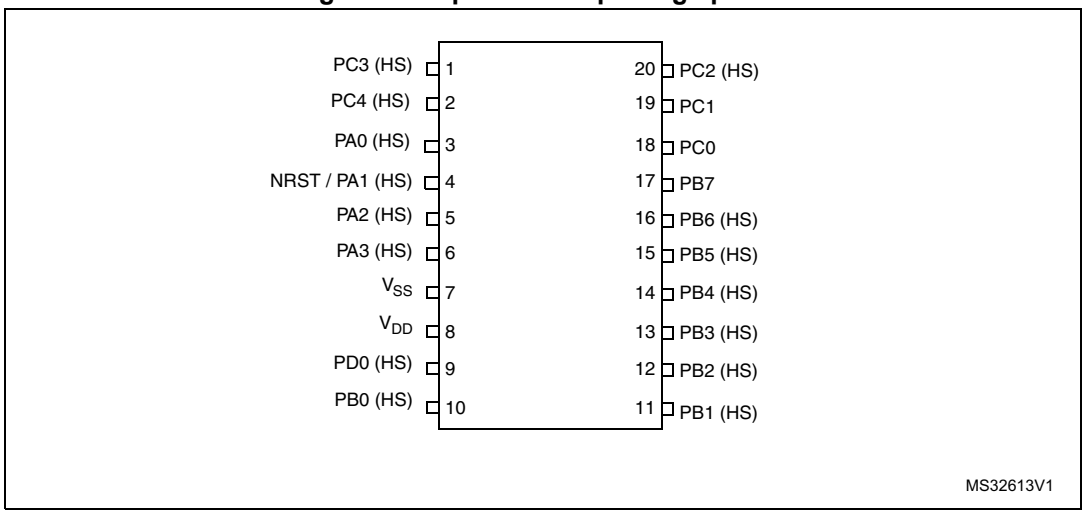
Figure 3. 20-pin UFQFPN package pinout for STM8L101F1U6ATR, STM8L101F2U6ATR and STM8L101F3U6ATR part numbers



1. Please refer to the warning below.
2. HS corresponds to 20 mA high sink/source capability.
3. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

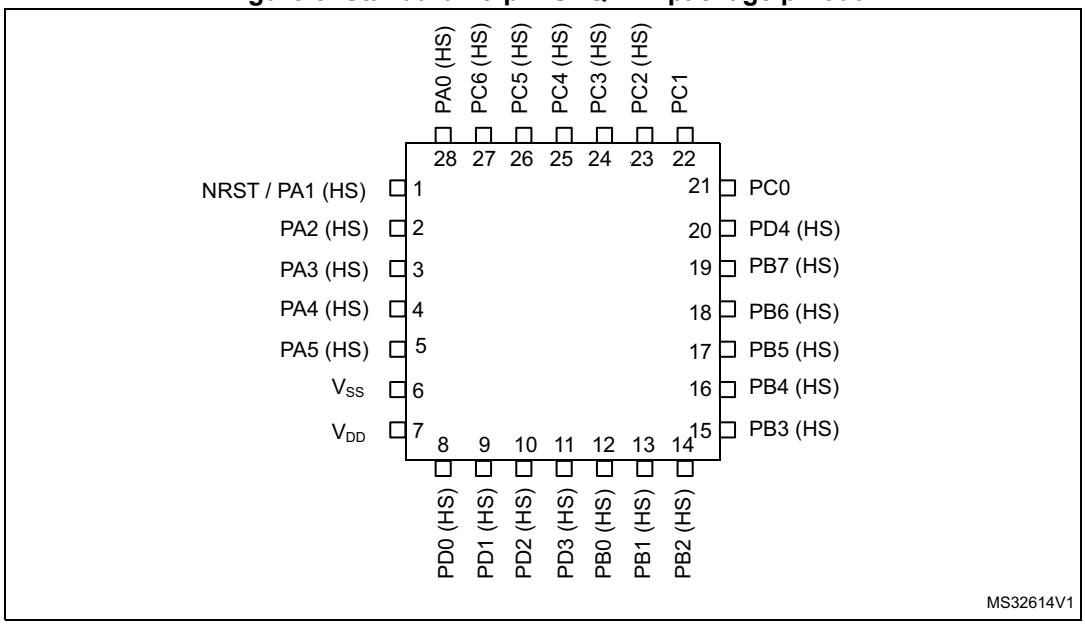
Warning: For the STM8L101F1U6ATR, STM8L101F2U6ATR and STM8L101F3U6ATR part numbers (devices with COMP_REF pin), all ports available on 32-pin packages must be considered as active ports. To avoid spurious effects, the user has to configure them as input pull-up. A small increase in consumption (typ. < 300 µA) may occur during the power up and reset phase until these ports are properly configured.

Figure 4. 20-pin TSSOP package pinout



1. HS corresponds to 20 mA high sink/source capability.
2. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

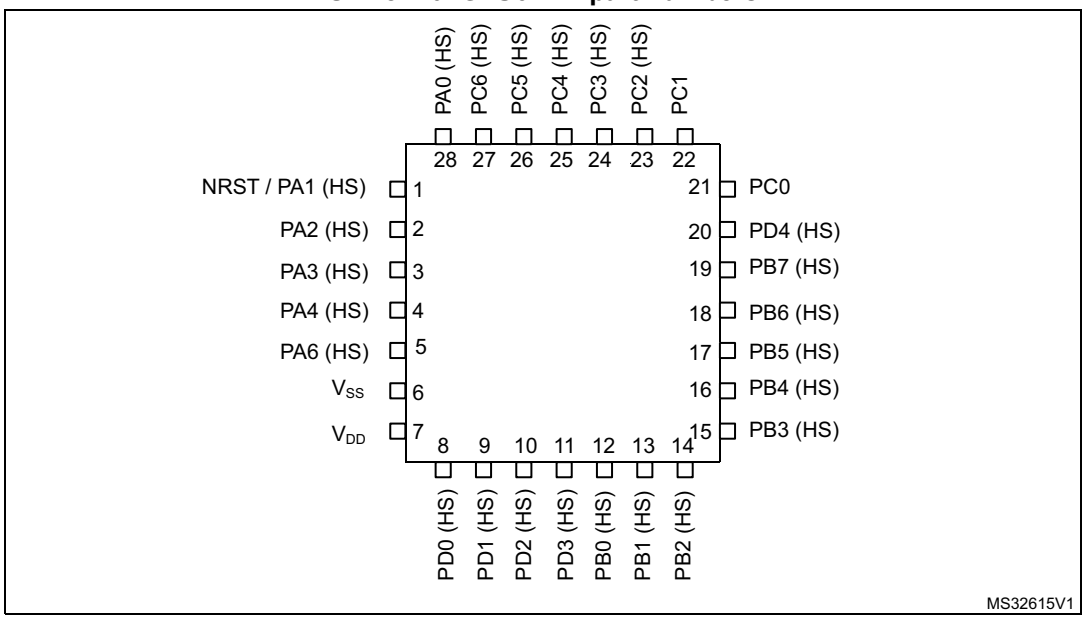
Figure 5. Standard 28-pin UFQFPN package pinout



1. HS corresponds to 20 mA high sink/source capability.
2. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

Note: The COMP_REF pin is not available in this standard 28-pin UFQFPN package. It is available on Port A6 in the Figure 6: 28-pin UFQFPN package pinout for STM8L101G3U6ATR and STM8L101G2U6ATR part numbers.

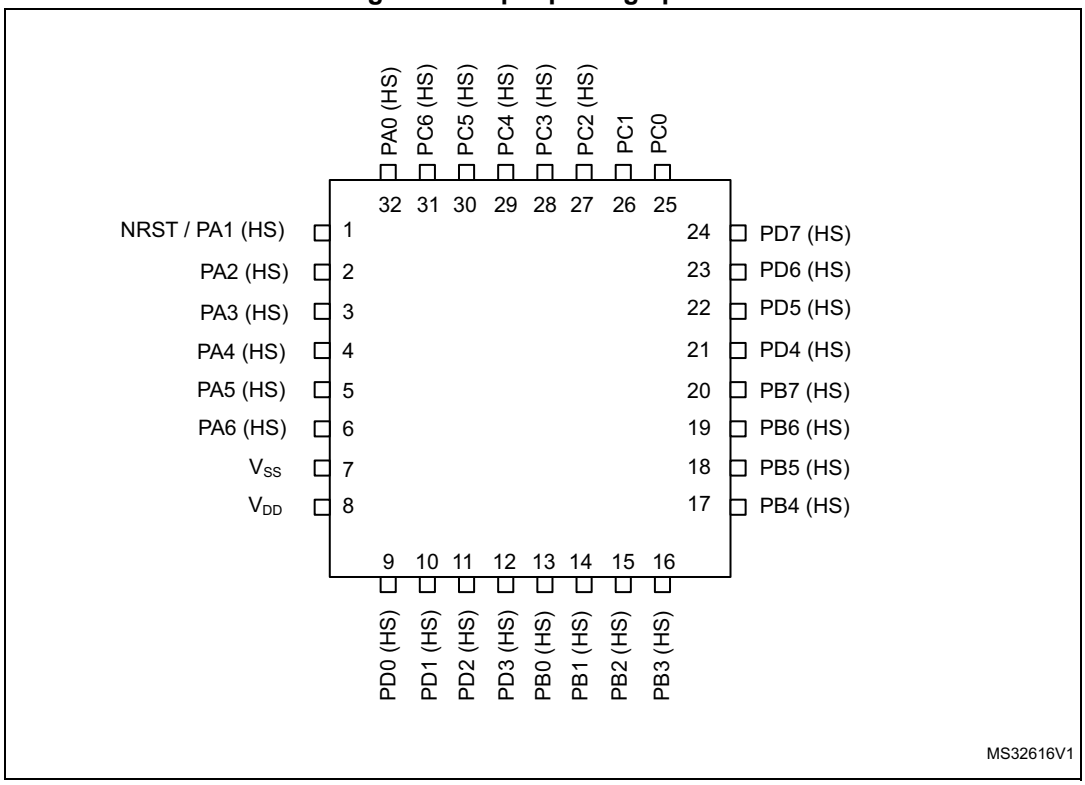
Figure 6. 28-pin UFQFPN package pinout for STM8L101G3U6ATR and STM8L101G2U6ATR part numbers



1. HS corresponds to 20 mA high sink/source capability.
2. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

Warning: For the STM8L101G3U6ATR and STM8L101G2U6ATR part numbers (devices with COMP_REF pin), all ports available on 32-pin packages must be considered as active ports. To avoid spurious effects, the user has to configure them as input pull-up. A small increase in consumption (typ. < 300 µA) may occur during the power up and reset phase until these ports are properly configured.

Figure 7. 32-pin package pinout



1. Example given for the UFQFPN32 package. The pinout is the same for the LQFP32 package.
2. HS corresponds to 20 mA high sink/source capability.
3. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

Table 3. Legend/abbreviation for table 4

Type	I= input, O = output, S = power supply	
Level	Input	CM = CMOS
	Output	HS = high sink/source (20 mA)
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state).	

Table 4. STM8L101xx pin description

Pin number						Pin name	Type	Input			Output			Main function (after reset)	Alternate function
standard UFQFPN20	UFQFPN20 with COMP_REF(1)	TSSOP20	standard UFQFPN28	UFQFPN28 with COMP_REF(1)	UFQFPN32 or LQFP32			floating	wpu	Ext. interrupt	High sink/source	OD	PP		
1	1	4	1	1	1	NRST/PA1(2)	I/O	-	**X**	-	HS	-	X	**Reset**	PA1
2	2	5	2	2	2	PA2	I/O	**X**	X	X	HS	X	X	**Port A2**	-
3	-	6	3	3	3	PA3	I/O	**X**	X	X	HS	X	X	**Port A3**	-
-	-	-	4	4	4	PA4/TIM2_BKIN	I/O	**X**	X	X	HS	X	X	**Port A4**	Timer 2 - break input
-	-	-	5	-	5	PA5/TIM3_BKIN	I/O	**X**	X	X	HS	X	X	**Port A5**	Timer 3 - break input
-	3	-	-	5	6	PA6/COMP_REF	I/O	**X**	X	X	HS	X	X	**Port A6**	Comparator external reference
4	4	7	6	6	7	V_{SS}	S	-	-	-	-	-	-	Ground	
5	5	8	7	7	8	V_{DD}	S	-	-	-	-	-	-	Power supply	
6	6	9	8	8	9	PD0/TIM3_CH2/ COMP1_CH3	I/O	**X**	X	X	HS	X	X	**Port D0**	Timer 3 - channel 2 / Comparator 1 - channel 3
-	-	-	9	9	10	PD1/TIM3_ETR/ COMP1_CH4	I/O	**X**	X	X	HS	X	X	**Port D1**	Timer 3 - trigger / Comparator 1 - channel 4
-	-	-	10	10	11	PD2/ COMP2_CH3	I/O	**X**	X	X	HS	X	X	**Port D2**	Comparator 2 - channel 3
-	-	-	11	11	12	PD3/ COMP2_CH4	I/O	**X**	X	X	HS	X	X	**Port D3**	Comparator 2 - channel 4

Table 4. STM8L101xx pin description (continued)

Pin number						Pin name	Type	Input			Output			Main function (after reset)	Alternate function
standard UFQFPN20	UFQFPN20 with COMP_REF(1)	TSSOP20	standard UFQFPN28	UFQFPN28 with COMP_REF(1)	UFQFPN32 or LQFP32			floating	wpu	Ext. interrupt	High sink/source	OD	PP		
7	7	10	12	12	13	PB0/TIM2_CH1/ COMP1_CH1 (3)	I/O	**X**(3)	X(3)	X	HS	X	X	**Port B0**	Timer 2 - channel 1 / Comparator 1 - channel 1
8	8	11	13	13	14	PB1/TIM3_CH1/ COMP1_CH2	I/O	**X**	X	X	HS	X	X	**Port B1**	Timer 3 - channel 1 / Comparator 1 - channel 2
9	9	12	14	14	15	PB2/ TIM2_CH2/ COMP2_CH1/	I/O	**X**	X	X	HS	X	X	**Port B2**	Timer 2 - channel 2 / Comparator 2 - channel 1
10	10	13	15	15	16	PB3/TIM2_ETR/ COMP2_CH2	I/O	**X**	X	X	HS	X	X	**Port B3**	Timer 2 - trigger / Comparator 2 - channel 2
11	11	14	16	16	17	PB4/SPI_NSS(3)	I/O	**X**(3)	X(3)	X	HS	X	X	**Port B4**	SPI master/slave select
12	12	15	17	17	18	PB5/SPI_SCK	I/O	**X**	X	X	HS	X	X	**Port B5**	SPI clock
13	13	16	18	18	19	PB6/SPI_MOSI	I/O	**X**	X	X	HS	X	X	**Port B6**	SPI master out/ slave in
14	14	17	19	19	20	PB7/SPI_MISO	I/O	**X**	X	X	HS	X	X	**Port B7**	SPI master in/ slave out
-	-	-	20	20	21	PD4	I/O	**X**	X	X	HS	X	X	**Port D4**	-
-	-	-	-	-	22	PD5	I/O	**X**	X	X	HS	X	X	**Port D5**	-
-	-	-	-	-	23	PD6	I/O	**X**	X	X	HS	X	X	**Port D6**	-
-	-	-	-	-	24	PD7	I/O	**X**	X	X	HS	X	X	**Port D7**	-
15	15	18	21	21	25	PC0/I2C_SDA	I/O	**X**	-	X	-	T(4)		**Port C0**	I2C data
16	16	19	22	22	26	PC1/I2C_SCL	I/O	**X**	-	X	-	T(4)		**Port C1**	I2C clock
17	17	20	23	23	27	PC2/USART_RX	I/O	**X**	X	X	HS	X	X	**Port C2**	USART receive
18	18	1	24	24	28	PC3/USART_TX	I/O	**X**	X	X	HS	X	X	**Port C3**	USART transmit
19	19	2	25	25	29	PC4/USART_CK/ CCO	I/O	**X**	X	X	HS	X	X	**Port C4**	USART synchronous clock / Configurable clock output

Table 4. STM8L101xx pin description (continued)

Pin number						Pin name	Type	Input			Output			Main function (after reset)	Alternate function
standard UFQFPN20	UFQFPN20 with COMP_REF(1)	TSSOP20	standard UFQFPN28	UFQFPN28 with COMP_REF(1)	UFQFPN32 or LQFP32			floating	wpu	Ext. interrupt	High sink/source	OD	PP		
-	-	-	26	26	30	PC5	I/O	**X**	X	X	HS	X	X	**Port C5**	-
-	-	-	27	27	31	PC6	I/O	**X**	X	X	HS	X	X	**Port C6**	-
20	20	3	28	28	32	PA0(5)/SWIM/ BEEP/IR_TIM (6)	I/O	X	**X**(5)	X	HS(6)	X	X	**Port A0**	SWIM input and output /Beep output/Timer Infrared output

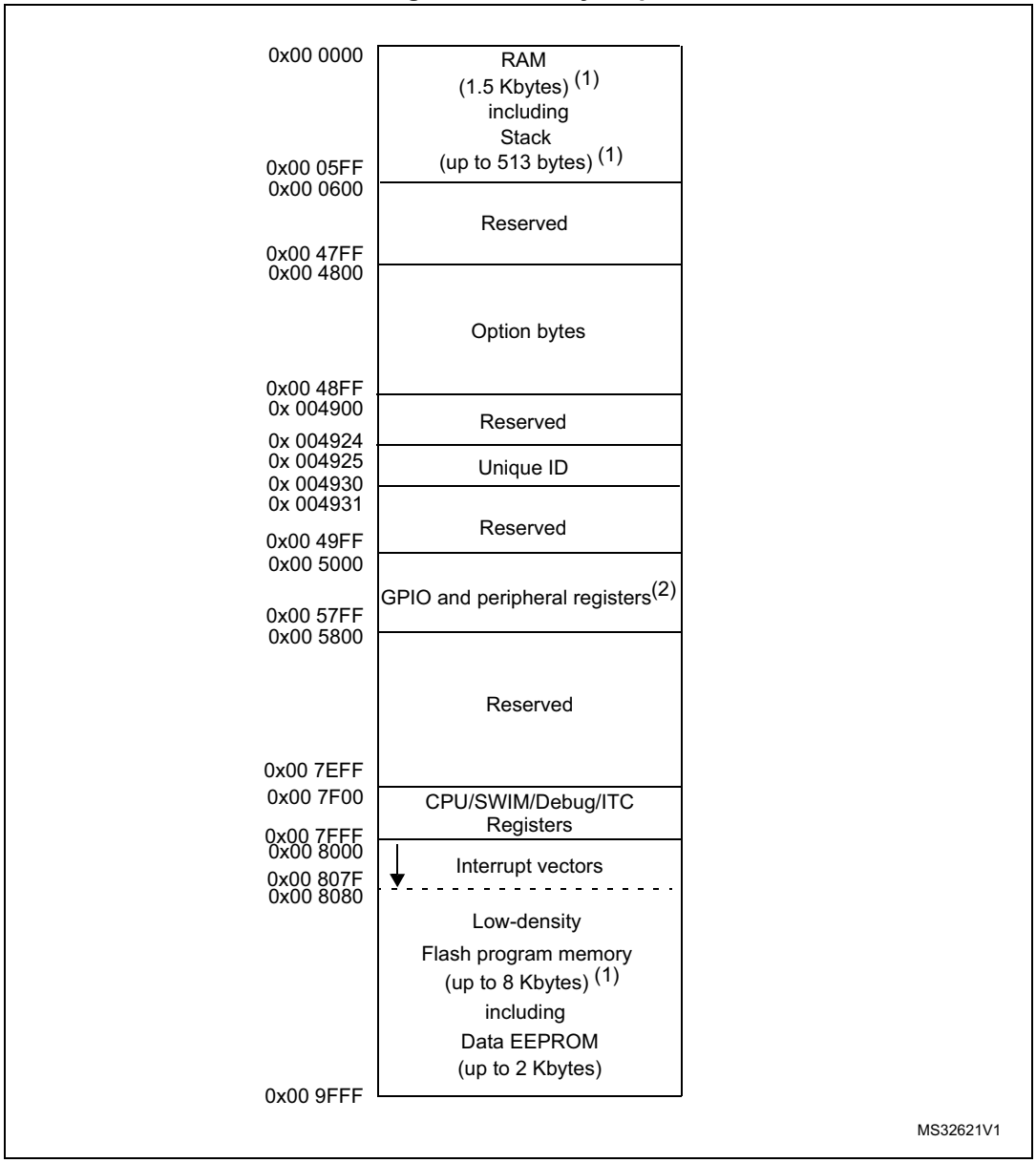
1. Please refer to the warning below.
2. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as a general purpose pin (PA1), it can be configured only as output push-pull, not neither as output open-drain nor as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L reference manual (RM0013).
3. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
4. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to V_{DD} are not implemented).
5. The PA0 pin is in input pull-up during the reset phase and after reset release.
6. High sink LED driver capability available on PA0.

Slope control of all GPIO pins can be programmed except true open drain pins and by default is limited to 2 MHz.

Warning: For the STM8L101F1U6ATR, STM8L101F2U6ATR, STM8L101F3U6ATR, STM8L101G2U6ATR and STM8L101G3U6ATR part numbers (devices with COMP_REF pin), all ports available on 32-pin packages must be considered as active ports. To avoid spurious effects, the user has to configure them as input pull-up. A small increase in consumption (typ. < 300 µA) may occur during the power up and reset phase until these ports are properly configured.

5 Memory and register map

Figure 8. Memory map



1. *Table 5* lists the boundary addresses for each memory size. The top of the stack is at the RAM end address.
2. Refer to *Table 7* for an overview of hardware register mapping, to *Table 6* for details on I/O port hardware registers, and to *Table 8* for information on CPU/SWIM/debug module controller registers.

Table 5. Flash and RAM boundary addresses

Memory area	Size	Start address	End address
RAM	1.5 Kbytes	0x00 0000	0x00 05FF
Flash program memory	2 Kbytes	0x00 8000	0x00 87FF
	4 Kbytes	0x00 8000	0x00 8FFF
	8 Kbytes	0x00 8000	0x00 9FFF

Note: 2 Kbytes of Data EEPROM is only available on devices with 8 Kbytes flash program memory.

Table 6. I/O Port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xxx
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xxx
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PC_IDR	Port C input pin value register	0xxx
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xxx
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x00
0x00 5013		PD_CR2	Port D control register 2	0x00

Table 7. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5050	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 5051		FLASH_CR2	Flash control register 2	0x00
0x00 5052		FLASH _PUKR	Flash Program memory unprotection register	0x00
0x00 5053		FLASH _DUKR	Data EEPROM unprotection register	0x00
0x00 5054		FLASH _IAPSR	Flash in-application programming status register	0xX0
0x00 5055 to 0x00 509F	Reserved area (75 bytes)			
0x00 50A0	ITC-EXTI	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2		EXTI_CR3	External interrupt control register 3	0x00
0x00 50A3		EXTI_SR1	External interrupt status register 1	0x00
0x00 50A4		EXTI_SR2	External interrupt status register 2	0x00
0x00 50A5		EXTI_CONF	External interrupt port select register	0x00
0x00 50A6	WFE	WFE_CR1	WFE control register 1	0x00
0x00 50A7		WFE_CR2	WFE control register 2	0x00
0x00 50A8 to 0x00 50AF	Reserved area (8 bytes)			
0x00 50B0	RST	RST_CR	Reset control register	0x00
0x00 50B1		RST_SR	Reset status register	0x01
0x00 50B2 to 0x00 50BF	Reserved area (14 bytes)			
0x00 50C0	CLK	CLK_CKDIVR	Clock divider register	0x03
0x00 50C1 to 0x00 50C2		Reserved area (2 bytes)		
0x00 50C3		CLK_PCKENR	Peripheral clock gating register	0x00
0x00 50C4		Reserved (1 byte)		
0x00 50C5		CLK_CCOR	Configurable clock control register	0x00
0x00 50C6 to 0x00 50DF	Reserved area (25 bytes)			